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Article

Low Buffer Trapping Effects above 1200 V in Normally off GaN-on-Silicon Field Effect Transistors

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Abstract: We report on the fabrication and electrical characterization of AlGa_xN/GaN normally off transistors on silicon designed for high-voltage operation. The normally off configuration was achieved with a p-gallium nitride (p-GaN) cap layer below the gate, enabling a positive threshold voltage higher than +1 V. The buffer structure was based on AlN/GaN superlattices (SLs), delivering a vertical breakdown voltage close to 1.5 kV with a low leakage current all the way to 1200 V. With the grounded substrate, the hard breakdown voltage transistors at $V_{GS} = 0$ V is 1.45 kV, corresponding to an outstanding average vertical breakdown field higher than 2.4 MV/cm. High-voltage characterizations revealed a state-of-the-art combination of breakdown voltage at $V_{GS} = 0$ V together with low buffer electron trapping effects up to 1.4 kV, as assessed by means of substrate ramp measurements.

Keywords: high-electron-mobility transistor (HEMT); GaN; normally off



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1. Introduction

Among the semiconductors, wide band gap (WBG) materials such as GaN and SiC show more suitable properties than Si to operate at higher power and higher voltage [1–6]. In addition to being available up to 8 inches on Si substrates, allowing a cost-effective fabrication, GaN material offers high electron mobility via the formation of a two-dimensional electron gas (2DEG) at the hetero-interface between the AlGa_xN barrier and the GaN channel layer. These devices are inherently normally on, delivering a negative threshold voltage. In order to achieve a normally off behavior, several methods have been reported in the literature [7–15]. All of them involve depleting the 2DEG below the gate electrode. One of the most promising approach is the use of a p-GaN layer that is etched outside the gate contact region [16–18]. In this case, the p-GaN layer raises the band diagram, causing the depletion of the 2DEG even without external bias. On the other hand, although these types of devices are commercially available, they are limited to 650 V voltage operation. Buffer engineering is required to generate highly insulating transition layers grown on silicon and further enhance the voltage operation. The use of graded AlGa_xN buffer layers is the historical approach [19–21]. Al_xGa_{1-x}N layers (several micrometers thick with different Al contents) allow the alleviation of lattice mismatch and thermal expansion between the silicon substrate and the GaN layer. Moreover, the introduction of intentional doping can significantly increase the resistivity of the buffer. Iron or carbon doping is generally used to produce highly resistive buffers by compensating the residual n-type doping, such as oxygen impurities, generally inducing parasitic leakage currents. However, it has been shown that a high Fe or C doping concentration generates electron trapping effects [22–24]. To suppress the undesired trapping effects while maintaining an excellent carrier confinement into the 2DEG under a high electric field, AlGa_xN back barrier [25] or superlattice buffer concepts [26,27] can be combined with a moderate C doping concentration. The desire to use AlN/GaN superlattices along with a carbon-doped buffer has been previously demonstrated for high-voltage capabilities in normally on transistors [28,29]. This concept

involves a series of thin layers such as Al(Ga)N and GaN to avoid the formation of internal stresses while benefiting from highly resistive buffer layers.

In this paper, we experimentally fabricated normally off p-GaN cap AlGaN/GaN HEMTs using a superlattice buffer with a total thickness of 6 μm , combining a high blocking voltage at $V_{\text{GS}} = 0 \text{ V}$ and low trapping effects above 1 kV.

2. Materials and Methods

Figure 1 shows a schematic cross-section of the p-GaN/AlGaN/GaN heterostructures grown by metal organic chemical vapor deposition (MOCVD) on a 1 mm-thick 6-inch Si substrate. Following the AlN nucleation layer, a 6 μm total buffer thickness based on 140 periods of 25 nm AlN/GaN superlattice and a carbon-doped GaN layer of $5 \times 10^{18} \text{ cm}^{-3}$, an unintentionally doped GaN channel, a 12 nm Al_{0.18}Ga_{0.82}N barrier layer, and an 80 nm p-type doped GaN layer. The Mg concentration was $2 \times 10^{19} \text{ cm}^{-3}$.

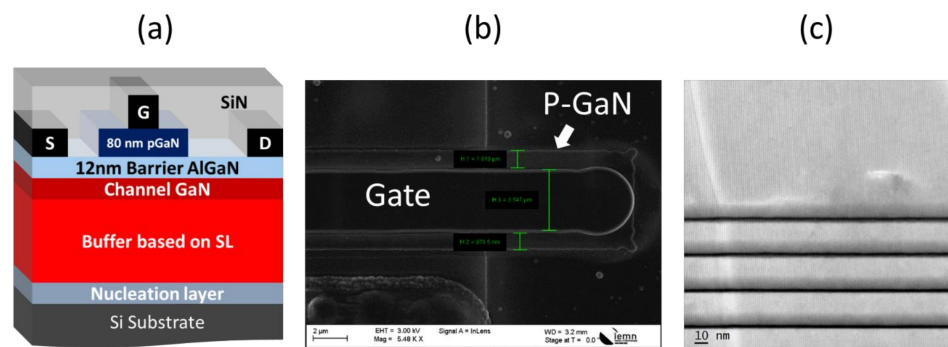


Figure 1. (a) Schematic cross section of the p-GaN/AlGaN/GaN HEMT on Si. (b) SEM top view of the gate including the partially etched p-GaN layer and (c) a zoomed TEM image of the superlattices.

The 2DEG properties obtained through Van der Pauw pattern showed an electron sheet concentration of $8 \times 10^{12} \text{ cm}^{-2}$ with an electron mobility of $1800 \text{ cm}^2/\text{V}\cdot\text{s}$. A Ti/Al/Ni/Au metal stack was deposited and annealed at $750 \text{ }^\circ\text{C}$ to form the source and drain ohmic contacts directly on top of the barrier layer by fully etching the p-GaN cap layer. Contact resistances of about $1 \text{ }\Omega\cdot\text{mm}$ were obtained, which can be reduced with further optimization. The isolation between contacts was realized by mesa etching with a depth of 400 nm. Outside the gate area, the entire remaining p-GaN area was etched and a Ni/Au gate metal was deposited. Lastly, a 150 nm PECVD SiN layer was deposited as final passivation.

3. Results

Figure 2a shows the vertical breakdown voltage close to 1500 V corresponding to an excellent breakdown field higher than 2.4 MV/cm. This reflects the high crystal quality of the growth related to the superlattice concept. It can be pointed out that typical values for a similar buffer thickness are below 2 MV/cm.

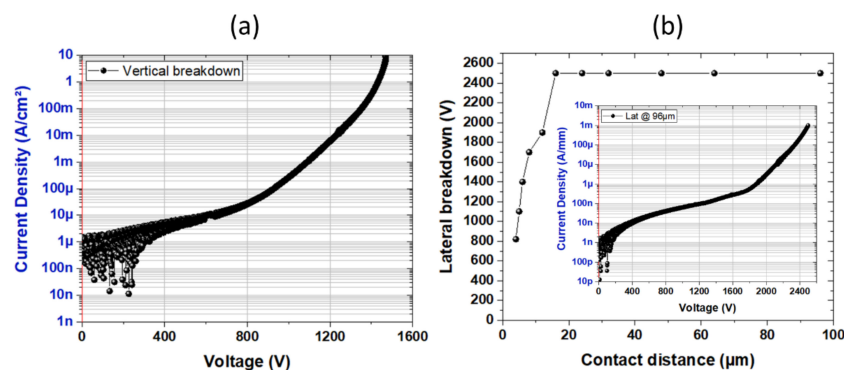


Figure 2. Vertical breakdown voltage (a) and lateral floating breakdown voltage as a function of the contact distances (b) and the p-GaN/AlGaN/GaN HEMT on Si at room temperature.

Lateral breakdown voltage measurements between isolated ohmic contacts on various distances with the substrate floating confirm the high-voltage capabilities. In order to avoid arcing in air between the probes, the sample is immersed in a liquid solution (Fluorinert). As shown in Figure 2b, an expected linear evolution of the breakdown voltage as a function of the contact distances followed by saturation is observed. A significant lateral breakdown voltage up to 2500 V is measured for a contact distance of 16 μm and above. It can be noticed that a blocking voltage of about 2000 V is reached at 1 $\mu\text{A}/\text{mm}$.

Moreover, a key parameter to assess GaN-based for power switch devices is the trapping effects. Thus, buffer trapping has been studied by means of substrate ramp measurements. [30,31]. This measurement is essentially sensitive to the traps into the buffer and surface independent. Indeed, a low bias is applied within a TLM (ohmic contacts), generating a current while the substrate is biased from 0 V down to a high negative potential. Any charge redistribution into the buffer during the sweeps (back and forth) will be detected as a current change (hysteresis). Indications on the time constant of the traps can also be determined to a certain extent by varying the sweep rate.

Figure 3 shows different measurements down to 500 V, 1000 V, and 1400 V at various sweep rates of 4 V/s in blue and 22 V/s in black. Extremely low hysteresis is evident in all cases, reflecting the outstanding low trapping effects observed up to 1400 V, regardless of the sweep speeds. This is attributed to the excellent material quality and the low charge storage within the structure, enabling both a superior breakdown field and reduced buffer trapping.

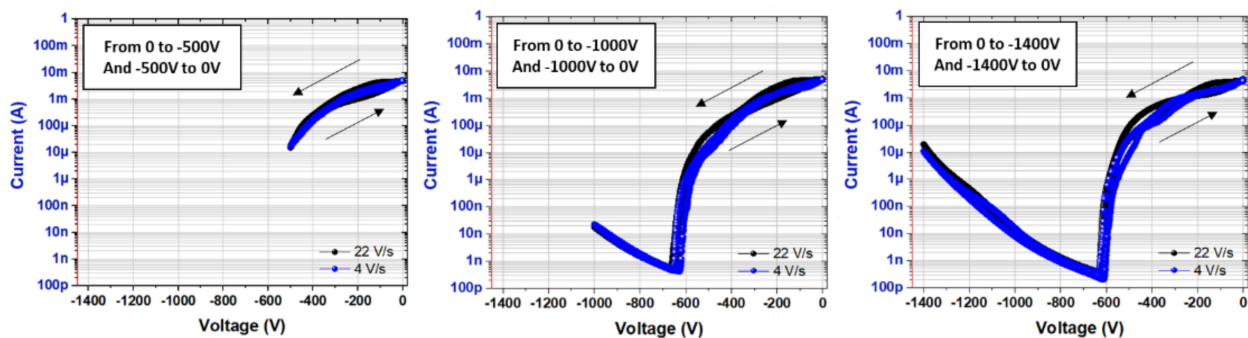


Figure 3. Substrate bias ramp measurements performed on the p-GaN/AlGaN/GaN HEMT on Si at room temperature.

Electrical characterizations are carried out on $2 \times 50 \mu\text{m}$ transistors with a gate-to-drain spacing, ranging from 8 to 40 μm . Transfer characteristics I_D - V_{GS} , as shown in Figure 4 at $V_{DS} = 4 \text{ V}$, reveal a low leakage current around 20 nA/mm and an excellent pinch-off behavior, showing the absence of parasitic punch-through effects or gate leakage current. Moreover, from the transfer characteristics plotted in semi-log and linear, a threshold voltage as high as +1.4 V is extracted, resulting in fully normally off transistors. Due to non-optimized ohmic contacts and a rather low Al content into the barrier, a moderate on-state current density of 150 mA/mm and an on-state resistance (R_{ON}) of about 32 $\text{m}\Omega/\text{cm}^2$ is obtained, as seen from the output characteristics in Figure 4.

Figure 5a shows the three-terminal off-state breakdown voltage of transistors at $V_{GS} = 0 \text{ V}$ as a function of the gate–drain distances with a floating and grounded substrate. The breakdown voltages of transistors with a grounded substrate are slightly higher than 1400 V, in agreement with the high breakdown field of the buffer layers. Similarly, as can also be seen in Figure 5b, the breakdown voltage with a floating substrate reaches 2500 V for large gate–drain distances higher than 20 μm . The leakage current remains below 1 $\mu\text{A}/\text{mm}$ above 1 kV. The specific on-state resistance versus breakdown voltage with grounded substrate has been benchmarked against normally off GaN transistors in the literature (Figure 6) [32–36]. These results highlight the benefits of superlattice-based buffer,

enabling high-performance normally off devices with low R_{ON} and low buffer trapping at a blocking voltage above 1200 V.

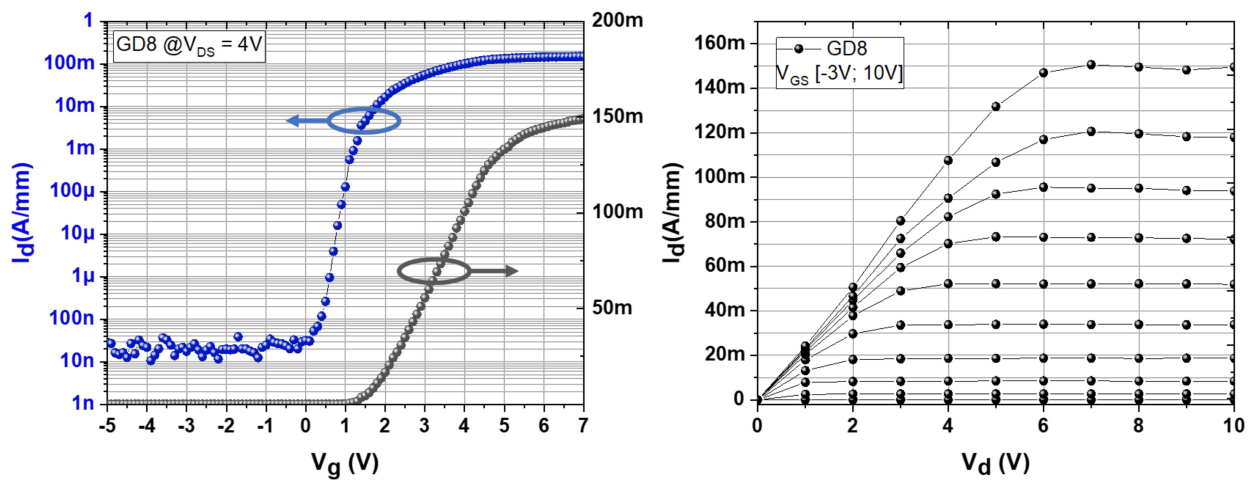


Figure 4. Transfer (left) and output (right) characteristics of a p-GaN/AlGaIn/GaN HEMT with a gate–drain distance of 8 μm at $V_{DS} = 4\text{ V}$ plotted in semi-log and linear scale.

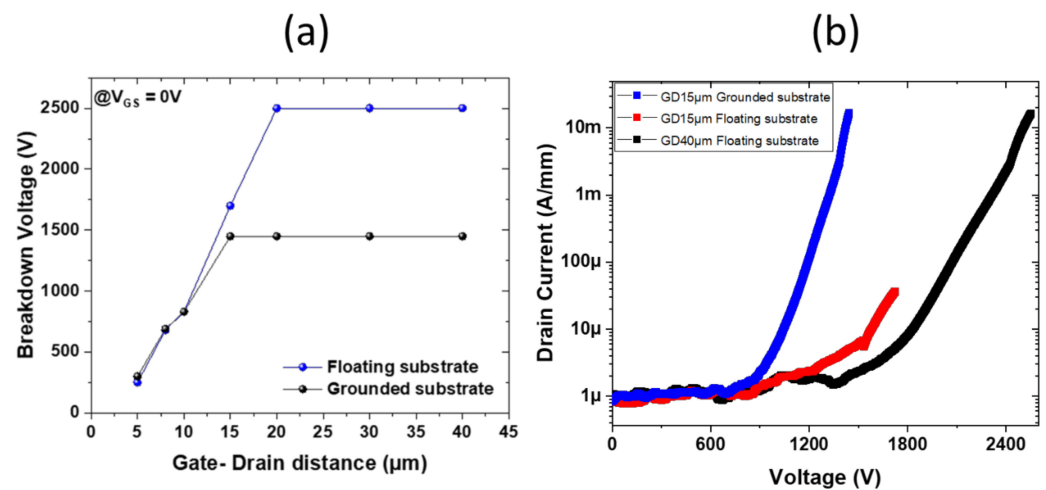


Figure 5. Three-terminal breakdown voltage at $V_{GS} = 0\text{ V}$ of p-GaN/AlGaIn/GaN HEMTs with floating and grounded substrate: (a) as a function of the gate-to-drain distance and (b) for various gate-to-drain distances.

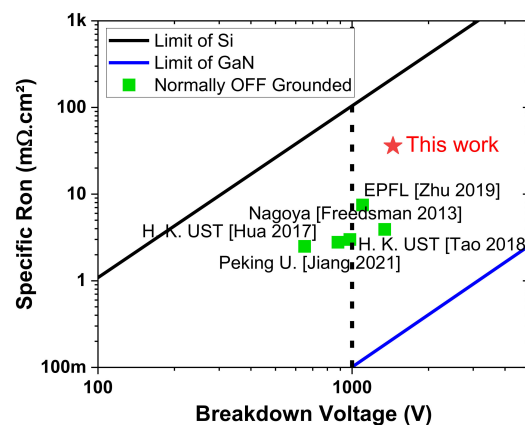


Figure 6. Benchmarking of breakdown voltage vs. specific on-resistance of normally off transistors with a grounded substrate. Solid lines in black and blue represent the theoretical limits of Si and GaN, respectively.

4. Conclusions

In summary, this paper demonstrated the fabrication and characterization of a state-of-the-art normally off AlGa_N/Ga_N heterostructure with a buffer based on superlattice structure capped with a p-GaN layer. This resulted in normally off transistors with a threshold voltage higher than +1 V. High vertical breakdown voltage close to 1500 V can be reached with low trapping effects. The three-terminal breakdown voltage measurements carried out on transistors show a breakdown field higher than 2.4 MV/cm with a grounded substrate and a breakdown voltage of 2500 V with floating substrate. These results unveil the excellent prospects of a superlattice-based buffer for 1200 V power applications, such as fast chargers for electric vehicles, motor drives, solar inverters, or three-phase PFC systems.

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References

1. Dogmus, E.; Zegaoui, M.; Medjdoub, F. GaN-on-silicon high-electron-mobility transistor technology with ultra-low leakage up to 3000 V using local substrate removal and AlN ultra-wide bandgap. *Appl. Phys. Express* **2018**, *11*, 034102. [[CrossRef](#)]
2. Baliga, B.J. Gallium nitride devices for power electronic applications. *Semicond. Sci. Technol.* **2013**, *28*, 074011. [[CrossRef](#)]
3. Millán, J.; Godignon, P. Wide Band Gap Power Semiconductor Devices. In Proceedings of the 2013 Spanish Conference on Electron Devices, Valladolid, Spain, 12–14 February 2013.
4. Abid, I.; Mehta, J.; Cordier, Y.; Derluyn, J.; Degroote, S.; Miyake, H.; Medjdoub, F. AlGa_N Channel High Electron Mobility Transistors with Regrown Ohmic Contacts. *Electronics* **2021**, *10*, 635. [[CrossRef](#)]
5. Zhong, Y.; Zhang, J.; Wu, S.; Jia, L.; Yang, X.; Liu, Y.; Zhang, Y.; Sun, Q. A review on the GaN-on-Si power electronic devices. *Fundam. Res.* **2022**, *2*, 462–475. [[CrossRef](#)]
6. Herbecq, N.; Roch-Jeune, I.; Linge, A.; Grimbert, B.; Zegaoui, M.; Medjdoub, F. GaN-on-silicon high electron mobility transistors with blocking voltage of 3 kV. *Electron. Lett.* **2015**, *51*, 1532–1534. [[CrossRef](#)]
7. Huang, X.; Liu, Z.; Li, Q.; Lee, F.C. Evaluation and application of 600 v GaN HEMT in cascode structure. *IEEE Trans. Power Electron.* **2014**, *29*, 2453–2461. [[CrossRef](#)]
8. Huang, X.; Li, Q.; Liu, Z.; Lee, F.C. Analytical loss model of high voltage GaN HEMT in cascode configuration. *IEEE Trans. Power Electron.* **2014**, *29*, 22208–22219. [[CrossRef](#)]
9. Sorrentino, G.; Melito, M.; Patti, A.; Parrino, G.; Raciti, A. GaN HEMT devices: Experimental results on normally-on, normally-off and cascode configuration. In Proceedings of the IECON 2013—39th Annual Conference of the IEEE Industrial Electronics Society, Vienna, Austria, 10–13 November 2013; pp. 816–821.
10. Chen, K.J.; Yuan, L.; Wang, M.J.; Chen, H.; Huang, S.; Zhou, Q.; Zhou, C.; Li, B.K.; Wang, J.N. Physics of fluorine plasma ion implantation for GaN normally-off HEMT technology. In Proceedings of the 2011 International Electron Devices Meeting, Washington, DC, USA, 5–7 December 2011; Volume 1, pp. 465–468.
11. Zhang, Z.; Fu, K.; Deng, X.; Zhang, X.; Fan, Y.; Sun, S.; Song, L.; Xing, Z.; Huang, W.; Yu, G.; et al. Normally Off AlGa_N/Ga_N MIS-High-Electron Mobility Transistors Fabricated by Using Low Pressure Chemical Vapor Deposition Fluorine Ion Implantation. *IEEE Electron Device Lett.* **2015**, *36*, 1128–1131. [[CrossRef](#)]
12. Wu, C.-H.; Han, P.-C.; Luc, Q.H.; Hsu, C.-Y.; Hsieh, T.-E.; Wang, H.-C.; Lin, Y.-K.; Chang, P.-C.; Lin, Y.-C.; Chang, E.Y. Normally-Off GaN MIS-HEMT with F-Doped Gate Insulator Using Standard Ion Implantation. *IEEE J. Electron Devices Soc.* **2018**, *6*, 893–899. [[CrossRef](#)]
13. Saito, W.; Takada, Y.; Kuraguchi, M.; Tsuda, K.; Omura, I. Recessed-gate structure approach toward normally off high-voltage AlGa_N/Ga_N HEMT for power electronics applications. *IEEE Trans. Electron Devices* **2006**, *53*, 356–362. [[CrossRef](#)]
14. Burnham, S.D.; Boutros, K.; Hashimoto, P.; Butler, C.; Wong, D.W.; Hu, M.; Micovic, M. Gate-recessed normally-off GaN-on-Si HEMT using a new O₂-BCl₃ digital etching technique. *Phys. Status Solidi Curr. Top. Solid State Phys.* **2010**, *7*, 2010–2012.

15. Oka, T.; Nozawa, T. AlGaIn/GaN recessed MIS-Gate HFET with high-threshold-voltage normally-off operation for power electronics applications. *IEEE Electron Device Lett.* **2008**, *29*, 668–670. [[CrossRef](#)]
16. Hwang, I.; Choi, H.; Lee, J.; Choi, H.S.; Kim, J.; Ha, J.; Um, C.-Y.; Hwang, S.-K.; Oh, J.; Kim, J.-Y.; et al. 1.6kV, 2.9 mΩcm² normally-off p-GaN HEMT device. In Proceedings of the 2012 24th International Symposium on Power Semiconductor Devices and ICs, Bruges, Belgium, 3–7 June 2012.
17. Hilt, O.; Brunner, F.; Cho, E.; Knauer, A.; Bahat-Treidel, E.; Wurfl, J. Normally-off high-voltage p-GaN gate GaN HFET with carbon-doped buffer. In Proceedings of the 2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs, San Diego, CA, USA, 23–26 May 2011; Volume 50, pp. 239–242.
18. Meneghini, M.; Hilt, O.; Wuerfl, J.; Meneghesso, G. Technology and reliability of normally-off GaN HEMTs with p-type gate. *Energies* **2017**, *10*, 153. [[CrossRef](#)]
19. Li, C.; Li, Z.; Peng, D.; Ni, J.; Pan, L.; Zhang, D.; Dong, X.; Kong, Y. Improvement of breakdown and current collapse characteristics of GaN HEMT with a polarization-graded AlGaIn buffer. *Semicond. Sci. Technol.* **2015**, *30*, 035007. [[CrossRef](#)]
20. Able, A.; Wegscheider, W.; Engl, K.; Zweck, J. Growth of crack-free GaN on Si(111) with graded AlGaIn buffer layers. *J. Cryst. Growth* **2005**, *276*, 415–418. [[CrossRef](#)]
21. Yang, Y.; Xiang, P.; Liu, M.; Chen, W.; He, Z.; Han, X.; Ni, Y.; Yang, F.; Yao, Y.; Wu, Z.; et al. Effect of compositionally graded AlGaIn buffer layer grown by different functions of trimethylaluminum flow rates on the properties of GaN on Si (111) substrates. *J. Cryst. Growth* **2013**, *376*, 23–27. [[CrossRef](#)]
22. Meneghini, M.; Rossetto, I.; Bisi, D.; Stocco, A.; Chini, A.; Pantellini, A.; Lanzieri, C.; Nanni, A.; Meneghesso, G.; Zanoni, E. Buffer Traps in Fe-Doped AlGaIn/GaN HEMTs: Investigation of the Physical Properties Based on Pulsed and Transient Measurements. *IEEE Trans. Electron Devices* **2014**, *61*, 4070–4077. [[CrossRef](#)]
23. Verzellesi, G.; Morassi, L.; Meneghesso, G.; Meneghini, M.; Zanoni, E.; Pozzovivo, G.; Lavanga, S.; Detzel, T.; Haberlen, O.; Curatola, G. Influence of Buffer Carbon Doping on Pulse and AC Behavior of Insulated-Gate Field-Plated Power AlGaIn/GaN HEMTs. *IEEE Electron Device Lett.* **2014**, *35*, 443–445. [[CrossRef](#)]
24. Moens, P.; Vanmeerbeek, P.; Banerjee, A.; Guo, J.; Liu, C.; Coppens, P.; Salih, A.; Tack, M.; Caesar, M.; Uren, M.J.; et al. On the impact of carbon-doping on the dynamic Ron and off-state leakage current of 650 V GaN power devices 2015. In Proceedings of the 2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD), Hong Kong, China, 10–14 May 2015.
25. Medjdoub, F.; Zegaoui, M.; Grimbert, B.; Rolland, N.; Rolland, P.A. Effects of AlGaIn Back Barrier on AlN/GaN-on-Silicon High-Electron-Mobility Transistors. *Appl. Phys. Express* **2011**, *4*, 124101. [[CrossRef](#)]
26. Li, A.; Wang, C.; He, Y.; Zheng, X.; Ma, X.; Zhao, Y.; Liu, K.; Hao, Y. GaN-based super-lattice Schottky barrier diode with low forward voltage of 0.81 V. *Superlattices Microstruct.* **2021**, *156*, 106952. [[CrossRef](#)]
27. Heuken, L.; Kortemeyer, M.; Ottaviani, A.; Schröder, M.; Alomari, M.; Fahle, D.; Marx, M.; Heuken, M.; Kalisch, H.; Vescan, A.; et al. Analysis of an AlGaIn/AlN Super-Lattice Buffer Concept for 650-V Low-Dispersion and High-Reliability GaN HEMTs. *IEEE Trans. Electron Devices* **2020**, *67*, 1113–1119. [[CrossRef](#)]
28. Kabouche, R.; Abid, I.; Püsche, R.; Derluyn, J.; Degroote, S.; Germain, M.; Tajalli, A.; Meneghini, M.; Meneghesso, G.; Medjdoub, F. Low On-Resistance and Low Trapping Effects in 1200 V Superlattice GaN-on-Silicon Heterostructures. *Phys. Status Solidi (a)* **2019**, *217*, 1900687. [[CrossRef](#)]
29. Tajalli, A.; Meneghini, M.; Besendörfer, S.; Kabouche, R.; Abid, I.; Püsche, R.; Derluyn, J.; Degroote, S.; Germain, M.; Meissner, E.; et al. High Breakdown Voltage and Low Buffer Trapping in Superlattice GaN-on-Silicon Heterostructures for High Voltage Applications. *Materials* **2020**, *13*, 4271. [[CrossRef](#)]
30. Moens, P.; Banerjee, A.; Uren, M.J.; Meneghini, M.; Karboyan, S.; Chatterjee, I.; Vanmeerbeek, P.; Cäsar, M.; Liu, C.; Salih, A.; et al. Impact of buffer leakage on intrinsic reliability of 650V AlGaIn/GaN HEMTs. In Proceedings of the 2015 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 7–9 December 2015.
31. Uren, M.J.; Karboyan, S.; Chatterjee, I.; Pooth, A.; Moens, P.; Banerjee, A.; Kuball, M. “Leaky Dielectric” Model for the Suppression of Dynamic RON in Carbon Doped AlGaIn/GaN HEMTs. *IEEE Trans. Electron Devices* **2017**, *64*, 2826–2834. [[CrossRef](#)]
32. Freedman, J.J.; Kubo, T.; Egawa, T. High drain current density e-mode Al₂O₃/AlGaIn/GaN MOS-HEMT on Si with enhanced power device figure-of-merit ($4 \times 10^8 \text{V}^2 \Omega^{-1} \text{cm}^{-2}$). *IEEE Trans. Electron Devices* **2013**, *60*, 3079–3083. [[CrossRef](#)]
33. Hua, M.; Wei, J.; Tang, G.; Zhang, Z.; Qian, Q.; Cai, X.; Wang, N.; Chen, K.J. Normally-off LPCVD-SiN_x/GaN MIS-FET with crystalline oxidation interlayer. *IEEE Electron Device Lett.* **2017**, *38*, 929–932. [[CrossRef](#)]
34. Tao, M.; Liu, S.; Xie, B.; Wen, C.P.; Wang, J.; Hao, Y.; Wu, W.; Cheng, K.; Shen, B.; Wang, M. Characterization of 880 V Normally Off GaN MOSHEMT on Silicon Substrate Fabricated With a Plasma-Free, Self-Terminated Gate Recess Process. *IEEE Trans. Electron Devices* **2018**, *65*, 1453–1457. [[CrossRef](#)]
35. Jiang, H.; Lyu, Q.; Zhu, R.; Xiang, P.; Cheng, K.; Lau, K.M. 1300 V Normally-OFF p-GaN Gate HEMTs on Si With High ON-State Drain Current. *IEEE Trans. Electron Devices* **2021**, *68*, 653–657. [[CrossRef](#)]
36. Zhu, M.; Ma, J.; Nela, L.; Erine, C.; Matioli, E. High-Voltage Normally-off Recessed Tri-Gate GaN Power MOSFETs With Low on-Resistance. *IEEE Electron Device Lett.* **2019**, *40*, 1289–1292. [[CrossRef](#)]