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# Tunneling FET Calibration Issues: Sentaurus vs. Silvaco TCAD

Amira Nabil<sup>1,3\*</sup>, Ahmed Shaker<sup>2</sup>, Mohamed Abouelatta<sup>1</sup>, Hani Ragai<sup>1</sup> and Christian Gontrand<sup>4,5</sup>

<sup>1</sup>Department of and Electronics and Electrical Communications, Faculty of Engineering, Ain Shams University, 11517 Cairo, Egypt

<sup>2</sup>Department of Engineering Physics and Mathematics, Faculty of Engineering, Ain Shams University, 11517 Cairo, Egypt

<sup>3</sup>Department of and Electronics and Electrical Communications, Higher Institute for Engineering and Technology, Fifth settlement, New Cairo, Egypt

<sup>4</sup>INL-INSA Lyon, Université de Lyon, 7 avenue Jean Capelle 69621 Villeurbanne, France

<sup>5</sup>IEP, INSA- Fès, Université Euro-méditerranéenne de Fès, Marocco

\*amira\_nabil64@hotmail.com

**Abstract.** In this paper, a comprehensive comparison of TFET simulations using two TCAD simulators, Sentaurus and Silvaco TCAD, is presented. The comparison is fully cover various types of TFETs, either from the structure geometry or the materials point of view, which proved a framework for TFET designs and simulations. For Sentaurus TCAD, a dynamic nonlocal BTBT model is used for all simulations as it is proved a good calibration for experimental data or full quantum data taken from the literature. The BTBT model's parameters are determined for different material and hetero-junctions structures where they can be used directly for any design or structure calibration. For the Silvaco simulator, a nonlocal BTBT model is utilized for calibration and its parameters are also provided. The study offers quick parameters data to be used directly, utilizing various materials without being involved in calibration difficulties.

## 1. Introduction

Tunneling field-effect transistors (TFETs) has been innovated as an alternative to tackle some challenges of traditional MOSFET transistors [1, 2]. The current in TFET is mainly due to band-to-band tunneling (BTBT) phenomena rather than thermionic emission in MOSFET [3, 4]. TFET can operate well at low supply voltage providing low OFF current [2, 5]. However, TFETs face a low ON current [2], am-bipolarity of current, and implementation difficulties [6].

Performance enhancement of TFETs is done to acquire mainly a higher ON current and to overcome other TFET obstacles [7]. In this regard, different structures are investigated, such as multi-gate [1] or gate all around (GAA) [8] structures, which can be entirely fabricated by CMOS technology and reduce short-channel effects. Hetero structures may also be used to enhance the TFET characteristics where the source material is replaced by a smaller bandgap material i.e. Ge or Mg<sub>2</sub>Si [2, 9]. Using such low bandgap materials results in a reduction of the tunneling resistance, so the ON current, in turn, is improved. Other III-V materials may completely replace Si to provide a good



tunneling probability like InAs [10], which has a direct bandgap instead of the indirect bandgap of Silicon.

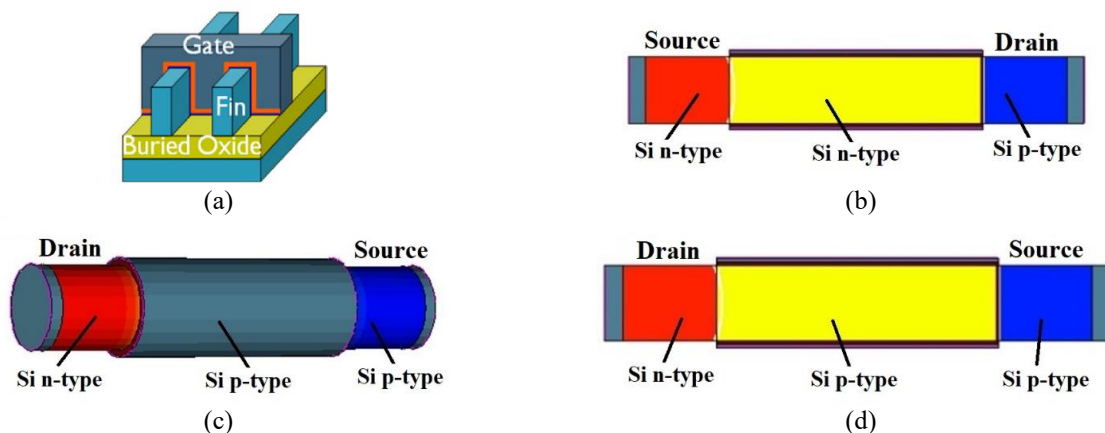
Many studies have been done on TFET fabrications [11, 12]. Others utilized the simulation results to predict, design, and optimize the TFETs performance [13, 14]. Many simulator tools are used such that Sentaurus [15] and Silvaco [16] TCAD simulators, which provide efficient BTBT models. Regarding TCAD environments, four models are equipped to track the BTBT phenomena [15]: Kane model, Hurkx model, Schenk model, and the nonlocal model. Among them, the nonlocal BTBT model is found to be the most accurate model to simulate tunneling in TFETs [15-17].

In Silvaco, the nonlocal BTBT model has to be accompanied by a fine quantum meshing around the expected tunneling area. On the other hand, in Sentaurus, the nonlocal model gives a dynamic path of tunneling starting from the Valence band (VB) to the Conduction band (CB) or vice versa in the direction of the electric field [15], so it is called dynamic nonlocal BTBT model. Both models show the right way to calibrate the experimental and full quantum simulation results.

In this work, extensive calibrations of different device structures with homo and heterojunctions using various materials are reported by using both Sentaurus and Silvaco TCAD Tools. The calibration results are compared to experimental and full quantum results available in the literature. The BTBT parameters for both simulators are given for the various TFET structures, which could facilitate the calibration process and expedite the TFET design utilizing different materials and structures.

## 2. Device structures and materials

Different TFET structures and materials are used in the following simulations. Fig. 1(a) shows a multi-gate TFET [18], which is used to allow TFET's implementation using standard FinFET processing techniques. Fig. 1(a) illustrates the actual 3D structure while Fig. 1(b) demonstrates the 2D representation used in the simulation. Fig. 1(c) shows a 3D Gate-all-around (GAA) silicon nanowire (NW) TFET [8] while Fig. 1(d) shows the 2D structure used for simulation where simulation is done by what is called cylindrical coordinates [16]. Further, Fig. 1(e) shows the third structure in which the source is formed of Ge instead of Silicon as a heterostructure to reduce the effective barrier height [6]. A hetero-dielectric-gate is also used in this structure with source overlap to confine tunneling inside Ge. Furthermore, Fig. 1(f) and (g) demonstrate the fourth structure used. The structure is a GAA TFET and the Silicon is wholly replaced by InAs material [19]. InAs is an III-V compound semiconductor that has a smaller bandgap than Silicon (having a bandgap of  $E_{g_{\text{InAs}}} = 0.37$  eV). Finally, Fig. 1(h) shows the last structure used in simulations. In this structure,  $\text{Mg}_2\text{Si}$  (having a bandgap of  $E_{g_{\text{Mg}_2\text{Si}}} = 0.77$  eV) is introduced as a new material for the source [20]. All the structures parameters and material properties used are summarized in Table 1.



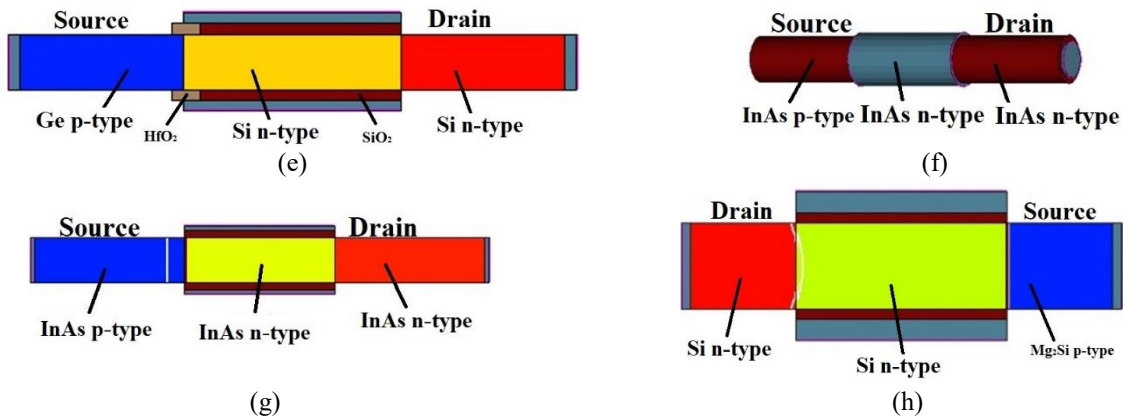


Figure 1. TFET structures used for calibration: (a) Multi-gate based Fin-FET, (b) 2D representation of multi-gate TFET, (c) GAA Si NW, (d) 2D representation of GAA Si NW, (e) Double gate Ge-source hetero-dielectric, (f) 3D representation of All InAs GAA, (g) 2D representation of All InAs GAA and (h) Double gate  $Mg_2Si$ -source.

Table 1. Parameters and material properties used in the simulations (lengths in nm and doping in  $cm^{-3}$ )

	Multi-gate Si	GAA Si NW	Ge source	$Mg_2Si$ -source	All InAs GAA	
					3D	2D
Channel length ( $L_g$ )	150	200	40	50	20	20
Drain length ( $L_d$ )	50	70	30	25	20	20
Source length ( $L_s$ )	50	70	30	25	20	20
Oxide thickness ( $t_{ox}$ )	2	4.5	2	2.5	1	1
Channel width ( $W$ )	40	70	10	20	$D = 6$	6
Dielectric constant ( $\kappa$ )	22	22	$\kappa_{SiO_2} = 3.9 / \kappa_{HfO_2} = 22$	22	12.7	12.7
Source doping ( $N_s$ )	$1 \times 10^{20}$	$1 \times 10^{19}$	$1 \times 10^{20}$	$1 \times 10^{20}$	$5 \times 10^{19}$	$5 \times 10^{19}$
Channel doping ( $N_c$ )	$1 \times 10^{15}$	$1 \times 10^{17}$	$1 \times 10^{16}$	$1 \times 10^{15}$	$1 \times 10^{15}$	$1 \times 10^{15}$
Drain doping ( $N_d$ )	$1 \times 10^{20}$	$1 \times 10^{19}$	$1 \times 10^{18}$	$1 \times 10^{20}$	$5 \times 10^{19}$	$5 \times 10^{19}$

### 3. Results and discussion

Firstly, the calibration is performed for a multi-gate TFET structure. Fig. 2 (a) shows the simulation results where the calibration is done vs experimental data available in [18]. To perform the calibration, the dynamic nonlocal BTBT model in Sentaurus is activated with the parameters' values for phonon-assisted of  $A_{path} = 2.2 \times 10^{17} cm^{-3}s^{-1}$  and  $B_{path} = 8.2 \times 10^6 Vcm^{-1}$  and for direct of  $A_{path} = 4.8 \times 10^{17} cm^{-3}s^{-1}$  and  $B_{path} = 6.45 \times 10^6 Vcm^{-1}$  [21]. For the low voltage values of  $V_{GS}$ , the Hurkx Trap-assisted Tunneling (TAT) model is used. The result in [18] is divided by  $25 \times 10^{-3}$  to account for the third gate. Regarding Silvaco TCAD, the effective tunneling masses of the nonlocal BTBT model are tuned to get the best fit. Electron and hole effective masses are found to be 0.11 and 0.17, respectively. These effective masses values are compatible with those found in the literature for a similar double gate n-type TFET structure [22-24]. The BTBT parameters for both Sentaurus and Silvaco are found to be used in all simulations concerning Silicon material. So, the same parameters will be used for the next case study which involves Silicon material.

Further, Fig. 2 (b) shows both experimental and simulation results of the Gate-all-around Silicon nanowire TFET structure [8]. To calibrate this structure in Sentaurus, the same model of multi-gate TFET is used. Also, Silvaco tunneling masses used in the previous structure are applied as stated above. To calibrate the OFF current when using Silvaco, the SRH (Shockley Read Hall) recombination and TAT (Trap Assisted Tunneling) models should be incorporated as the BTBT model

is not suitable to fit this region because the tunneling width is increased and thermionic current dominates. To get the best fit, the adjusted values of the lifetimes are found to be  $\tau_{n0} = \tau_{p0} = 5$  ns [25]. The TAT model used is the default model of Silvaco. Regarding Sentaurus, Scharfetter relation [15] is enabled for recombination with  $\tau_{\min} = 0$  for both electron and holes and  $\tau_{\max} = 1 \times 10^{-5}$  s for electron and  $\tau_{\max} = 3 \times 10^{-6}$  s for holes, for TAT models, Electron and hole effective masses are found to be 0.11 and 0.17, respectively.

Furthermore, Fig. 2 (c) shows the simulation results of Ge-source hetero-dielectric TFET [6]. As can be seen from the results, the ON current has improved with a decline in the OFF current compared to silicon TFET. To calibrate the full quantum simulation results, the direct BTBT model is used with  $A_{\text{path}} = 1.465 \times 10^{20} \text{ cm}^{-3} \text{ s}^{-1}$  and  $B_{\text{path}} = 6.03 \times 10^6 \text{ Vcm}^{-1}$  [6] and the phonon-assisted model is used with  $A_{\text{path}} = 4 \times 10^{14} \text{ cm}^{-3} \text{ s}^{-1}$  and  $B_{\text{path}} = 1.9 \times 10^7 \text{ Vcm}^{-1}$ . Regarding Silvaco, the electron and hole tunneling masses are adjusted as 0.12 and 0.18, respectively. It should be pointed out here that the adjustment of the tunneling masses is straightforward and needs little effort to reach the best fit. This is also valid for all materials, as will be shown hereafter.

Moreover, Fig. 2 (d) and (e) shows the calibration results of all InAs GAA TFET. The results show an improvement in ON current compared to silicon TFET while the OFF current is degraded. The data used in calibration is based on a full quantum simulator. However, this simulator proved to be compatible with measurements [19, 26, 27]. To calibrate the results in Sentaurus, the pre-factor value is found to be  $A_{\text{path}} = 2 \times 10^{20}$  and the exponential factor  $B_{\text{path}} = 2.24 \times 10^6 \text{ Vcm}^{-1}$  as mentioned in [28]. The simulation shown in Fig. 2 (d) is done also with the same parameters in 3D using Sentaurus.

Regarding Silvaco TCAD, the simulation is done for the 2D case only as the BTBT model used in Silvaco is not enabled in 3D structures, which is a disadvantage of this simulator. Silvaco nonlocal BTBT model is only constrained to modeling 1D and 2D TFET geometries. It can be used to model a 3D TFET structure if the structure is cylindrical and can be divided into two symmetric parts. In this regard, half the device is considered and the meshing option of cylindrical is enabled as done in the case of GAA. Silvaco's fitting parameters of electron and hole tunneling masses are adjusted to 0.15 and 0.18, respectively, to get the best fit.

Finally, Fig. 2 (f) shows the simulation results of  $\text{Mg}_2\text{Si}$ -source TFET. Like Ge-source TFET, the  $\text{Mg}_2\text{Si}$ -source TFET shows an enhancement in ON current, and the OFF current is reduced compared to all-silicon TFET. Comparing  $\text{Mg}_2\text{Si}$ -source TFET with Ge-source TFET, the  $\text{Mg}_2\text{Si}$ -source TFET shows better ON current. As there is no experimental or full quantum data are available for this new material, we used the same effective masses used in Silicon for Silvaco simulation while for Sentaurus simulation the parameters' values for phonon-assisted are adjusted to  $A_{\text{path}} = 9 \times 10^{17} \text{ cm}^{-3} \text{ s}^{-1}$  and  $B_{\text{path}} = 1.9 \times 10^7 \text{ Vcm}^{-1}$  and for direct of  $A_{\text{path}} = 2 \times 10^{21} \text{ cm}^{-3} \text{ s}^{-1}$  and  $B_{\text{path}} = 2.06 \times 10^7 \text{ Vcm}^{-1}$ . These results are compatible with the first published work for a TFET regarding this material [29].

Table 2. Calibrated parameters for Sentaurus and Silvaco Simulators ( $A_{\text{path}}$  and  $B_{\text{path}}$  are in units of  $\text{cm}^{-3} \text{ s}^{-1}$  and  $\text{Vcm}^{-1}$ , respectively)

TFET Structure	Sentaurus Parameters				Silvaco Parameters	
	Phonon-assisted		Direct		$m_e$	$m_h$
	$A_{\text{path}}$	$B_{\text{path}}$	$A_{\text{path}}$	$B_{\text{path}}$		
Multi-gate Si	$2.2 \times 10^{17}$	$8.2 \times 10^6$	$4.8 \times 10^{17}$	$6.45 \times 10^6$	0.11	0.17
GAA Si NW	$2.2 \times 10^{17}$	$8.2 \times 10^6$	$4.8 \times 10^{17}$	$6.45 \times 10^6$	0.11	0.17
Ge-source hetero-dielectric	$4 \times 10^{14}$	$1.9 \times 10^7$	$1.465 \times 10^{20}$	$6.03 \times 10^6$	0.12	0.18
All InAs GAA	$2 \times 10^{20}$	$2.24 \times 10^6$	$2 \times 10^{20}$	$2.24 \times 10^6$	0.15	0.18
$\text{Mg}_2\text{Si}$ -source	$9 \times 10^{17}$	$1.9 \times 10^7$	$2 \times 10^{21}$	$2.06 \times 10^7$	0.11	0.17

Table 2 summarizes the calibrated parameters used in the nonlocal BTBT models of both Sentaurus and Silvaco simulators. As can be depicted from the previous simulations and the reported values given in Table 2, we can highlight the following. Although Sentaurus provides a wide range of parameters to be tuned when calibrating its dynamic BTBT model, which could be an advantage, it

may lead to different parameters used from research to another. Meanwhile, Silvaco limits the calibration of the nonlocal BTBT model only on two parameters, which are easier to be fitted even manually.

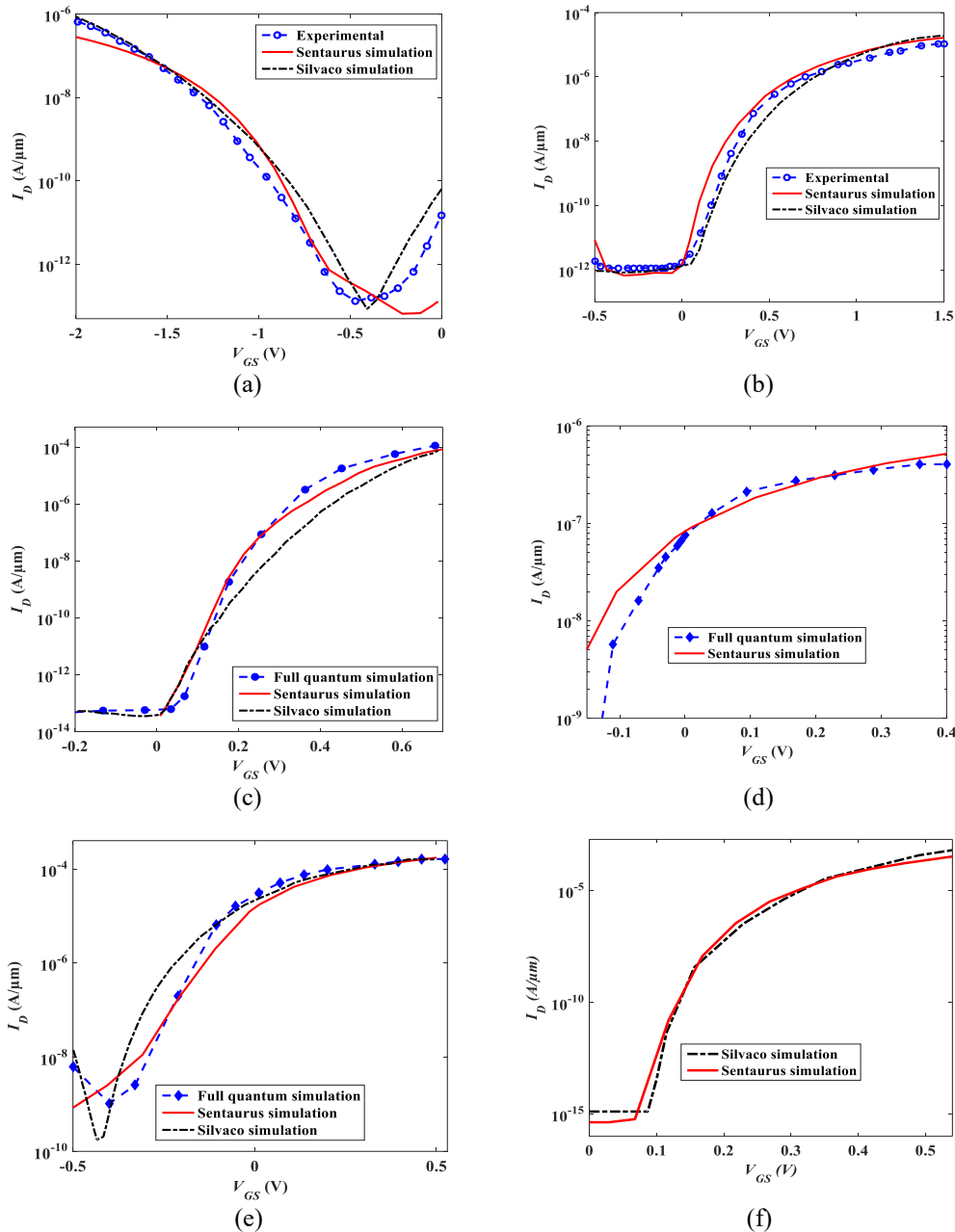


Figure 2. Calibration of (a) multi-gate Silicon TFET. (b) Gate-all-around Silicon nanowire TFET. (c) Ge-source hetero-dielectric TFET. (d) All InAs GAA TFET (3D case) (e) All InAs GAA TFET (2D case) (f) Simulation results of Mg<sub>2</sub>Si-source TFET.

#### 4. Conclusion

In this work, a brief flow of TFET calibration using Sentaurus and Silvaco TCAD tools is presented. The calibration is done using experimental and full quantum data. Different structures including multi-gate Silicon, Gate-All-Around Si nanowire, Ge-source, Mg<sub>2</sub>Si-source, and all InAs TFETs are used in this calibration study to find the BTBT parameters, for both Sentaurus and Silvaco simulators, that

best fit the data. The simulation results could provide a good source in investigating numerous TFET structures with different materials either for Sentaurus or Silvaco TCAD environments.

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