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Modeling of high-current polycrystalline silicon thin film transistors by incorporating buried electrode

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Abstract

For display applications, high current and large on/off current ratio are pursued for driving and switching transistors. In this article, a thin film transistor (TFT) device incorporating a buried electrode is proposed, which enables to increase the driving current due to the reduction of the channel length, with the channel length only at the drain side. This lateral short channel TFT enables to increase the on-current when maintaining the field

effect mobility, in comparison to our experimental short-channel vertical TFT structure. Another advantage of the proposed structure lies in the suppression of the Schottky barrier at the source and drain contacts when using high-work-function source/drain contacts for an *N-type* TFT, with an increased on/off current ratio reaching approximately 10^6 . The suppression of Schottky barrier at source/drain has been verified by the contact resistance measurements. Even though high driving current is obtained, the off-current is still high due to the weakened electric field at source/drain sides and needs to be further optimized.

Key words: polycrystalline silicon, thin film transistor, buried electrode, short channel TFT, Schottky barrier

1. Introduction

Polycrystalline silicon has been widely used in solar cells [1] and low-cost logic circuits [2], mainly due to its larger intrinsic mobility with large grain boundaries morphology, its ease of doping, and its simple process compatible with CMOS technology. For building up logic circuits, the thin film transistors (TFTs) that make use of polycrystalline silicon layers have been widely studied, where they have also been used in radio-frequency identification (RFID) tags [3], in random access memories [4]. In addition, the intrinsic mobility of polycrystalline silicon enables reasonable drain

current-especially for driving all kinds of displays, such as electrophoretic display (EPD) [5], active-matrix liquid crystal display (AMLCD) [6], and active-matrix organic light-emitting diode display (AMOLED) [7]. However, for high-resolution displays, especially for high-resolution AMOLED, the drain current requires further increasement, and the power consumption should be lowered as well.

For polycrystalline silicon TFTs, the device normally works in linear regime, and the drain current can be expressed as a first approximation by the following formula:

$$I_{ds} = \frac{W}{L} C_{ox} \mu_{FE} [(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2] \quad (1)$$

Where W/L is channel width/length ratio, C_{ox} is the gate dielectric capacitance per unit area, μ_{FE} is the field effect mobility, V_{gs} and V_{ds} are gate-source voltage and drain-source voltage, respectively, and V_{th} is the threshold voltage. In most cases, the main approaches of increasing the drain current focus on the improvement of the field effect mobility, and in industry, the excimer laser annealing (ELA) procedure is widely adopted to enlarge the polycrystalline silicon grain size and thus improve the field effect mobility, however, the production cost is high, and the uniformity between pixel units cannot be guaranteed [8]. In another approach, the channel length can be shortened to strengthen the electric field between source and drain, adopting a vertical configuration that requires better control of the channel length by adopting relatively high film thickness, in

order to suppress the short channel effects, which increases the production cost [9]. Other methods, such as increasing the surface capacitance of the gate dielectric by adopting low equivalent oxide thickness (EOT) can be proposed, but it may lead to larger gate leakage or higher hysteresis [10].

In order to appropriately shorten the channel length, a polycrystalline silicon TFT structure is proposed with a buried electrode. Figure 1 shows a schematic representation of such a device, the source, drain, buried electrode, and gate are indicated, with a source-buried electrode distance of $L1$, and a drain-buried electrode distance of $L2$. On one hand, the buried electrode enables higher electric field in the semiconducting active layer between buried electrode and the source/drain electrode. On the other hand, the optimization of the buried electrode position relative to the source/drain contact $L1/L2$ can suppress the short channel effect. In addition, the introduction of the buried electrode can suppress the parasitic resistance at the source/drain contact due to energy level misalignment at source(drain)/semiconducting active layer interface. Therefore, the drain current and I_{on}/I_{off} ratio can further increase, which are the main objectives for driving high-resolution displays.

2. Configuration of simulated devices

Polycrystalline silicon TFTs with bottom gate, top contact configuration were studied. Initially, aluminum layer was employed as the

gate electrode, then a 100 nm silicon oxide layer acts as the gate dielectric layer. Thereafter, for the conventional TFT, a 50 nm thick *N-type* lightly-doped (10^{17} cm^{-3}) polycrystalline silicon layer works as the active layer and the device is accomplished by patterning deposited aluminum layer to form source and drain contact pads. In contrast, for the proposed TFT, a 10 nm thick aluminum layer is designed prior to the polycrystalline silicon active layer deposition to form buried electrode. The structure configurations of the conventional and proposed TFTs are shown in figure 2(a) and 2(b), respectively. The bottom gate layer is at the top of the simulated structure. Source and drain contacts are simplified in this simulation. For the conventional TFT, the channel width is 1 μm by default in this 2D simulation, and channel length is defined as 16 μm . For the TFT with buried electrode, the position of the buried electrode is at the middle between source and drain, with different lengths of the buried electrode. Note that, for this bottom-gate, top contact configuration, the alignment of the buried electrode is not necessary, therefore, the patterning of the buried electrode can be achieved by low-cost shadow masks without photolithography step. In addition, the buried electrode can adopt low-cost metal, such as aluminum. Therefore, the total cost of device fabrication for the TFT device with buried electrode is comparable to the conventional TFT. The simulations are based on the Silvaco TCAD tool.

3. Results and Discussion

The simulation parameters were listed in table I. The transfer characteristics of conventional TFT and proposed TFT with buried electrode are shown in figure 3(a), the drain voltage is fixed at 5 V, and the gate voltage scans from -20V to 20V. Note that, the oxide capacitance per unit area is used to calculate the mobility, and the introduction of buried electrode only affects the total oxide capacitance that is related to the oxide layer area, while it does not affect the areal capacitance that is used to calculate the mobility. For the polycrystalline silicon active layer, the density of states (DOS) incorporating tail states and the Gaussian distributions can be expressed as [11]:

$$g_{TA}(E) = 1.12 \times 10^{21} \exp\left(\frac{E - E_c}{0.025}\right) \quad (2)$$

$$g_{TD}(E) = 4 \times 10^{20} \exp\left(\frac{E_V - E}{0.05}\right) \quad (3)$$

$$g_{GA}(E) = 5 \times 10^{17} \exp\left[-\left(\frac{0.4 - E}{0.1}\right)^2\right] \quad (4)$$

$$g_{GD}(E) = 1.5 \times 10^{18} \exp\left[-\left(\frac{E - 0.4}{0.1}\right)^2\right] \quad (5)$$

From the transfer characteristics, the conventional TFT shows an off-current of 9.3×10^{-13} A and an on-current of 6.3×10^{-6} A, indicating a current ratio I_{on}/I_{off} of 6.8×10^6 . In contrast, the proposed TFT with a buried electrode length of 10 μm shows an off-current of 1.6×10^{-12} A and an on-current of 3.9×10^{-5} A, indicating a current ratio of 2.4×10^7 . The proposed

structure with buried electrode shows an on/off current ratio of 3.5 times higher than the conventional TFT. Note that, the on-current of the proposed TFT is 6.2 times higher than the conventional TFT, indicating its stronger driving capability. From the transfer curves, the same threshold voltage of 9.5 V can be obtained due to the same trap density of states for both of the two TFTs, and for the conventional TFT, the field effect mobility is approximately $55 \text{ cm}^2/\text{V}\cdot\text{s}$, which is consistent with the experimentally fabricated lateral TFT in our group using solid-phase crystallization method [12]. In contrast, the field effect mobility for the proposed TFT with buried electrode needs to be evaluated, considering the exact value of the channel length is unknown. The other electrical parameters are also listed in table II, while the same subthreshold slope of the two types of TFTs also indicates the same trap density. All the electrical parameters are deduced from the transfer curves as expressed by formula 1.

In addition, the TFT with buried electrode can also be compared with double-gate TFT. Figure 3(b) and 3(c) show the structure configuration of the double-gate TFT, and the transfer characteristics of different devices. It shows that when the negative bias of -20V is applied on the second gate, the larger threshold voltage and the lower off-current are obtained. In contrast, when the positive bias of 20V is applied on the second gate, the off-current is greatly increased due to creation of conduction channel under the second gate positive bias resulting that the on-off current ratio reduces

to be only approximately 10, while the threshold voltage reduces. Note that, even though the on-current increases when the positive bias is applied on the second gate bias, the on-current of the double-gate TFT is still smaller than the TFT with buried electrode, indicating the advantage of our proposed TFT configuration in terms of the large on-current and the small off-current.

In order to evaluate the precise channel length of the TFT configuration with buried electrode, the electrical field in the active layers for three different structures are demonstrated in figure 4(a), 4(b), and 4(c), while the corresponding transfer characteristics plotted at $V_{ds} = 5V$ are demonstrated in figure 4(d) for the three structures. As shown in figure 4(a) and figure 4(d), when the buried electrode totally overlaps with the drain contact, the drain and source are short-circuited. This may be due to that, the electrical field at source is negative, and the current flow needs that the electrical field at buried electrode is larger than the source, which is natural, and for the overlapping between buried electrode and drain, the short distance between the two electrodes forms short circuit. In contrast, as shown in figure 4(b), the current flow needs that the electric field at buried electrode is smaller than the drain, therefore, due to the negative electric field at drain, the gate bias should be large to obtain lower electrical field at the buried electrode than the drain electric field, thus, the gate modulation of the current is obtained, as shown in figure 4(d). It is therefore

concluded that only the channel length at the drain side is the actual channel length. In addition, as shown in figure 4(c) and 4(d), when the buried electrode left edge is moved far from the source contact while keeping the same distance between the buried electrode right edge and the drain contact, the electrical characteristics still maintain the same, indicating the function part of only drain side. From this point of view, the actual channel length of the proposed configuration with the buried electrode is only the distance between the buried electrode and the drain contact. Therefore, considering the channel length is approximately 3 μm , the field effect mobility of the proposed structure in figure 2(b) is approximately 63.8 $\text{cm}^2/\text{V}\cdot\text{s}$, which is similar to the conventional structure with a field effect mobility of 55 $\text{cm}^2/\text{V}\cdot\text{s}$.

In order to further study the effect of the buried electrode length on the electrical characteristics, different buried electrode lengths of 12 μm , 10 μm , 6 μm , and 1 μm are adopted, with channel lengths being approximately 2 μm , 3 μm , 5 μm , and 7.5 μm , respectively. The corresponding transfer characteristics are shown in figure 4(e). From the transfer characteristics plotted at $V_{\text{ds}} = 5\text{V}$, the on-current is reversely proportional to the channel length, while the off-current is also reversely proportional to the channel length when the channel length is above 3 μm . However, when the channel length further reduces to 2 μm , the off-current abruptly increases, due to short channel effects at a high drain-source voltage of 5 V. In an

experimental demonstration based on the short-channel polycrystalline silicon vertical TFT ($W/L=20\ \mu\text{m}/1.2\ \mu\text{m}$) and the long-channel polycrystalline silicon lateral TFT ($W/L=40\ \mu\text{m}/20\ \mu\text{m}$), as shown in figure 4(f), when the drain-source voltage V_{ds} is 1V, the on-current is approximately 2.5 times higher for the vertical TFT. Accordingly, the off-current should also be only 2.5 times higher for the vertical TFT when there are no short channel effects. However, the off-current of the vertical TFT is two orders of magnitude higher than its lateral counterpart, verifying the short channel effects that takes place when the channel length L is below $3\ \mu\text{m}$ for a drain-source voltage of 1 V. In addition, when considering the relationship between on-current and channel width/length ratio, the field effect mobility of experimental vertical TFT is much smaller than the experimental lateral TFT, which may be due to the high-thickness rough sidewall for the active layer deposition, and vertical growth kinetics for the polycrystalline silicon active layer may be different from the lateral growth of the polycrystalline silicon active layer for the lateral TFT [9]. In theory, this lateral short-channel TFT can maintain the high field effect mobility by well controlling the buried electrode thickness and morphology, which shows its advantage for this proposed short-channel lateral TFT with buried electrode.

In addition to the high driving current due to the short channel length, another advantage of this buried electrode is the ease of choosing different

source/drain contact materials. This is important especially for the *N-type* TFT, as low-work-function metals are usually needed for source and drain contacts, which degrade electrical characteristics [13]. Therefore, by aid of the buried electrode, its high electrical field enables to suppress the Schottky barrier introduced by high-work-function contacts. Note that, a source-gated transistor (SGT) had been proposed [14, 15] previously by introducing asymmetric source Schottky contact and drain Ohmic contact, while the overlapping between gate and source contact enables the gate modulation of the source Schottky barrier height. However, due to the limited gate modulation strength of the Schottky barrier height even with high gate bias, the high Schottky barrier height limits the carrier injection thus results in lower current density. In contrast, with the aid of the buried electrode, the Schottky barrier height can be totally eliminated by the high electric field. In order to prove this, the *N-type* polycrystalline silicon TFT devices with copper source and drain contacts are studied, with a high work function of 4.7 eV that forms Schottky barriers with *N-type* polycrystalline silicon at source/drain. From the transfer characteristics shown in figure 5, for the conventional device without buried electrode, due to the gate overlapping with source and drain contacts, the device shows SGT-like property, with an off-current of approximately 10^{-11} A, while the on-current is in the order of only 10^{-8} A, giving a current ratio of only approximately 10^3 . In contrast, when introducing the buried electrode, on-current has been

increased to approximately $3.4 \times 10^{-5} \text{ A}$, which is very similar to the proposed structure with buried electrode and low-work-function (4.2 eV) aluminum source and drain contacts, indicating the suppression of the Schottky barrier with the high electric field. In fact, in order to prove the suppression of the Schottky barrier, the device based on lutetium (low work function of 3.84 eV) source and drain contacts are also studied, with source and drain being Ohmic contact, and the similar on-current is obtained, further proving the suppression of the Schottky barrier.

The Schottky barrier height can also be verified by the contact resistance. The contact resistance R_{contact} can be calculated by the following formula:

$$R_{\text{total}} = \frac{V_{ds}}{I_{ds}} = R_{\text{contact}} + \frac{L}{WC_{ox}\mu_{FE}} \cdot \frac{1}{V_{gs} - V_{th}} \quad (6)$$

As shown in figure 6(a) and 6(b), the simple model shows a high contact resistance of approximately $10^7 \Omega$ for the device without buried electrode, while for the device with buried electrode, the contact resistance is in the order of $10^3 \Omega$, the contact resistance has been greatly reduced by the buried electrode.

In order to further evaluate the contact resistance by involving the spreading resistance, the contact resistances are also evaluated by transmission line method (TLM) [16]. As shown in figure 6(c) and 6(d), for the device without buried electrode, the contact resistance is more than $10^7 \Omega$. In contrast, for the device with buried electrode, the contact

resistance can be negligible. Therefore, by introducing buried electrode, the Schottky barrier has been suppressed also calculating from TLM method. Note that, the gate bias is set to be more than 8V, and the extracted contact resistance corresponds to a large negative value when the gate bias is below 8V, which may be due to the short-channel effect with a high drain-source voltage of 5V.

Note that, for the high work function electrode devices, even though the on-current has been improved by the buried electrode, the off-current has also increased. As shown from figure 3 and figure 5, for the device with buried electrode as well as aluminum source and drain, the off-current is in the order of 10^{-12} A, while the off-current is in the order of 10^{-11} A for the device with copper source and drain contacts, and the off-current is approximately 10^{-10} A for the device with buried electrode and copper source and drain contacts. This anomalous phenomenon can be explained by analyzing the electric field distribution in the active layer. As shown in figure 7(a), for the device with aluminum source and drain, the electric field from the buried electrode at the drain side conflicts with the electric field from the drain contact, thus the off-current is lower. In contrast, for the device with copper source and drain, due to the Schottky barrier, the electric field from the source and drain contacts is consistent with the electric field from the gate (figure 7(b)) or the electric field from the buried electrode (figure 7(c)), thus the off-currents are higher, especially for the

device with buried electrode. Note that, for the source and drain Schottky barrier, the strong electric field from the buried electrode points from source to drain, which lifts the potential at the source side and reduces the potential at the drain side, thus counteracting with the original electric fields at source and drain contacts, and the total electric fields at source and drain are weakened. Therefore, the Schottky barriers at source and drain contacts are suppressed, and thus the off-current increases.

It is worthy of mentioning that, high electric field is observed near the buried electrode, which may influence the reliability of the fabricated devices. To control the value of the electric field in this region, the solutions could be i) an adjusted doping concentration of the active layer especially in the upper part of the silicon layer in contact with the buried electrode, and/or ii) the choice of the conductive material of the buried electrode. The different crystallization methods can also further increase the driving current and the breakdown voltage.

Conclusion

The polycrystalline silicon TFT with buried electrode enables a higher driving current due to the reduced channel length, while the actual channel is formed only at the drain side, and this short-channel lateral TFT with buried electrode can maintain the field effect mobility in comparison to the conventional long-channel lateral TFT. In addition, another advantage of

the TFT with buried electrode lies in the suppression of the source and drain Schottky barriers and thus it supports much higher driving current, which enables the usage of the high-work-function source and drain contacts for *N-type* TFT. However, the off-current of the TFT with Schottky source and drain contact increases, and further work will be on the reduction of the off-current for the device with buried electrode and Schottky source/drain.

Data Availability Statements

The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

Statements & Declarations

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Conflict of Interest Statement

On behalf of all authors, the corresponding author states that there is no conflict of interest.

References:

- [1] G. Beaucarne, S. Bourdais, A. Slaoui, J. Poortmans, Thin-film polysilicon solar cells on foreign substrates using direct thermal CVD: material and solar cell design. *Thin Solid Films*. 403-404, 229 (2002).
- [2] C. Wei, W. Mingxiang, Z. Yan, W. Man, Degradation of Polycrystalline Silicon TFT CMOS Inverters under AC Operation. *IEEE T. Electron. Dev.* 60, 295 (2013).
- [3] Y. Yueh-Hua, L. Yuan-Jiang, L. Yu-Hsuan, K. Chung-Hung, L. Chun-Huai, H. YaoJen, Emery C. Yi-Jan, An LTPS TFT Demodulator for RFID Tags Embeddable on Panel Displays. *IEEE T. Microw. Theory.* 57, 1356 (2009).
- [4] H. Jin-Woo, R. Seong-Wan, K. Dong-Hyun, C. Yang-Kyu, Polysilicon Channel TFT With Separated Double-Gate for Unified RAM (URAM)—Unified Function for Nonvolatile SONOS Flash and High-Speed Capacitorless 1T-DRAM. *IEEE T. Electron. Dev.* 57, 601 (2010).
- [5] S. Inoue, K. Sadao, T. Ozawa, Y. Kobashi, H. Kawai, T. Kitagawa, T. Shimoda, in *IEEE International Electron Devices Meeting* (2000), p.197.
- [6] S. Inoue, S. Utsunomiya, T. Saeki, T. Shimoda, Surface-free technology by laser annealing (SUFTLA) and its application to poly-Si TFT-LCDs on plastic film with integrated drivers. *IEEE Trans. Electron. Dev.* 49, 1353 (2002).

- [7] P. Kee Chan, J. Jae-Hong, K. YoungIl, C. Jae Beom, C. Young-Jin, Z. Zhi Feng, K. ChiWoo, A poly-Si AMOLED display with high uniformity. *Solid. State. Electron.* 52, 1691 (2008).
- [8] H. Akito, T. Fumiyo, T. Michiko, S. Katsuyuki, Y. Kenichi, C. Mitsuru, S. Yasuyuki, S. Nobuo, High-Performance Polycrystalline Silicon Thin Film Transistors on Non-Alkali Glass Produced Using Continuous Wave Laser Lateral Crystallization. *Jpn. J. Appl. Phys.* 41, L311 (2002).
- [9] P. Zhang, E. Jacques, R. Rogel, O. Bonnaud, P-type and N-type multi-gate polycrystalline silicon vertical thin film transistors based on low-temperature technology. *Solid. State. Electron.* 86, 1 (2013).
- [10] N. Kai, S. Atanu, C. Wriddhi, Y. Huacheng, G. Benjamin, S. Jeffrey, G. Bruce Rayner, G. Sumeet, D. Suman, in *IEEE International Electron Devices Meeting* (2019), p. 7.4.1.
- [11] Silvaco, Atlas user's manual (2000), p.218.
- [12] L. Pichon, K. Mourgues, F. Raoult, T. Mohammed-Brahim, K. Kission, D. Briand, O. Bonnaud, Thin film transistors fabricated by in situ doped unhydrogenated polysilicon films obtained by solid phase crystallization, *Semicond. Sci. and Tech.* 16, 918 (2001).
- [13] L. Ting, S. Lei-Lai, Z. Yu-Qing, P. Gregory, F. Guanhua, Z. Chenxin, L. Sicheng, B. Ray, W. H.-S. Philip, H. Tsung-Ching, C. Kwang-Ting, B. Zhenan, Low-voltage high-performance flexible digital and analog circuits based on ultrahigh-purity semiconducting carbon nanotubes. *Nat.*

Commun. 10, 2161 (2019).

[14] A. S. Radu, T. Michael, Y. Nigel, M. S. John, P. Silva S. Ravi, Temperature Effects in Complementary Inverters Made with Polysilicon Source-Gated Transistors. *IEEE Trans. Electron. Dev.* 62, 1498 (2015).

[15] M. S. John, Alexandru S. Radu, G. Stamatis, S. Maxim, P. Silva S. Ravi. Low-Field Behavior of Source-Gated Transistors. *IEEE Trans. Electron. Dev.* 60, 2444 (2013).

[16] T. Abbas, L. Slewa, *Int. J. Nanoelectron. M.*, Transmission line method (TLM) measurement of (metal/ZnS) contact resistance. *Int. J. Nanoelectronics and Materials.* 8, 111 (2015).

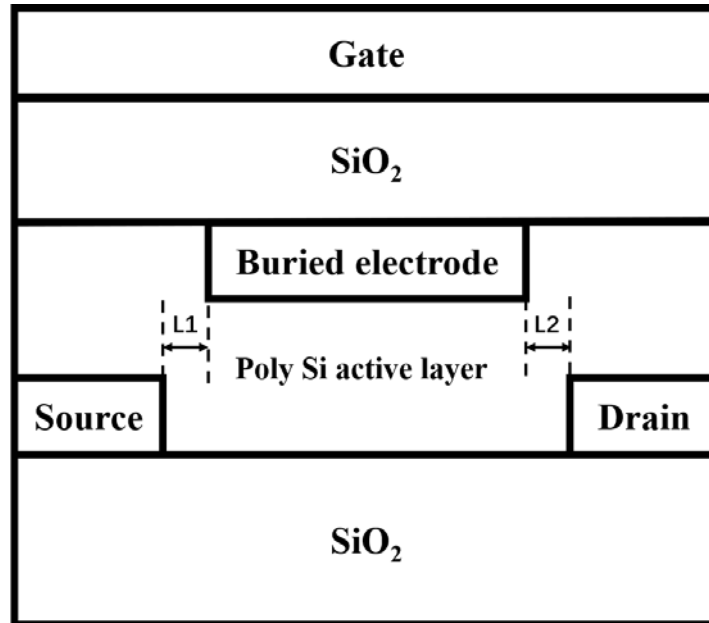


Figure 1: Schematic representation of the novel TFT. The source and drain contacts, the gate contact and the buried contact are demonstrated, with source-buried electrode distance of $L1$, and drain-buried electrode distance of $L2$. The buried electrode creates new electrical behavior.

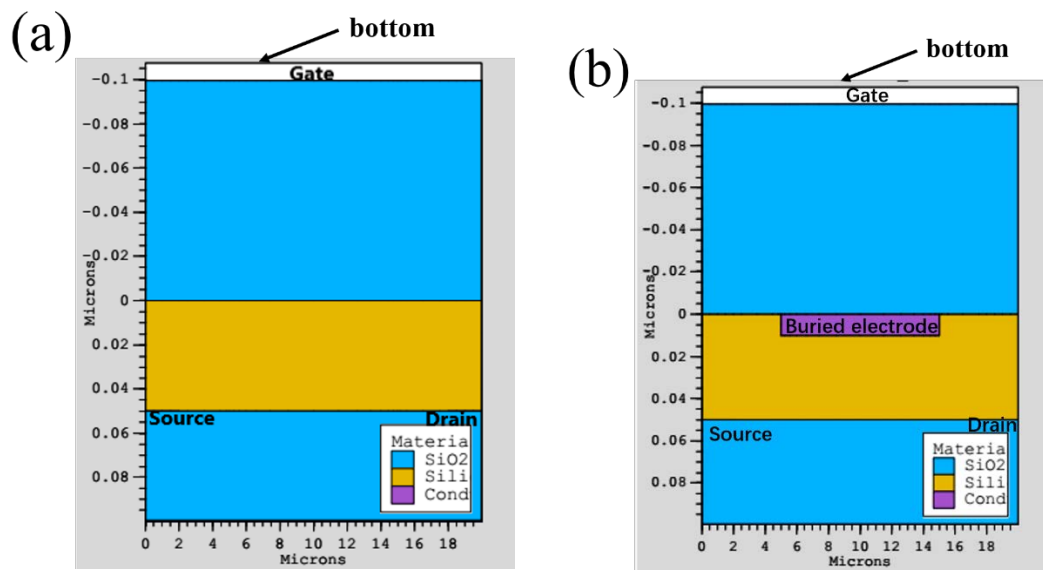


Figure 2: (a) configuration of the simulated conventional polycrystalline silicon TFT without buried electrode, (b) configuration of the simulated polycrystalline silicon TFT with buried electrode.

Table I: physical parameters for the simulations

Type	Conventional TFT	TFT with buried electrode
channel width W	1 μm	1 μm
Source/drain extending length	2 μm	2 μm
Channel length L	16 μm	3 μm for 10 μm buried electrode
Oxide thickness t_{ox}	100 nm	100 nm
active layer electron concentration n	10^{17} cm^{-3}	10^{17} cm^{-3}
drain bias v_{ds}	5 V	5 V
gate bias v_{gs}	-20V – 20V	-20V – 20V
conduction band edge intercept densities NTA	$1.12 \times 10^{21} \text{ cm}^{-3}/\text{eV}$	$1.12 \times 10^{21} \text{ cm}^{-3}/\text{eV}$
valence band edge intercept densities NTD	$4 \times 10^{20} \text{ cm}^{-3}/\text{eV}$	$4 \times 10^{20} \text{ cm}^{-3}/\text{eV}$
characteristic decay energy WTA	0.025 eV	0.025 eV
characteristic decay energy WTD	0.05 eV	0.05 eV
Total density of states NGA	$5 \times 10^{17} \text{ cm}^{-3}/\text{eV}$	$5 \times 10^{17} \text{ cm}^{-3}/\text{eV}$
Total density of states NGD	$1.5 \times 10^{18} \text{ cm}^{-3}/\text{eV}$	$1.5 \times 10^{18} \text{ cm}^{-3}/\text{eV}$
characteristic decay energy WGA	0.1 eV	0.1 eV
characteristic decay energy WGD	0.1 eV	0.1 eV
Peak energy distribution EGA	0.4 eV	0.4 eV
Peak energy distribution EGD	0.4 eV	0.4 eV

Table II: Electrical parameters of conventional TFT and proposed TFT with buried electrode.

TFT types	Threshold Voltage (V)	mobility (cm²/V•s)	Transconductance (μS)	Subthreshold slope (V/dec)
Conventional TFT	9.5	55	59.3	1.2
Proposed TFT	9.5	63.8	367	1.2

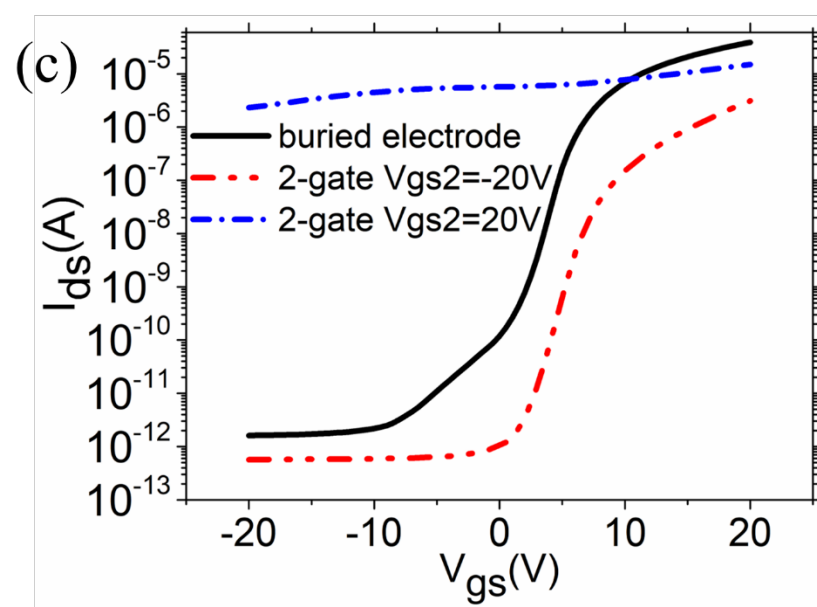
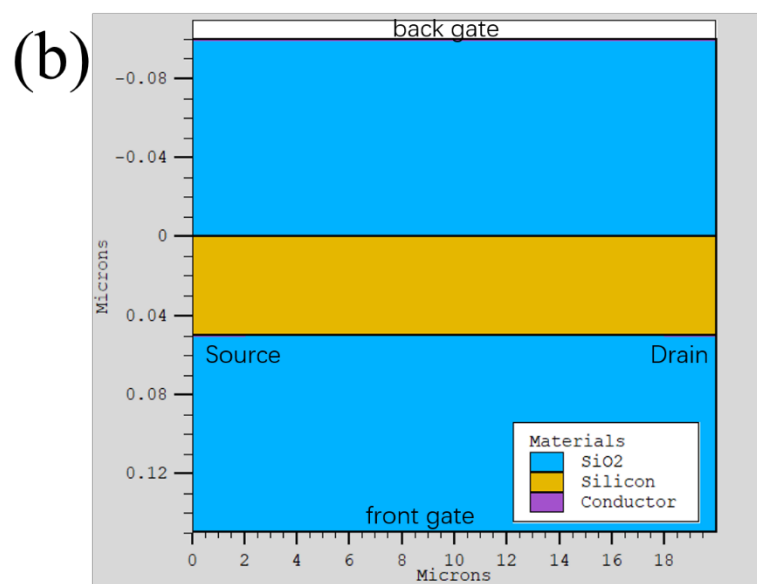
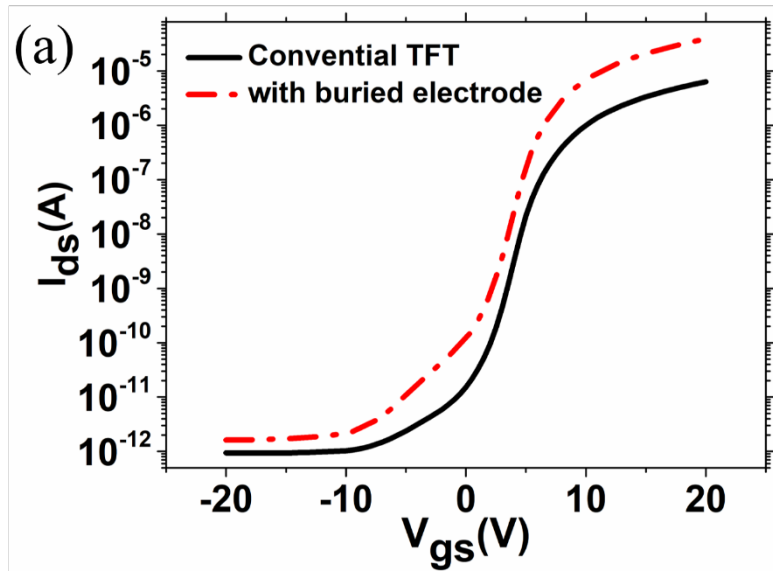
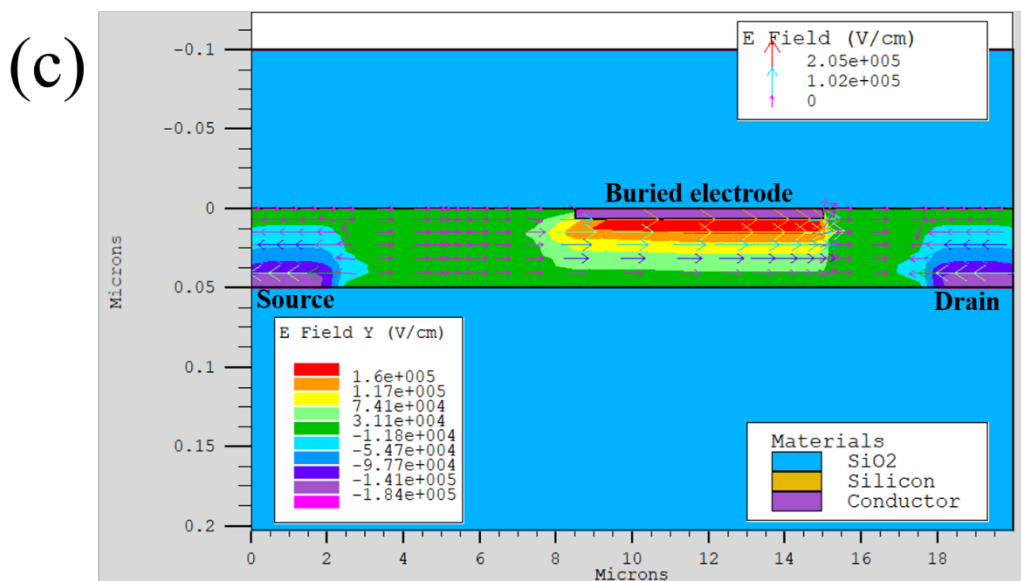
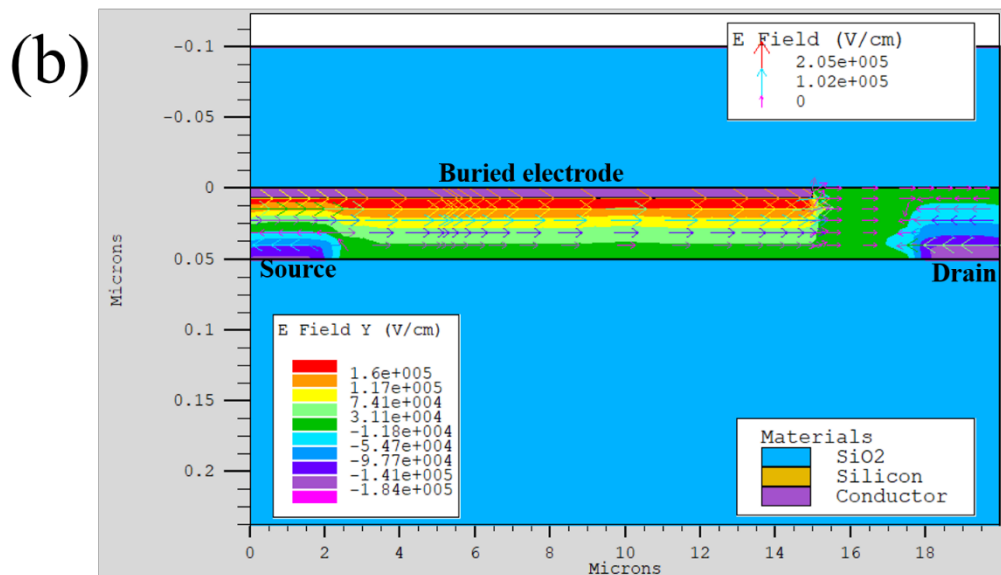
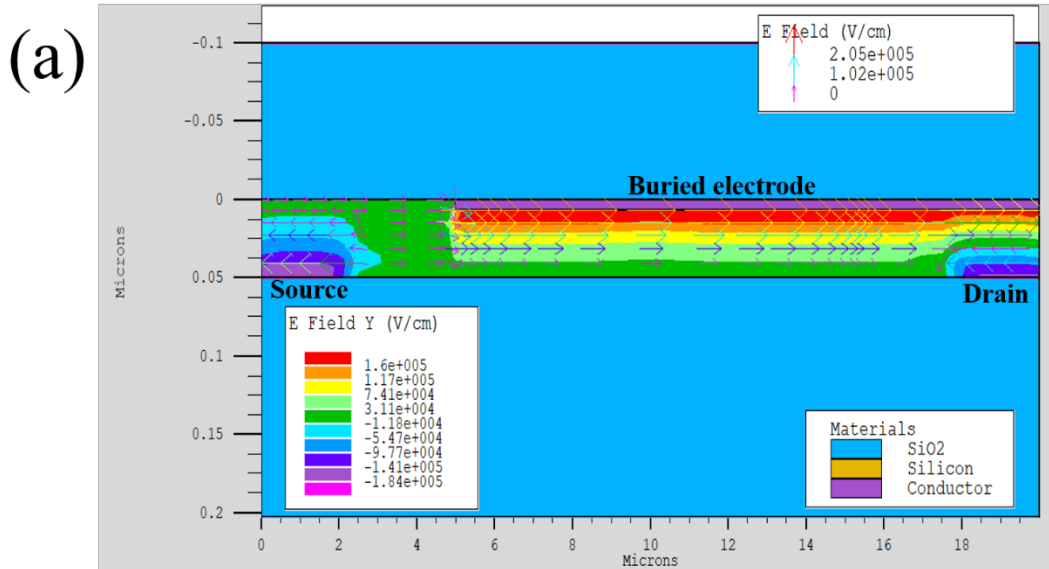


Figure 3: (a) transfer characteristics of the conventional TFT and proposed TFT with buried electrode when $V_{ds} = 5V$. Under this condition, the on-state current I_{on} is approximately 6.2 times higher, (b) the structure configuration of the double-gate TFT, (c) the transfer characteristics comparison between the proposed TFT with buried electrode and the double-gate TFT.



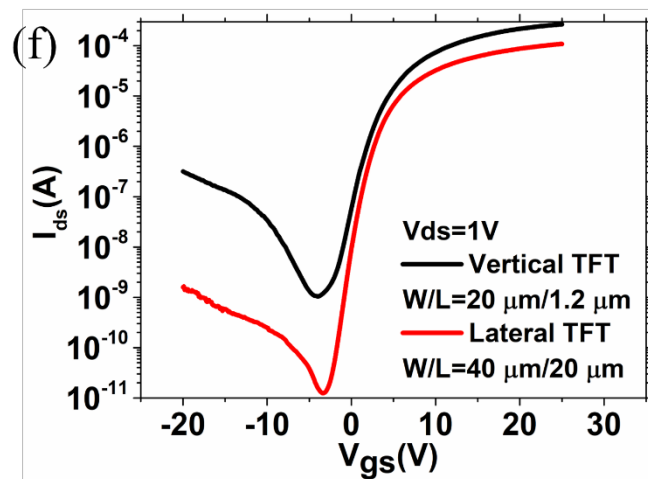
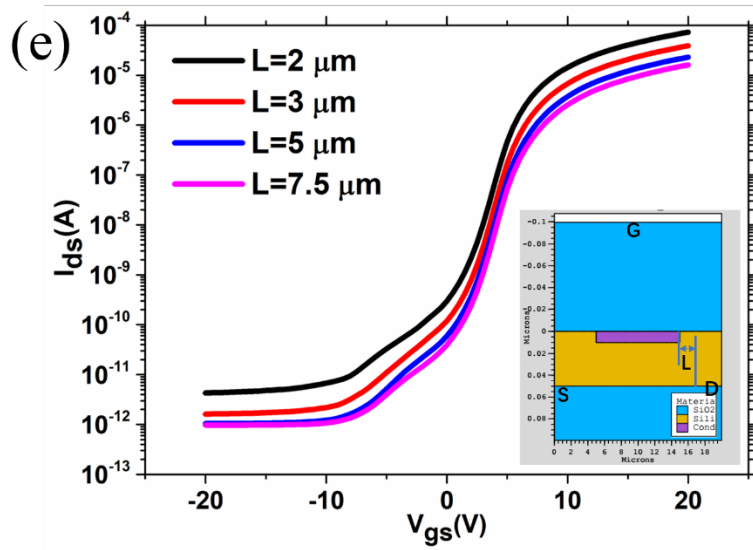
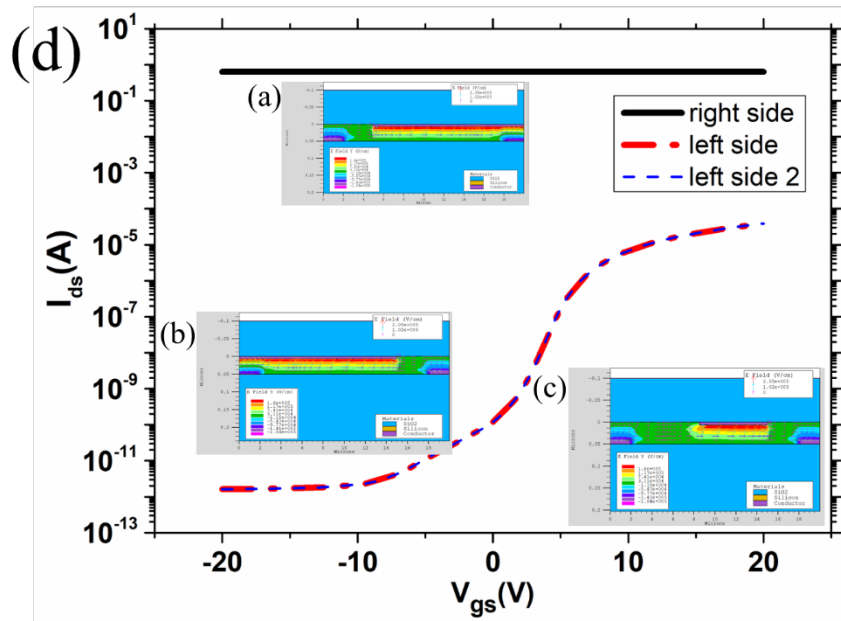


Figure 4: (a) the electrical field for the device with buried electrode overlapping with drain contact, (b) the electrical field for the device with buried electrode overlapping with source contact, (c) the electrical field for the device with buried electrode within the source/drain contact separation, (d) the comparison of the transfer characteristics with different buried electrode conditions corresponding to figure 4(a), 4(b), and 4(c), (e) the transfer characteristics with different channel lengths, the on-current increase in reverse proportion to the channel lengths, the drain-source voltage V_{ds} is 5V, (f) experimental demonstration of the short channel effects, the off-current is much higher for the short channel device ($L=1.2 \mu\text{m}$) than for the long channel device ($L=20 \mu\text{m}$).

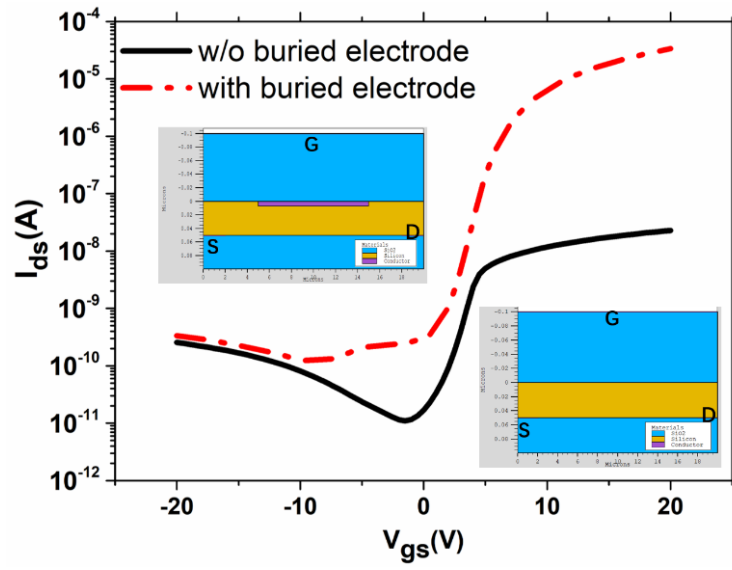
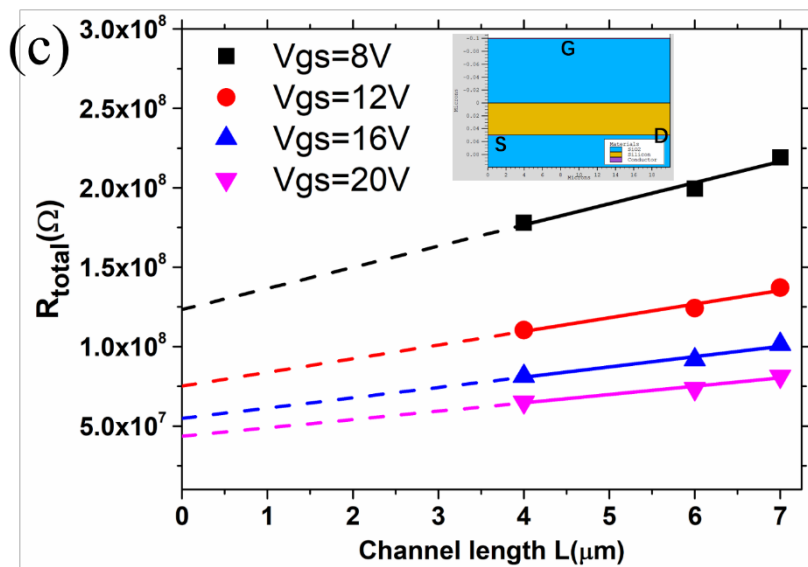
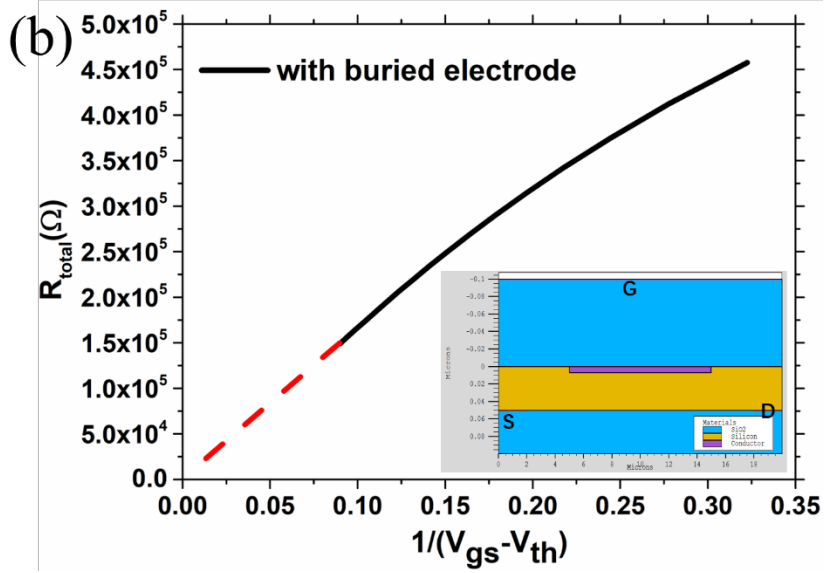
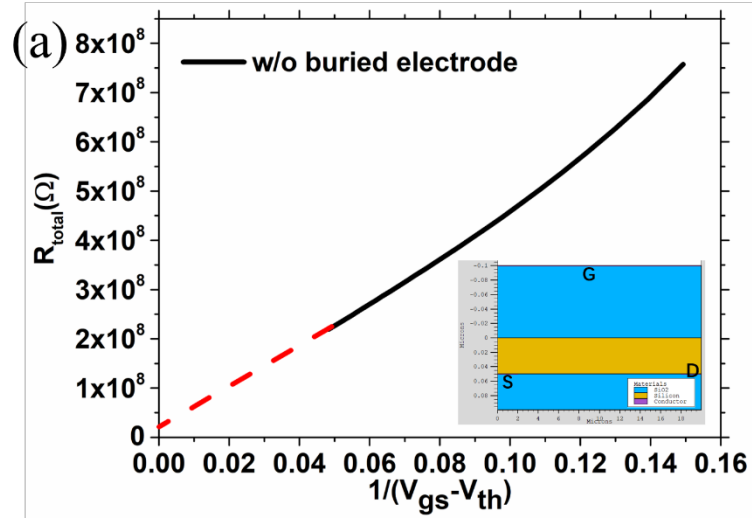


Figure 5: Transfer characteristics of the devices with Schottky source and drain contacts, and with or without buried electrode.



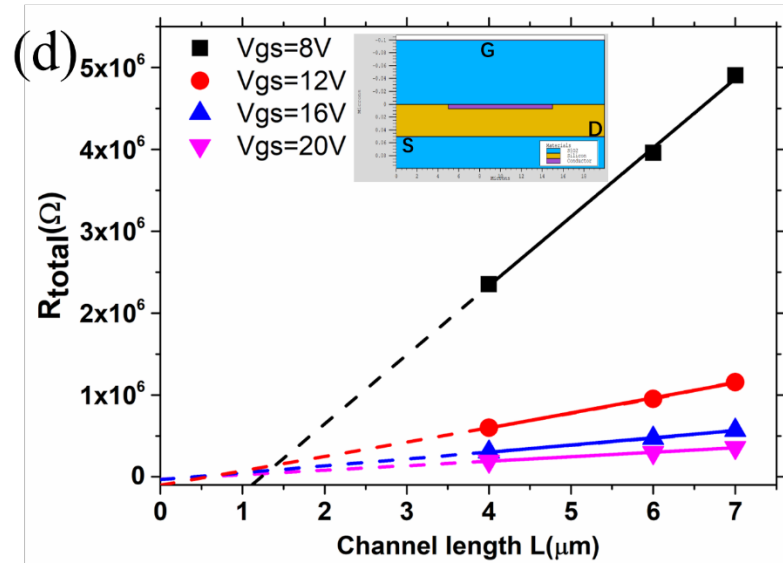


Figure 6: (a) and (b) access resistances from transfer curves for the devices with and without buried electrode, (c) and (d) access resistances from transmission line method for the devices with and without buried electrode.

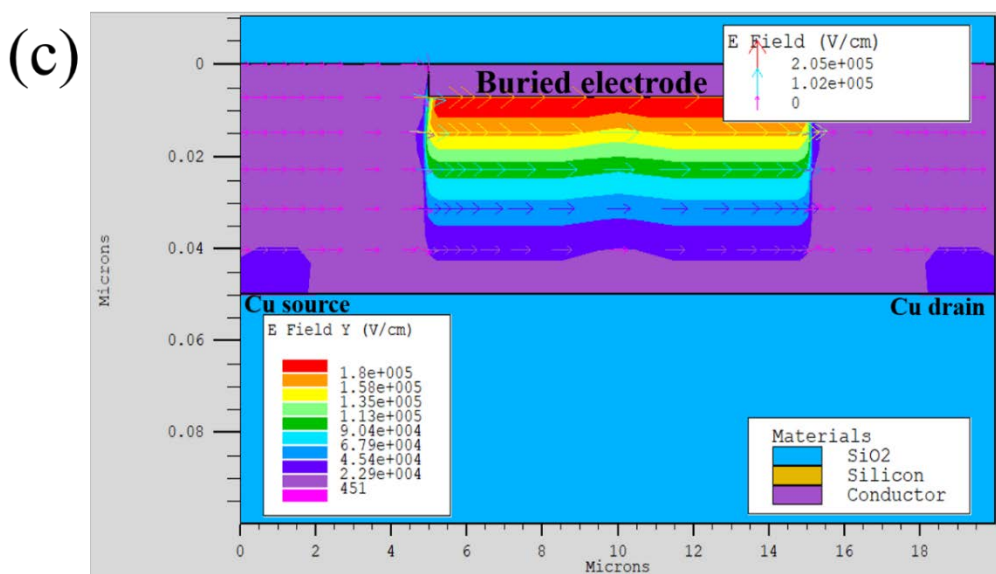
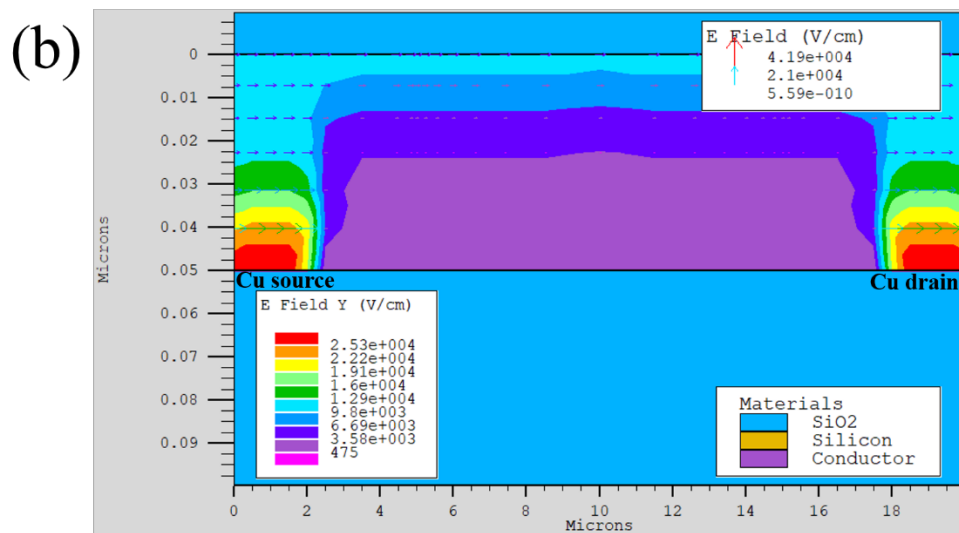
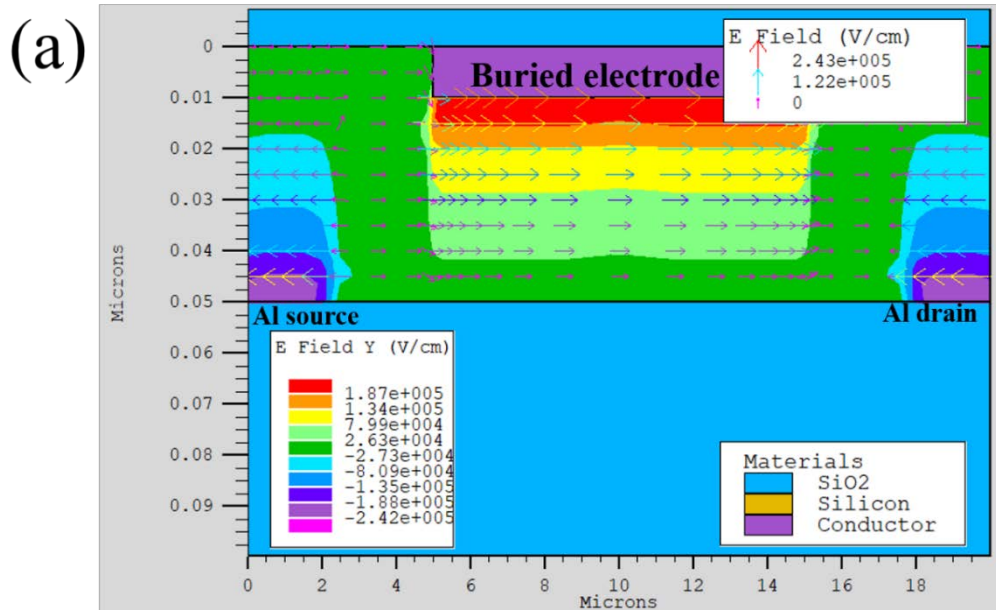


Figure 7: (a) the electric field for the device with aluminum (Ohmic) source /drain and with buried electrode, (b) the electric field for the device with copper (Schottky) source/drain and without buried electrode, (c) the electric field for the device with copper (Schottky) source/drain and with buried electrode.