



An organic ambipolar charge trapping non-volatile memory device based on double heterojunctions

Peng Zhang, Emmanuel Jacques, Laurent Pichon, Olivier Bonnaud

► To cite this version:

Peng Zhang, Emmanuel Jacques, Laurent Pichon, Olivier Bonnaud. An organic ambipolar charge trapping non-volatile memory device based on double heterojunctions. *Thin Solid Films*, 2022, 759, pp.139458. 10.1016/j.tsf.2022.139458 . hal-03776593

HAL Id: hal-03776593

<https://hal.science/hal-03776593>

Submitted on 16 Sep 2022

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

An organic ambipolar charge trapping non-volatile memory device
based on double heterojunctions

Peng Zhang^{a)}, Emmanuel Jacques, Laurent Pichon, Olivier Bonnaud

Peng Zhang^{a)}

College of Integrated Circuit Science and Engineering, Nanjing
University of Posts and Telecommunications, Nanjing 210023, P. R.
China

^{a)} Electronic mail: zp@njupt.edu.cn

Emmanuel Jacques, Laurent Pichon, and Olivier Bonnaud

Département OASiS (Organic And Silicon Systems), Institut
d'Electronique et des Technologies du numéRique, Université de
Rennes 1, 35042 Rennes Cedex, France

Highlights :

- 1) Memory device based on double heterojunctions enables fully-electrical operation.
- 2) The C₆₀/Pentacene sole heterojunction shows large built-in field.
- 3) The double heterojunctions suppress the large built-in field.

Abstract

An organic ambipolar charge trapping non-volatile memory device is proposed based on tris(8-hydroxy quinoline) aluminum(Alq₃)/

fullerene(C_{60})/pentacene double heterojunctions. The double heterojunctions were analyzed and compared with the sole heterojunction. Even though the Alq_3 /pentacene sole heterojunction shows a negative threshold voltage shift for programming under negative biasing, light illumination is required to efficiently erase. In contrast, for C_{60} /pentacene sole heterojunction, the negative shift of threshold voltage is observed even with a positive erasing voltage. By combining the two trapping layers, a large memory window with fully-electrical programming and erasing is obtained. The efficient programming and erasing of the double heterojunctions structure are analyzed, sufficient electrons can be injected that enables the electrical erasing, and the negative shift of the threshold voltage under positive erasing voltage for the C_{60} /pentacene structure is suppressed due to the suppression of the large built-in potential for the sole heterojunction, which can be verified by a large positive shift for the pentacene/ C_{60} /pentacene double heterojunctions.

Key words: non-volatile memory, heterojunction, ambipolar charge trapping, built-in field

1. Introduction

With the rapid development of the semiconductor industry and information technology, non-volatile memory emerges as a

promising and important branch for information storage and exchange. Since S. M. Sze et al. proposed the thin film floating gate non-volatile memory based on field effect transistor configuration [1], diverse non-volatile memories based on field effect transistor configuration have been developed, such as the nano-particle floating gate memory [2, 3], single-electron memory cell [4], Silicon Oxide Nitride Oxide Silicon (SONOS) memory [5, 6], ferroelectric memory [7], and so forth. The most representative application of the non-volatile memory lies in the Flash memory, where the industrial applications have been envisioned. For this application, traditional floating gate memory has been applied at the early state using semiconductor or metal floating gate as the charge storage layer [8], where SONOS is an ameliorated device using nitride as the charge trapping layer, therefore, it potentially enables higher charge storage capability, and it gradually becomes the mainstream of Flash memory [9]. With the scale-down of the floating gate memory and thus improved integration density, single-electron memory has also been proposed using nanocrystal as the charge trapping layer, thus the Coulomb blockade effect is obtained, which supports single electron storage, and this type of memory shows potential applications [10]. Ferroelectric memory adopts ferroelectric materials to achieve different polarization properties and change the

memory states, which shows its advantage in high operating speed, and thus is an excellent substitute for the conventional non-volatile memory [11]. The non-volatile memory device has also been applied in other fields, such as in displays [12], in artificial synapse [13], in sensors [14], in radio-frequency identification tags [15], and in other portable electronic devices [16,17].

For the typical non-volatile memories listed above, excepting for the ferroelectric memory that uses residual polarized charges under electric field to change the memory states, most of the non-volatile memories function by charges trapping and detrapping under the external gate bias or by other measurements such as the light illumination, which forms the binary current states of the non-volatile memory. In addition to the conventional inorganic non-volatile memory for high-speed applications, organic non-volatile memories have also been proposed, mainly focusing on low-cost, large-area fields with a low-processing-temperature that is compatible with flexible substrates. For organic non-volatile memory, the conventional device adopts metallic charge trapping layer [18], which is easy for stored charges leakage, or employs the electret memory configuration with dielectric charge trapping layer, which is always limited by the operation speed [19]. Semiconductor could also be applied as the charge trapping layer of organic

non-volatile memory cell, which can potentially provide moderate charge storage capability as well as higher operation speed. In one type of organic non-volatile memory, the organic semiconductor charge trapping layer is in direct contact with the active layer, which may enable to improve the memory performance due to the elimination of tunneling layer. However, there may be heterojunction effect, where the Fermi levels alignment causes the band bending and the built-in field that hinders or facilitates the injection of the carriers from the active layer to the charge trapping layer. The band bending and the built-in field caused by the energy level alignment has also been proved in organic heterojunctions, such as in Copper (II)

1,2,3,4,8,9,10,11,15,16,17,18,22,23,24,25-hexadecafluoro-29H,31H-phthalocyanine ($F_{16}CuPc$)/ Copper (II) Phthalocyanine ($CuPc$) heterojunction [20], in Zinc Phthalocyanine ($ZnPc$)/ fullerene (C_{60}) heterojunction [21]. The band bending due to the Fermi-level alignment causes space charge regions that the charge accumulates at the heterojunction interface to form accumulation-type heterojunction, or charge depletes at the heterojunction interface to form depletion-type heterojunction. Due to the space charge region, there forms built-in field pointing from P-type region to N-type region. The hindering effect of the built-in field is demonstrated as a

smaller memory window or even suppression of the memory window, which will adversely affect the memory performance.

For the organic non-volatile memory employing semiconductors as the charge trapping layer, several parallel works have been demonstrated. Ref [22] shows an organic non-volatile memory based on P₃HT nanofiber/F₁₆CuPc thin layer heterojunction, a stable current ratio and long retention time are obtained, while the device with thick F₁₆CuPc layer does not show hysteresis effect, which puts forward the rigid requirement on the film thickness. Ref [23] shows a non-volatile memory based on pentacene/Zinc oxide (ZnO) heterojunction, where the electrical characteristics vary with ZnO film thickness, also indicating the rigid requirement of ZnO film thickness to obtain a non-volatile memory. Ref [24] demonstrates the introduction of N-type *N,N'*-ditridecyl-3,4,9,10-perylenetetracarboxylic diimide between poly(2-vinyl naphthalene) and pentacene, which lowers the injection barrier of the carriers from pentacene due to the energy level alignment, and thus improves the memory characteristics, especially in terms of larger memory window. For the previous works, even though good memory characteristics have been obtained, the basic working principles of the heterojunction memory are not elucidated or unified, which needs further working on this aspect.

In this article, the organic thin film transistor (OTFT) non-volatile memory based on double heterojunctions incorporating three organic semiconductor layers' stacking is studied, where the basic principle that the heterojunction effect of a sole heterojunction is suppressed due to the interaction of the built-in electric fields between the two heterojunctions, is proposed in this article. The suppression of the heterojunction effect enables the improvement of the memory performance and enables fully-electrical operation.

2. Experimental section

The fabrication process of the OTFT non-volatile memory is based on a bottom-gate, top-contact configuration. Initially, the heavily-doped silicon wafer substrates covered with 300 nm thermally oxidized silicon oxide (SiO_2) layer were employed as the gate electrode and gate dielectric layer, respectively. The silicon substrates are N-type doped with arsenic, and the doping concentration is approximately 10^{20} cm^{-3} . The 300 nm SiO_2 layer is formed by dry oxidation method in oxygen atmosphere with high quality, which was deposited by the manufacturer. For the 6-inch silicon substrates, they were cut into 1.5 cm×1.5 cm slices. The substrates were cleaned by acetone, alcohol, and deionized water, respectively for 10 minutes and assisted by ultrasonic oscillation. Thereafter, the cleaned

substrates were heated in an oven in order to remove the organic residual and the moisture, and then the samples were treated with an ultraviolet/ozone surface cleaner. After that, 25 nm Alq₃/65 nm C₆₀/50 nm pentacene layers were deposited in sequence by thermal evaporation with a well-controlled evaporation rate. Alq₃ is bought from TCI Shanghai Co., the purity is 98%, and the molecular weight is 459.44. C₆₀ is bought from Shanghai Aladdin Co., the purity is 99.9%, and the molecular weight is 720.64. Pentacene is bought from TCI Shanghai Co., which is purified by sublimation. The three organic semiconductors were used as received. For controlling the thicknesses of different organic layers, the crystal oscillator is used to monitor the film thickness during the deposition process, assisted by using step profiler to further check the actual thickness. For Alq₃, the evaporation rate is 0.067 nm/s at the evaporation temperature of 210 °C. For C₆₀, the evaporation rate is 0.17 nm/s at the evaporation temperature of 420 °C. For pentacene, the evaporation rate is 0.13 nm/s at the evaporation temperature of 170 °C. Note that, Alq₃ shows high moisture/oxygen stability in ambient air, thus it could also function as a passivation layer deposited on SiO₂ layer. The reference device with 25 nm Alq₃/50 nm Pentacene heterojunction structure was also fabricated in the same conditions. In addition, for reference devices without Alq₃ passivation layer, a thin polystyrene (PS) layer was spin-coated on SiO₂ layer, then

C₆₀/pentacene heterojunction and pentacene/C₆₀/pentacene double heterojunctions were also fabricated on the thin PS layer. PS is bought from Shanghai Aladdin Co., and the molecular weight is 104.14. PS is dissolved in toluene to form a 3 mg/mL solution, and the spin-coating is carried out with a spin-coating speed of 3000 rpm for 30 s, resulting a deposited thickness of approximately 10 nm. The devices were accomplished by thermally evaporating a thick copper layer, the source and drain contacts were patterned by shadow masks, which defines a channel width/length ratio of 1500 μm /100 μm . The copper layer thickness is approximately 133 nm, with an evaporation thickness of 0.2 nm/s at a heating current of 79 A. The uniformity of the devices has also been checked by measuring different devices, and there are 20 samples on one substrate slice. For each structure, two slices were used. Therefore, there are 40 devices for each structure. The schematic view of the fabricated non-volatile memory device is shown in Fig. 1(a). All the electrical measurements were carried out by a Keithley 4200 SCS semiconductor parameter analyzer in ambient air.

3. Results and discussion

The initial trial is based on a sole Alq₃/pentacene heterojunction memory device without depositing C₆₀ layer, where the hysteresis

property of the transfer characteristics at drain-source voltage $V_{ds} = -30$ V is shown in Fig. 1(b). Initially, the threshold voltage of the memory device is -2.7 V, and after -120 V programming for 1 s, the threshold voltage shifts to -51.9 V, indicating a hysteresis window of 49.2 V under -120 V programming. However, the erasing can only be accomplished by light illumination, which generates sufficient photogenerated carriers that recombine with the trapped holes in Alq₃. In order to be efficiently erased, N-type organic semiconductors, such as C₆₀, are supposed to be capable of efficiently erasing, which own large lowest unoccupied molecular orbital difference with pentacene that facilitate the electrons injection, and are good electron transporting layers. The introduction of C₆₀ between pentacene and Alq₃ built up double heterojunctions, which may benefit for charge injection. The output characteristics of the non-volatile memory based on double heterojunctions is shown in Fig. 1(c), where the linear and saturation regimes are well discriminated, indicating the field effect of the fabricated OTFT memory. Fig. 1(d) shows the transfer characteristics of the fabricated double heterojunctions device, where the ambipolar charge trapping of holes and electrons is demonstrated. This ambipolar charge trapping property is not obtained for the memory devices with a single heterojunction [22, 23]. In addition, the ambipolar transport

characteristics of a single transfer curve were also observed, indicating the efficient P-type transporting in pentacene, and efficient N-type transporting in C₆₀, meaning that the built-in field between pentacene and C₆₀ that hinders the negative charge from injecting from pentacene to C₆₀, should be suppressed. In a reference device, for both of the initial and writing states, the ambipolar transport characteristics were demonstrated, while for the erasing state, the unipolar transport characteristics was demonstrated, indicating the suppression of the heterojunction effect by holes trapping, and the enhancement of the heterojunction effect by electrons reverse trapping. In fact, the trapping (writing) and reverse trapping (erasing) cause the changes of the band bending and the built-in field. For the transfer characteristics, the drain-source voltage is -30 V, therefore, the drain current follows the formula in saturation regime:

$$I_{ds} = \frac{W}{2L} C_i \mu_{FE} (V_{gs} - V_{th})^2 \quad (1)$$

Where the W/L is channel width/length ratio, C_i is the gate capacitance per unit area, μ_{FE} is the field effect mobility, V_{th} is the threshold voltage, and V_{gs} is gate-source voltage. From this formula, the field effect mobility and the threshold voltage can be deduced. Initially, a threshold voltage of -10.5 V is obtained, after applying a -120 V programming voltage for 1 s, the threshold voltage shifts to

-40.3 V, indicating a hysteresis window of 29.8 V. When applying a positive erasing voltage of 120 V for 1 s, the threshold voltage positively shifts to 16.2 V, which demonstrates a hysteresis window of 26.7 V and thus a global hysteresis window of 56.5 V, indicating a fully-electrical driving non-volatile memory. Note that, the programming and erasing voltages of ± 120 V are rather high, which can be reduced by decreasing the gate dielectric layer thickness, or adopting high-K dielectric. This can also maintain the ratio between the memory window and the programming voltage, which will be the further work. For the initial, programming and erasing states, the calculated field effect mobility is approximately $0.07 \text{ cm}^2/\text{V}\cdot\text{s}$. In addition, from the hysteresis curves, a memory ratio of approximately 5×10^3 is obtained at the gate bias of -20 V from the contrast between the drain-source currents for programming and erasing states. Note that, for the electrical characterization, the central 9 devices of one slice were used, and therefore, 18 devices are needed to be measured in one structure. High repeatability with almost same memory window and memory ratio was obtained for the 18 devices by passivating the substrates and better controlling the thicknesses of each layer.

The charge trap density for the programming and erasing states can be obtained from the following formula:

$$N_T = \frac{C_i \Delta V_{th}}{q} \quad (2)$$

Where ΔV_{th} is the threshold voltage shift, and q is the charge element. For the programming procedure, the memory window is 29.8 V, thus the charge trap density is calculated to be $2.14 \times 10^{12} \text{ cm}^{-2}$, while for the erasing procedure, the memory window is 56.5 V, and thus the charge trap density is approximately $4.06 \times 10^{12} \text{ cm}^{-2}$.

Due to the introduction of C_{60} , the double heterojunctions are formed. In order to further study the heterojunction effect, a different kind of double heterojunctions incorporating C_{60} deposition prior to Alq_3 deposition is fabricated, and the hysteresis property of this C_{60}/Alq_3 /pentacene double heterojunctions is shown in Fig. 1(e). From the transfer curves, the -80 V programming causes a threshold voltage similar to the sole Alq_3 /Pentacene heterojunction, where it can only be partially erased even with a larger positive erasing voltage of 120 V, which inhibits the application of this C_{60}/Alq_3 /pentacene double heterojunctions.

In order to further study the heterojunction effect in the non-volatile memory, C_{60} /pentacene heterojunction and symmetric pentacene/ C_{60} /pentacene double heterojunctions structures were also fabricated and compared. For the sole C_{60} /pentacene heterojunction, the typical transfer characteristics are shown as Fig. 2(a), with an initial threshold voltage of approximately -11.7 V, and interestingly,

when applying a positive gate bias of 120 V for 1 s, the threshold voltage negatively shifts to -19.4 V, instead of a positive threshold voltage shift under the positive gate bias. This can be explained as followings: due to the large Fermi levels difference of C_{60} and pentacene, there are electrons transferring from pentacene to C_{60} , which cause the band bending and the built-in field pointing from pentacene to C_{60} . When applying a positive voltage of 120 V, the strong built-in field can still drive the holes to inject from pentacene to C_{60} , which overcomes the external electrical field. This elucidation is not suggested previously [22-24]. In fact, when applying the positive gate bias, the external electric field points from C_{60} to pentacene, which is opposite to the built-in field. With the external electric field, the space charge region shrinks, however, the built-in field is strong, which may inhibit the carriers from injecting under the external field. This can be verified by applying a -120 V gate bias on the same device, where the threshold voltage has shifted beyond the scope of the scanning regime (from 50 V to -60 V), indicating the combination effect of the external electric field and the built-in field. In contrast, for pentacene/ C_{60} /pentacene double heterojunctions structure, the initial threshold voltage is approximately -9.2 V, and after applying a positive gate bias of 120 V, the threshold voltage shifts to approximately 35.1 V, indicating

the external gate bias dominates the trapping procedure, as show in Fig. 2 (b). As the carriers are initially injected from the top pentacene layer, the effect of the built-in field in the sole C_{60} /pentacene heterojunction that hinders the charge injection has been partially suppressed. Note that, the memory state can only be partially erased at -120 V for 1 s, while it can be efficiently erased at -120 V for 10 s.

In order to explain the anomalous phenomena of the C_{60} /Pentacene sole heterojunction, the pentacene/ C_{60} /pentacene double heterojunctions, and the Alq₃/ C_{60} /pentacene double heterojunctions, the energy diagrams of these heterojunctions are shown in Fig. 2(c), 2(d), and 2(e), respectively. Based on the references [25, 26], the estimated potential barrier of electrons for pentacene/ C_{60} heterojunction is approximately 0.5 eV, while the estimated potential barrier of electrons for Alq₃/ C_{60} heterojunction is approximately 0.6 eV. In addition, the precise band bending conditions cannot be assured, especially for C_{60} layer. Therefore, to be more accurate, at this stage, the band bending of C_{60} layer is not given. In Fig. 2(c), the chemical potential alignment results in the built-in field pointing from pentacene to C_{60} , which drives the holes to inject from pentacene to C_{60} , even with a positive gate bias. In contrast, as shown in Fig. 2(d), for the pentacene/ C_{60} /pentacene double heterojunctions, due to the

opposite built-in field directions of the two heterojunctions, they are partially counteracted, which is demonstrated as smaller band bending of both pentacene and C_{60} . For Alq_3/C_{60} /pentacene double heterojunctions, the built-in field can be further suppressed, showing as less band bending in Fig. 2(e), the ambipolar transport characteristics of the transfer curves and the larger threshold voltage shift can thus be obtained. Therefore, the external gate bias dominates the operation procedures for the non-volatile memory based on double heterojunctions. The precise band bending data can be measured by ultraviolet photoelectronic spectroscopy (UPS). In addition, due to the reproducible memory window and memory ratio for different devices, the potential barrier heights variation can be negligible in the same run.

In the practical measurements, the write-read-erase-read (WRER) measurement is also carried out. In our measurements, more than 100 cycles were tested. As mentioned above, the memory ratio of approximately 5×10^3 is obtained at the gate bias of -20 V. Therefore, in WRER measurement, the setting parameters is shown as followings: the writing voltage is -120 V for 5 time intervals, the reading voltage is -20 V for 5 time intervals, and the erasing voltage is 120 V for 5 time intervals. In order to further analyze the WRER property, five cycles are chosen, as shown in Fig. 3(a). For the

reading current after -120 V programming, it is approximately -4×10^{-9} A, while for the reading current after 120 V erasing, it is approximately -5×10^{-6} A, indicating a reading current ratio of more than 10^3 . This reading current ratio is in accordance with the memory ratio mentioned above, and also consists with the previous works [22-24]. In order to show the aging characteristics, the endurance property is also given for 100 cycles, as shown in Fig. 3(b). After -120 V programming, the low-level current increases from -3×10^{-9} A to less than -5×10^{-9} A, and then reduces again to approximately -3×10^{-9} A. In contrast, after 120 V erasing, the high-level current reduces from -6×10^{-6} A to approximately -2×10^{-6} A, indicating a current ratio of more than 5×10^2 . This stable endurance property indicates the good device quality, and also indicates the possibility of a multi-level non-volatile memory device to further enlarge the storage capability. Another property index of the non-volatile memory device is the retention time, which is shown in Fig. 3(c). As shown from the retention curves, after applying 120 V for 1 s, the high-level current decreases rapidly from 4×10^{-6} A to 2×10^{-8} A, indicating a 200 times reduction of the high-level current. In contrast, after applying -120 V gate bias for 1 s, the low-level current increases slightly from 2×10^{-9} A to 4×10^{-9} A. The remarkable reduction of the high-level current results in a short

retention time, where the high-level and low-level currents cannot be discriminated by approximately 30 hours. It is assumed that the rapid reduction of the high-level current is due to the rapid loss of the trapped electrons in C_{60} , especially when C_{60} is in direct contact with pentacene and Alq_3 from both sides. The retention time is only comparable with the previous work in [23], however, inferior to the previous works in [22] and [24].

In order to improve the retention property, a thin PS tunneling layer is deposited on top of the Alq_3/C_{60} heterojunction, and then pentacene layer is deposited. The structure of the device with PS tunneling layer is sketched as the inset of Fig. 4(a), where the thin PS layer is deposited above the Alq_3/C_{60} heterojunction. Transfer characteristics of the fabricated devices are shown in Fig. 4(a), and a smaller hysteresis window is obtained. The obtained rapid increase of the low-level current might be due to the detrapping of the holes, as shown in Fig. 4(b). In contrast, when applying a positive gate bias of 120 V, the electrons are trapped, and the electrons trapping is comparatively stable. The low retention time is maybe due to the comparatively high conductivity of C_{60} , which facilitates holes leakage. In addition, the much faster holes detrapping may also be due to the heterojunction effect. In fact, as shown in Fig. 4(c), for a reference device based on Alq_3/C_{60} heterojunction using C_{60} as the

active layer, a negative programming voltage of -120 V results in a positive threshold voltage shift, instead of a negative threshold voltage shift under the negative gate bias, indicating the electrons trapping even with negative gate bias, which might be due to the built-in field of $\text{Alq}_3/\text{C}_{60}$ sole heterojunction. For this improved structure, the high-level and low-level currents cannot be discriminated by more than 100 hours, which are still far from the practical applications, and the working mechanism of the charge leakage needs to be further studied. Nevertheless, the double heterojunctions non-volatile memory device shows a prototype for realizing the ambipolar charge trapping and fully-electrical driving memory device, and the basic mechanism of the double heterojunctions memory is preliminarily demonstrated.

4. Conclusions

The non-volatile memory devices based on $\text{Alq}_3/\text{C}_{60}$ /pentacene double heterojunctions were fabricated and analyzed. Compared to the Alq_3 /pentacene sole heterojunction adopting light illumination erasing, the double heterojunctions enable a fully-electrical driving memory device, and the ambipolar charge trapping was achieved. From the analysis of the C_{60} /pentacene sole heterojunction and the symmetric pentacene/ C_{60} /pentacene double heterojunctions, the

built-in field of the sole heterojunction is beneficial for holes injection while inhibiting the electrons injection. By suppressing the large built-in field adopting double heterojunctions, both of the holes and electrons injections can be achieved. The WRER property shows a large reading current ratio of approximately 10^3 , while during the 100-cycle endurance test, the stable current ratio of more than 5×10^2 is obtained. The retention property is analyzed, where the fast electrons detrapping degrades the retention time. Even though improvement has been made to increase the retention time by introducing a thin PS tunneling layer, further work will be on the notable improvement of the retention time.

Credit author statement

Peng Zhang: Fabrication, Measurement, Writing

Emmanuel Jacques: Fabrication assistance, Validation

Laurent Pichon: Supervision

Olivier Bonnaud: Supervision

Conflicts of interest

We wish to confirm that there are no known conflicts of interest associated with this publication and there has been no significant financial support for this work that could have influenced its outcome.

We confirm that the manuscript has been read and approved by all named authors and that there are no other persons who satisfied the criteria for authorship but are not listed. We further confirm that the order of authors listed in the manuscript has been approved by all of us.

We confirm that we have given due consideration to the protection of intellectual property associated with this work and that there are no impediments to publication, including the timing of publication, with respect to intellectual property. In so doing we confirm that we have followed the regulations of our institutions concerning intellectual property.

Acknowledgements

This work was supported by the Natural Science Foundation of Jiangsu Province (BK20180762), and also sponsored by NUPTSF (Grant No. NY219099).

Reference:

- [1] S. M. Sze, Physics of Semiconductor Devices, second edition, Wiley, New York, USA, 1981.
- [2] S. Li, D. Guérin, S. Lenfant, and K. Lmimouni, Optimization of pentacene double floating gate memories based on charge injection regulated by SAM functionalization, AIP Adv. 8 (2018) 025110: 1-7. <https://doi.org/10.1063/1.5010403>.
- [3] Furkan Kuruoğlu, Murat Çalışkan, Merih Serin, Ayşe Erol, Well-ordered nanoparticle arrays for floating gate memory applications, Nanotechnology 31(21) (2020) 215203. <https://doi.org/10.1088/1361-6528/ab7043>.
- [4] Rashmit Patel, Yash Agrawal, Rutu Parekh, Single-electron transistor: review in perspective of theory, modelling, design and fabrication, Microsyst. Technol. 27 (2021) 1863–1875.

<https://doi.org/10.1007/s00542-020-05002-5>.

[5] Ji-Man Yu, Jun-Young Park, Tae Jin Yoo, Joon-Kyu Han, Dae-Hwan Yun, Geon-Beom Lee, Jae Hur , Byung-Hyun Lee , Seong-Yeon Kim, Byoung Hun Lee, Yang-Kyu Choi, Quantitative Analysis of High-Pressure Deuterium Annealing Effects on Vertically Stacked Gate-All-Around SONOS Memory, IEEE T. Electron Dev., 67(9) (2020) 3903-3907. 10.1109/TED.2020.3008882.

[6] Jae-Gab Lim, Seung-Dong Yang, Ho-Jin Yun, Jun-Kyo Jung, Jung-Hyun Park, Chan Lim, Gyu-seok Cho, Seong-gye Park, Chul Huh, Hi-Deok Lee, Ga-Won Lee, High Performance SONOS Flash Memory with In-Situ Silicon Nanocrystals Embedded in Silicon Nitride Charge Trapping Layer, Solid State Electron. 140 (2018) 134-138. <https://doi.org/10.1016/j.sse.2017.10.031>.

[7] You-Sheng Liu; Pin Su, Impact of Trapped-Charge Variations on Scaled Ferroelectric FET Nonvolatile Memories, IEEE T. Electron Dev. 68(4) (2021) 1639-1643. 10.1109/TED.2021.3061330.

[8] P. Blomme, A. Cacciato, D. Wellekens, L. Breuil, M. Rosmeulen, G. S. Kar, S. Locorotondo, C. Vrancken, O. Richard, I. Debusschere, and J. Van Houdt, Hybrid Floating Gate Cell for Sub-20-nm NAND Flash Memory Technology, IEEE Electr. Dev. L. 33(3) (2012) 333-335. 10.1109/LED.2011.2181152.

[9] Pooja Bohara, Santosh Kumar Vishvakarma, Overcoming bit loss mechanism in self-amplified multilevel silicon-oxide-nitride-oxide-silicon memory cell, *IEEE T. Electron Dev.* 65(10) (2018) 4297-4303. <https://doi.org/10.1002/jnm.2924>.

[10] Yasuo Azuma, Masanori Sakamoto, Toshiharu Teranishi, and Yutaka Majima, Memory operations in Au nanoparticle single-electron transistors with floating gate electrodes, *Appl. Phys. Lett.* 109 (2016) 223106: 1-5. <https://doi.org/10.1063/1.4971190>.

[11] T. Mikolajick, U. Schroeder; S. Slesazeck, The Past, the Present, and the Future of Ferroelectric Memories, *IEEE T. Electron Dev.* 67(4) (2020) 1434-1443. [10.1109/TED.2020.2976148](https://doi.org/10.1109/TED.2020.2976148).

[12] Seung-Hyuck Lee, Jongbin Kim, Seong Ho Yoon, Kyeong-Ah Kim, Sung-Min Yoon, Chunwon Byun, Chi-Sun Hwang, Gi Heon Kim, Kyoung-Ik Cho, and Seung-Woo Lee, Pixel Architecture for Low-Power Liquid Crystal Display Comprising Oxide and Ferroelectric Memory Thin Film Transistors, *IEEE T. Electron Dev.* 36 (6) (2015) 585–587. [10.1109/LED.2015.2424216](https://doi.org/10.1109/LED.2015.2424216).

[13] F. Molina-Lopez, T.Z. Gao, U. Kraft, C. Zhu, T. Öhlund, R. Pfattner, V.R. Feig, Y. Kim, S. Wang, Y. Yun, Z. Bao, Inkjet-printed stretchable and low voltage synaptic transistor array, *Nat. Commun.* 10 (2019) 2676: 1-10.

<https://doi.org/10.1038/s41467-019-10569-3>.

[14] T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, T. Sakurai, T. Someya, Organic Nonvolatile Memory Transistors for Flexible Sensor Arrays, *Science* 326 (2009) 1516–1519.

<http://dx.doi.org/10.1126/science.1179963>.

[15] P. Baude, D. Ender, M. Haase, T. Kelley, D. Muyres, S. Theiss, Pentacene-based radio-frequency identification circuitry, *Appl. Phys. Lett.* 82(22) (2003) 3964–3966. <https://doi.org/10.1063/1.1579554>.

[16] X. Chen, J. Pan, J. Fu, X. Zhu, C. Zhang, L. Zhou, Y. Wang, Z. Lv, Y. Zhou, and S. Han, Polyoxometalates-Modulated Reduced Graphene Oxide Flash Memory with Ambipolar Trapping as Bidirectional Artificial Synapse, *Adv. Electron. Mater.* 4(12) (2018) 1800444: 1-9, 2018. <https://doi.org/10.1002/aelm.201800444>.

[17] H. Huitema, G. Gelinck, J. van der Putten, K. Kuijk, C. Hart, E. Cantatore, P. Herwig, A. van Breemen, D. de Leeuw, Plastic transistors in active-matrix displays, *Nat.* 414 (2001) 599-599.

<https://doi.org/10.1038/414599a>.

[18] Zhengchun Liu, Fengliang Xue, Yi Su, Yuri M. Lvov, Kody Varahramyan, Memory effect of a polymer thin-film transistor with self-assembled gold nanoparticles in the gate dielectric, *IEEE T. Nanotechnol.* 5(4) (2006) 379-384.

<https://doi.org/10.1109/TNANO.2006.876928>.

- [19] Th. B. Singh, N. Marjanovi, G. J. Matt, N. S. Sariciftci, R. Schwödiauer, S. Bauer, Nonvolatile organic field-effect transistor memory element with a polymeric gate electret, *Appl. Phys. Lett.* 85(22) (2004) 5409-5411. <https://doi.org/10.1063/1.1828236>.
- [20] K. M. Lau, J. X. Tang, H. Y. Sun, C. S. Lee,^a and S. T. Lee, Donghang Yan, Interfacial electronic structure of copper phthalocyanine and copper hexadecafluorophthalocyanine studied by photoemission, *Appl. Phys. Lett.* 88 (2006) 173513:1-3. <https://doi.org/10.1063/1.2198484>.
- [21] Yingjie Xing, Shuai Li, Guiwei Wang, Tianjiao Zhao, and Gengmin Zhang, Field emission analysis of band bending in donor/acceptor heterojunction, *J. Appl. Phys.* 119 (2016) 245503: 1-8. <https://doi.org/10.1063/1.4955219>.
- [22] Hsuan-Chun Chang, Chien-Chung Shih, Cheng-Liang Liu, Wen-Chang Chen, A 1D Electrospun Nanofiber Channel for Organic Field-Effect Transistors Using a Donor/Acceptor Planar Heterojunction Architecture, *Adv. Mater. Interfaces* 2 (2015) 1500054: 1-5. <https://doi.org/10.1002/admi.201500054>.
- [23] Bhola Nath Pal, Phylcia Trottman, Jia Sun, and Howard E. Katz, Solution-deposited Zinc oxide and Zinc oxide/Pentacene Bilayer Transistors: High Mobility n-Channel, Ambipolar and Nonvolatile Devices, *Adv. Funct. Mater.* 18 (2008) 1832–1839.

<https://doi.org/10.1002/adfm.200701430>.

[24] Yiru Wang, Chao Lu, Limin Kang, Shangyang Shang, Jiang Yin, Xu Gao, Guoliang Yuan, Yidong Xia, and Zhiguo Liu, Enhanced Performance of Organic Field- Effect Transistor Memory by Hole-Barrier Modulation with an N- Type Organic Buffer Layer between Pentacene and Polymer Electret, *Adv. Electron. Mater.* (2020) 1901184: 1-9. <https://doi.org/10.1002/aelm.201901184>.

[25] S.J. Kang, Y. Yi, C.Y. Kim, S.W. Cho, M. Noh, K. Jeong, C.N. Whang, Energy level diagrams of C₆₀/pentacene/Au and pentacene/C₆₀/Au, *Synthetic Met.* 156 (2006) 32–37. <https://doi.org/10.1016/j.synthmet.2005.10.001>.

[26] Yu-Zhan Wang, Dong-Chen Qi, Shi Chen, Hong-Ying Mao, Andrew T. S. Wee, Xing-Yu Gao, Tuning the electron injection barrier between Co and C₆₀ using Alq₃ buffer layer, *J. Appl. Phys.* 108 (2010) 103719: 1-5. <http://dx.doi.org/10.1063/1.3514553>.

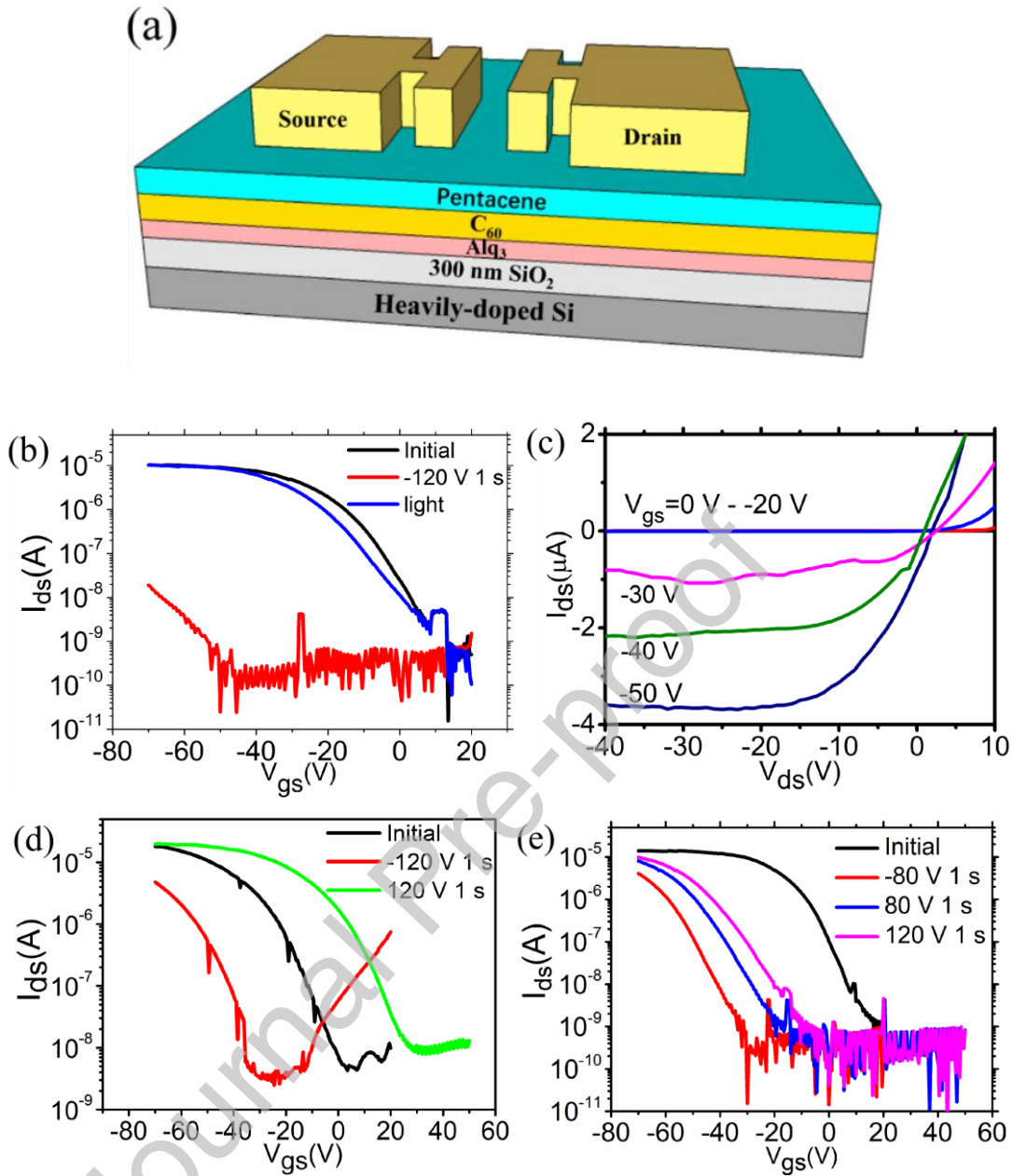


Figure 1: (a) schematic view of the fabricated bottom-gate, top-contact OTFT non-volatile memory device, (b) the hysteresis property of the sole Alq₃/pentacene heterojunction at $V_{ds} = -30$ V, (c) the output characteristics of the non-volatile memory based on the Alq₃/C₆₀/pentacene double heterojunctions, (d) the transfer characteristics of the non-volatile memory based on the Alq₃/C₆₀/pentacene double heterojunctions at $V_{ds} = -30$ V, (e) the

hysteresis property of the C_{60}/Alq_3 /pentacene double heterojunctions.

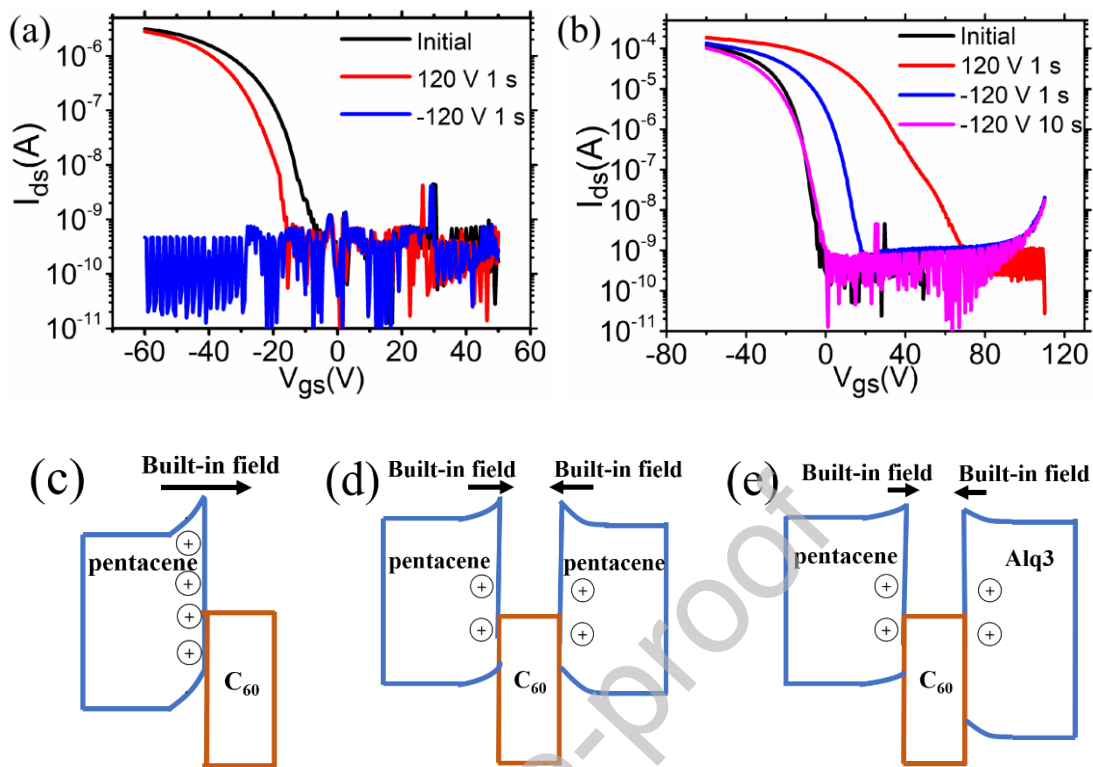


Figure 2: (a) the non-volatile memory performance of C_{60} /pentacene sole heterojunction, (b) the non-volatile memory performance of pentacene/ C_{60} /pentacene double heterojunctions, (c) energy diagram of the C_{60} /pentacene sole heterojunction, (d) energy diagram of pentacene/ C_{60} /pentacene double heterojunctions, and (e) energy diagram of Alq₃/ C_{60} /pentacene double heterojunctions.

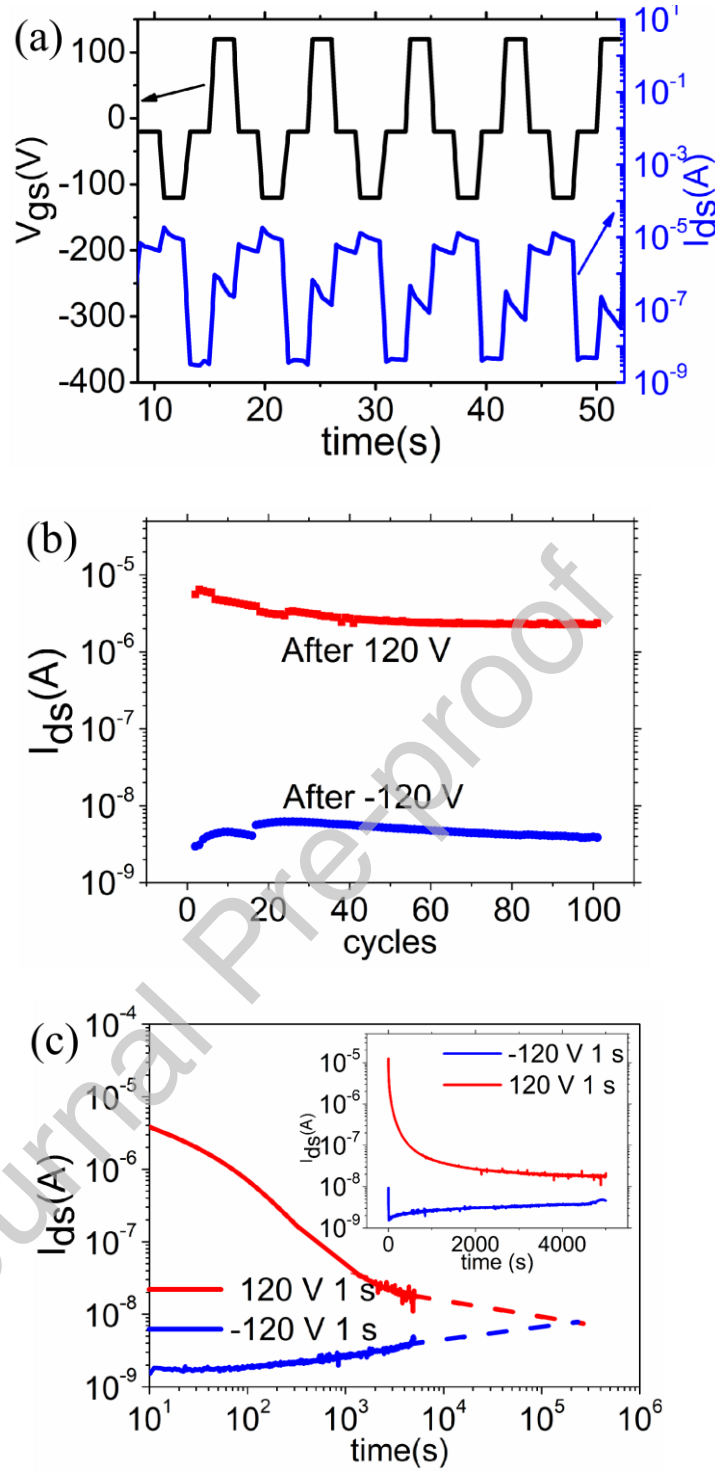


Figure 3: (a) Write-read-erase-read (WRER) property of the fabricated non-volatile memory, (b) endurance characteristics of the fabricated non-volatile memory with 100 cycles, (c) retention property of the fabricated device.

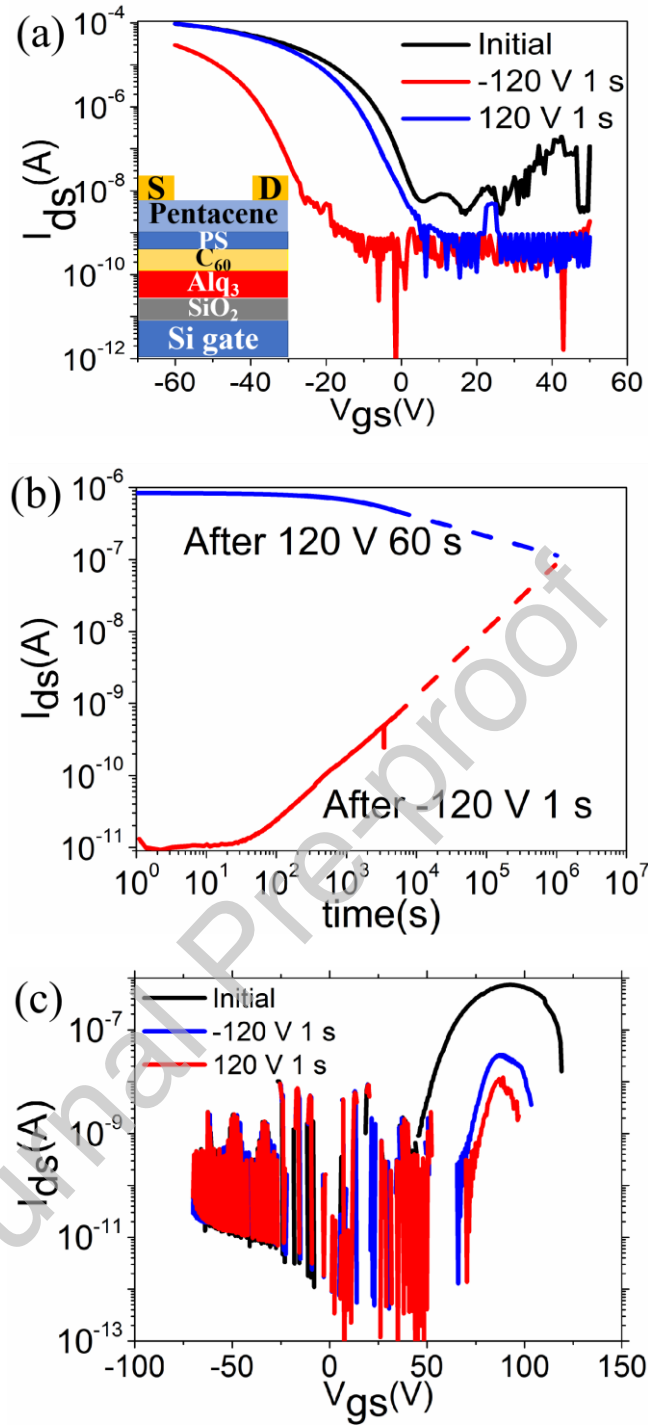


Figure 4: (a) the memory characteristics of the nonvolatile memory with PS tunneling layer on top of the Alq_3/C_{60} heterojunction, (b) the retention property of the non-volatile memory with PS tunneling layer, (c) the memory characteristics for Alq_3/C_{60} sole heterojunction.