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A Technique for the *In-Situ* Experimental Extraction of the Thermal Impedance of Power Devices

Ciro Scognamillo, Sebastien Fregonese, Thomas Zimmer, *Senior Member, IEEE*,
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***Abstract*—In this letter, an innovative technique is presented, which allows the experimental extraction of the junction-to-ambient thermal impedance (Z_{TH}) of power devices operating in their application environment (*in situ*). The technique draws inspiration from the thermal characterization of RF transistors, and is based on simple measurements of electrical signals, while not requiring a thermochuck, the calibration of a thermometer, as well as temperature sensors or IR cameras. The validation of the technique is unambiguously performed by applying the 'simulated experiments' strategy on a SiC-based multi-chip power module.**

***Index terms*–Electrothermal simulation, finite-element method simulation, *in-situ* thermal characterization, power devices, thermal impedance measurement.**

I. Introduction

Nowadays, the working conditions of power circuits are limited by their heat disposal capability. Utmost importance must be given to the self-heating thermal impedance (Z_{TH}) of devices [1], which fully describes their individual dynamic thermal behavior and allows defining power ratings and safe operating areas [2]. The Z_{TH} can be experimentally extracted through (i) an *indirect* temperature assessment with the measurement of a temperature-sensitive electrical parameter (TSEP), the temperature dependence of which (*thermometer*) has to be well established [3]–[6], or (ii) a *direct* temperature measurement by means of sensors (e.g., thermocouples) [7], [8] or IR cameras [9].

Unfortunately, both indirect and direct approaches are difficult or even impossible to apply for the evaluation of the overall junction-to-ambient Z_{TH} ($Z_{TH,j\text{-}a}$) of a power device operating in its application environment (*in situ*). The calibration of the thermometer is unviable in most cases, since the temperature of the backside of the system embedding the device under test is typically not controlled. Likewise, the adoption of sensors or IR imaging is inhibited, as the top surface of the device under test is often not exposed; moreover, direct methods are more suited for detecting slow or even dc thermal responses. Lastly, the evaluation of the *in-situ* $Z_{TH,j\text{-}a}$ with the above approaches also requires a nontrivial estimation of the ambient temperature.

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In this letter, a technique is proposed for the *in-situ* experimental extraction of the $Z_{TH,j\text{-}a}$, which relies on simple measurements of electrical signals and does not require a thermometer definition, costly equipment for the detection of temperature maps, or the assessment of the ambient temperature. The theory behind the technique is inspired by Müller [10] and Rinaldi [11], who laid the theoretical foundations for the frequency-domain thermal characterization of RF transistors from low-frequency *y*-parameters.

The technique is first presented along with the associated measurement setup, and then is unambiguously validated not by comparing it with traditional methods – unviable for *in-situ* extractions – but through the 'simulated experiments' strategy applied to a SiC-based multi-chip power module (PM) [12]. The validation is performed by emulating the experimental procedure with circuit-based electrothermal (ET) simulations accounting for a *known* $Z_{TH,j\text{-}a}$ used as a reference, and comparing the extracted $Z_{TH,j\text{-}a}$ with the reference counterpart.

II. *In-Situ* Extraction Technique

Regardless of the nature of the electronic component, the critical temperature impacting the I-V characteristics is conventionally referred to as junction temperature (T_j). As accurately described in [13], [14], the junction-to-ambient self-heating thermal impedance $Z_{TH,j\text{-}a}(t)$ [K/W] of a device embedded in a system is defined as

$$Z_{TH,j-a}(t) = \frac{T_j(t) - T_{amb}}{P_D} \tag{1}$$

where P_D is the amplitude of a dissipated power step applied at t=0 and T_{amb} is the ambient temperature. $Z_{TH,j\text{-}a}$ depends on (i) the geometry of the domain and of the heat source, (ii) thermal properties of the materials, and (iii) boundary conditions.

The thermal behavior in the frequency domain – analyzed in the power electronics scenario by Ma *et al.* in [15], [16] – is characterized by the junction-to-ambient power pulse thermal response $Z_{j\text{-}a}(f)$, which is the F-transformation of the time derivative of the thermal impedance $dZ_{TH,j\text{-}a}(t)/dt$ [17]. A simple fitting with a Foster thermal network allows converting any Z(f) to the corresponding $Z_{TH}(t)$ and *vice versa*.

A. Extraction Procedure

The extraction procedure is described for the specific case of a MOS transistor, yet, *mutatis mutandis*, it can be simply generalized to other power devices. The drain current (I_D) can be expressed as a function of the input voltages and junction temperature:

$$I_D = F_{I_D}\left(V_{DS}, V_{GS}, T_j\right) \tag{2}$$

which in the frequency domain becomes

$$I_D = F_{I_D}\left(V_{DS}, V_{GS}, Z_{j-a}\cdot P_D + T_{amb}\right) \quad (3)$$

Let us consider an operating condition in which $V_{GS}=V_{GSdc}$, and V_{DS} is given by the superposition of a dc value and a small ac signal ($V_{DS}=V_{DSdc}+V_{DSac}$); in this case, the V_{DS} derivative of (3) is given by

$$\frac{dI_D}{dV_{DS}} = \left.\frac{\partial F_{I_D}}{\partial V_{DS}}\right|_{T_{jdc}} + \left.\frac{\partial F_{I_D}}{\partial T_j}\right|_{V_{DSdc}} \cdot \frac{dT_j}{dV_{DS}} \quad (4)$$

where T_{jdc} is the T_j unaffected by the small signal (i.e., only determined by the dc bias). Let us denote as g_o the frequency-dependent output conductance of the transistor and as $g_o|_{T_{jdc}}$ the output conductance at $T_j=T_{jdc}$.

$$g_o(f) = \frac{dI_D}{dV_{DS}}; \quad g_o|_{T_{j,dc}} = \left.\frac{\partial F_{I_D}}{\partial V_{DS}}\right|_{T_{jdc}} \quad (5)$$

By making use of (5) in (4), it follows:

$$\frac{dT_j}{dV_{DS}}(f) = \frac{g_o(f) - g_o|_{T_{jdc}}}{\left.\frac{\partial F_{I_D}}{\partial T_j}\right|_{V_{DSdc}}} \quad (6)$$

According to the perturbative approach shown in [10],

$$\frac{dP_D}{dV_{DS}}(f) = I_{Ddc} + V_{DSdc}\cdot\frac{dI_D}{dV_{DS}}(f) = I_{Ddc} + V_{DSdc}\cdot g_o(f) \quad (7)$$

Since $T_j(f)=Z_{j-a}(f)\cdot P_D(f)+T_{amb}$, the term dT_j/dV_{DS} is given by

$$\frac{dT_j}{dV_{DS}}(f) = Z_{j-a}(f)\cdot\left[I_{Ddc} + V_{DSdc}\cdot g_o(f)\right] \quad (8)$$

from which

$$Z_{j-a}(f) = \frac{g_o(f) - g_o|_{T_{jdc}}}{\left.\frac{\partial F_{I_D}}{\partial T_j}\right|_{V_{DSdc}}\cdot\left[I_{Ddc} + V_{DSdc}\cdot g_o(f)\right]} \quad (9)$$

In (9), the term $\partial F_{I_D}/\partial T_j|_{V_{DSdc}}$ is a thermometer that should be in principle determined in a temperature-controlled environment. To make the $Z_{j-a}(f)$ evaluation only relying on *in-situ* measurements of electrical signals, such a term is simplified by normalizing (9) to $Z_{j-a}(0)$, which is the static value of $Z_{j-a}(f)$ and represents the junction-to-ambient thermal resistance ($R_{TH,j-a}$). The normalized junction-to-ambient power pulse thermal response $z_{j-a}(f)$ is given by

$$z_{j-a}(f) = \frac{Z_{j-a}(f)}{Z_{j-a}(0)} = \frac{g_o(f) - g_o|_{T_{jdc}}}{g_o(0) - g_o|_{T_{jdc}}}\cdot\frac{I_{Ddc} + V_{DSdc}\cdot g_o(0)}{I_{Ddc} + V_{DSdc}\cdot g_o(f)} \quad (10)$$

In (10), $g_o|_{T_{jdc}}$ is easily obtainable through a fitting of g_o, while $g_o(0)$ is the measured value at f=0 Hz. Further details are provided in [18].

Once $z_{j-a}(f)$ is extracted, the corresponding $Z_{j-a}(f)$ can be evaluated through a de-normalization process, which makes use of the junction-to-case power pulse thermal response $Z_{j-c}(f)$ (i.e., the Z(f) of the device not embedded in the assembly) taken from the device datasheet. First, a high-frequency matching range is identified, where the $Z_{j-c}(f)$ (known) and $Z_{j-a}(f)$ (to be determined) coincide, as the heat is still confined in the device region [19], [20]. Subsequently, $R_{TH,j-a}=Z_{j-a}(0)$ is tuned to make $Z_{j-a}(f)=z_{j-a}(f)\cdot R_{TH,j-a}$ coincide with $Z_{j-c}(f)$ in the matching range. This de-normalization procedure is schematically depicted in Fig. 1. Finally, $Z_{TH,j-a}(t)$ is obtained by (i) fitting $Z_{j-a}(f)$ with a Foster thermal network and (ii) computing its power step response.

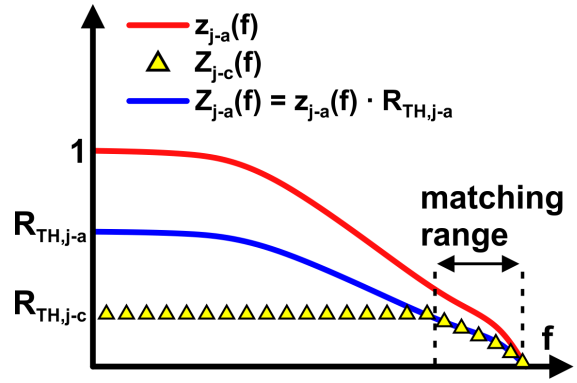

Fig. 1. Schematic representation of the de-normalization process: the $R_{TH,j-a}$ value is tuned to overlap $Z_{j-a}(f)$ (solid blue line) and $Z_{j-c}(f)$ (yellow triangles) in the high-frequency matching range; $z_{j-a}(f)$ is also shown (solid red line).

B. Measurement setup

The measurement circuit sketched in Fig. 2 is devoted to the extraction of g_o vs. frequency by operating in the time domain. The circuit requires: (i) two voltage supplies (i.e., V_{GGdc} and V_{DDdc}) making the transistor work at the desired bias point, that is, V_{DSdc} and I_{Ddc}; (ii) a voltage generator (V_{DDac}) applying a small-signal piecewise sinusoidal waveform; (iii) two voltage probes and a shunt resistor (R_{shunt}) allowing the sensing of $V_{DS}(t)$ and $I_D(t)$. For each frequency, the evaluation of g_o is performed according to the following equation:

$$g_o = \frac{RMS\left(I_D(t) - I_{Ddc}\right)}{RMS\left(V_{DS}(t) - V_{DSdc}\right)} = \frac{RMS\left(I_{Dac}(t)\right)}{RMS\left(V_{DSac}(t)\right)} \quad (11)$$

where RMS stands for root mean square.

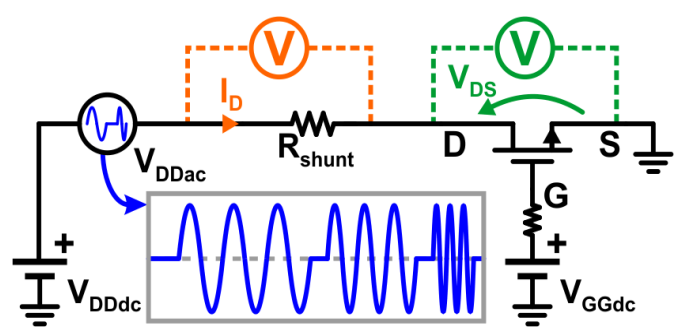

Fig. 2. Circuit conceived to perform the measurements of the electrical signals $V_{DS}(t)$ and $I_D(t)$. The gray box shows the small-signal piecewise sinusoidal waveform (solid blue line).

III. 'Simulated Experiments' Strategy

As other experimental methods are not suited for an *in-situ* extraction, the proposed technique was validated by resorting to the 'simulated experiments' strategy (e.g., [21], [22]), which also allows for an unambiguous accuracy verification since the $Z_{TH,j-a}$ to extract is *known*.

A PM embedding four SiC-based VDMOS transistors was considered as a case-study; the devices replicate the bare-die CREE product CPMF-1200-S080B (rated 1200 V, 50A [23]).

To emulate the *in-situ* $Z_{TH,j\text{-}a}$ extraction, the 'simulated experiments' strategy was applied to one of the devices mounted on the PM. The procedure is articulated as follows:

- First, the reference $Z_{TH,j\text{-}a}$ of the device was obtained through detailed purely-thermal 3-D FEM simulations in the COMSOL Multiphysics environment [24], in which the exact replica of the PM was reproduced (Fig. 3). The boundary conditions were accounted for through a heat transfer coefficient h=2×10^3 W/m^{2}K applied to the bottom surface of the thick copper baseplate, which describes the contact with an efficient heat-sink [25].
- The obtained reference $Z_{TH,j\text{-}a}$ was used to build a SPICE-compatible thermal feedback network (TFN) with a Foster topology [26]; the TFN was then coupled to the electrical model of the VDMOS transistor, the temperature-sensitive parameters of which were allowed to vary during the simulation run. The electrical model was calibrated on experimental data [27] and is thoroughly described in [28].
- Transient simulations were conducted in the OrCAD Capture software package [29] on the ET model to emulate the experimental procedure presented in Section II.B to extract the $z_{j\text{-}a}$.
- The $Z_{j\text{-}c}$ was determined by simulating the bare-die device with isothermal backside at 300 K in COMSOL.
- The de-normalization process and the time domain conversion were then carried out to obtain the thermal impedance $Z_{TH,j\text{-}a}$.
- The reference and extracted $Z_{TH,j\text{-}a}$s were finally compared.

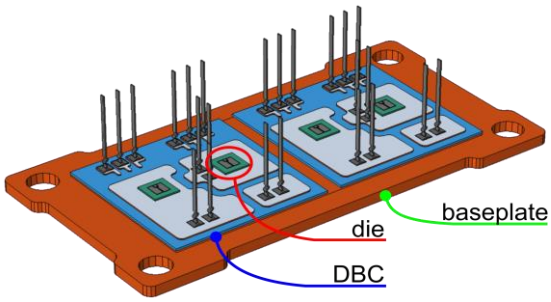

Fig. 3. 3-D representation of the PM under investigation reproduced in COMSOL Multiphysics. Evidenced are: the direct-bonded copper (DBC) substrate in the aluminum nitride technology, the copper baseplate, and the die corresponding to the VDMOS transistor on which the extraction technique was applied.

IV. Results and Discussion

The device was biased with V_{DDdc}=15 V, V_{GGdc}=10 V, and R_{shunt}=200 mΩ. For the given bias point, a preliminary investigation allowed observing that nonlinear thermal effects do not play a relevant role in defining the dynamic response of the assembly. Concerning the piecewise waveform, 3-period sinusoids were adopted for each frequency. The logarithmically-spaced frequency range was 3 mHz–20 kHz with six points per decade. The V_{DDac} waveform was approximately 1 hour long, while its amplitude was set at 0.5 V. The large thermal time constants introduced by the thick copper baseplate led to a relatively long duration of the experiment, this being the main drawback of the *in-situ* characterization of the assembly under analysis.

The I_D and V_{DS} vs. time waveforms were computed according to (11), and $z_{j\text{-}a}(f)$ was extracted through (10). Results are shown in Fig. 4, where the reference and extracted $z_{j\text{-}a}(f)$ are compared. An excellent agreement was achieved: considering the percentage mean-square error as a figure of merit, the mismatch between the two curves in the high-frequency matching range turned out to be 1.72%, while 0.34% was the discrepancy in the overall frequency range.

The de-normalization process discussed in Section II.A was then applied. Results are shown in Fig. 5; $R_{TH,j\text{-}a}$ was calibrated to 0.35 K/W (to be compared with the COMSOL reference $R_{TH,j\text{-}a}$=0.354 K/W) to overlap the curves in the 3–20 kHz matching range. Fig. 5 witnesses the agreement between the extracted and reference thermal responses $Z_{j\text{-}a}(f)$ and impedances $Z_{TH,j\text{-}a}(t)$.

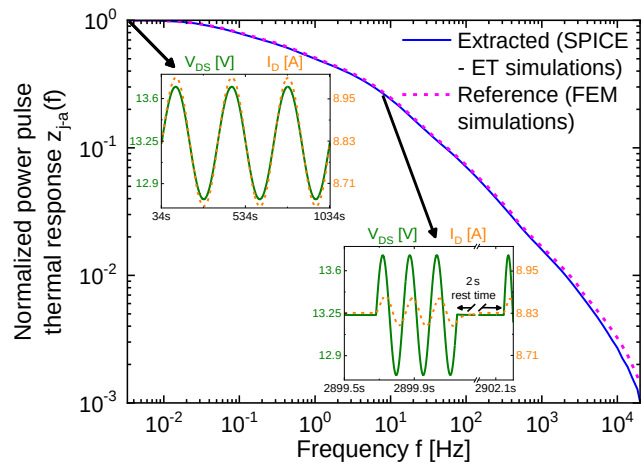

Fig. 4. Comparison between extracted (solid blue line) and reference (dashed magenta) $z_{j\text{-}a}(f)$. Also reported are the V_{DS} (solid green line) and I_D (dashed orange) vs. time waveforms at f=3 mHz and f=6 Hz (top-left and bottom insets, respectively).

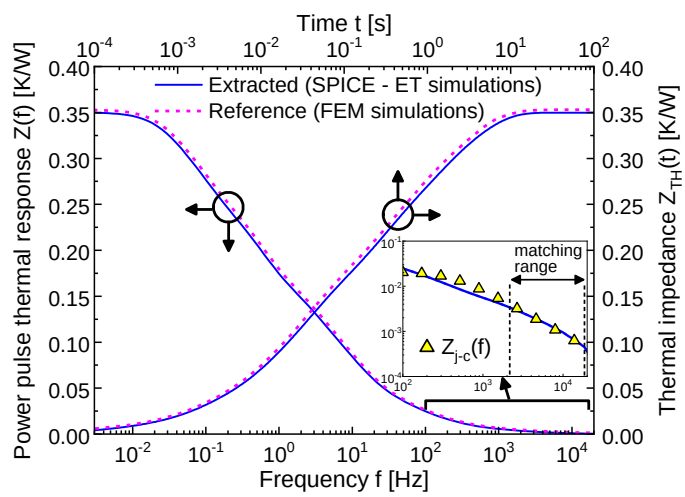

Fig. 5. (bottom-left axes) comparison between extracted (solid blue line) and reference (dashed magenta) $Z_{j\text{-}a}(f)$s. The inset highlights the matching range and the overlap between $Z_{j\text{-}a}(f)$ and $Z_{j\text{-}c}(f)$ (yellow triangles). (top-right axes) comparison between extracted and reference $Z_{TH,j\text{-}a}(t)$s.

V. Conclusions

This letter presents an innovative technique allowing the measurement of the overall junction-to-ambient self-heating thermal impedance of power devices mounted in a generic assembly and working under any environmental condition (*in-situ* extraction). The technique is applicable to any power semiconductor device without the need for temperature sensing; it only relies on the measurement of electrical signals and requires the knowledge of the junction-to-case thermal impedance of individual devices (i.e., not embedded in the assembly). The thermal impedance extraction can take from tens of minutes to few hours to be performed, depending on how slow the dynamic thermal response of the assembly is.

Since traditional methods do not allow *in-situ* measurements, their accuracy cannot be compared with that ensured by the proposed technique; therefore, a successful and unambiguous validation of the technique has been performed through the 'simulated experiments' strategy. The thermal behavior of a SiC-based VDMOS transistor embedded in a state-of-the-art multi-chip power module has been considered as a case-study. Electrothermal simulations in a SPICE-like software package have been used to emulate the experimental application of the proposed technique. An excellent assessment of the junction-to-ambient thermal impedance was obtained. Therefore, this technique proposes itself as a valid solution for the *in-situ* thermal characterization of power devices.

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