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# TRL-calibration Standards with Emphasis on Crosstalk Reduction

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**Abstract**— We present an innovative “shifted RF Pad” TRL on-wafer calibration kit to minimize the impact of crosstalk. The impact of the crosstalk in on-wafer measurement up to 330 GHz is observable by comparing results of DUTs obtained using the shifted and conventional RF pad calibration kit during calibration. Use of shifted RF pad structures shows improvement in measured DUT characteristics owing to reduced crosstalk. In addition, simulation results obtained using EM simulator, TCAD and SPICE models are employed to analyze the on-wafer measurement of DUTs.

**Index Terms**—S-parameter measurement, Semiconductor Devices, HBT, Sub-THz frequency, THz frequency, on-wafer TRL calibration, calibration kit structures design.

## I. INTRODUCTION

For accurate on-wafer S-parameter measurements beyond 110 GHz, on-wafer TRL calibration is the method of choice [1], [2]. In the on-wafer TRL calibration based on 8-term error model, all information about standards are not required; moreover, the DUT measurement environment is identical with respect to the calibration environment – unlike off-wafer ISS calibration. The drawback of TRL calibration is that in the associated error model the crosstalk is not accounted for [3]. Therefore, to improve the on-wafer TRL calibration prediction, minimization of crosstalk is important. Innovative calibration kit structures can be one possible way to minimize the crosstalk between port-1 to port-2 in the on-wafer measurements. So far, applying the open de-embedding after the on-wafer measurement of transistors allows the crosstalk to be partially corrected (see Fig. 1, removing of  $C_{12}$  contribution through de-embedding). However, there is no thorough method for crosstalk correction in standard calibration/de-embedding procedures. The crosstalk has the potential to alter the calibration error terms values and make them erroneous. Thus, our goal is to reduce crosstalk using innovative calibration kit design.

## II. STRUCTURE IMPLEMENTATION

With the aim of reducing crosstalk, we propose to misalign the access pads in TRL calibration structures so that the RF probes no longer face each other. To show the implementation of the misaligned access pads of one of the on-wafer TRL standards, the “thru” is shown in Fig. 2. The calibration kit with this shifted access pad uses a micro-strip line in the direction perpendicular to the conventional line as shown in Fig. 2. From the accesses to the central part of the line, the transition is made by a 45-degree bend similar to that of the

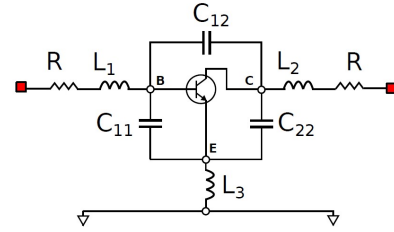


Fig. 1. Two step circuit model for short-open de-embedding of the HBT.

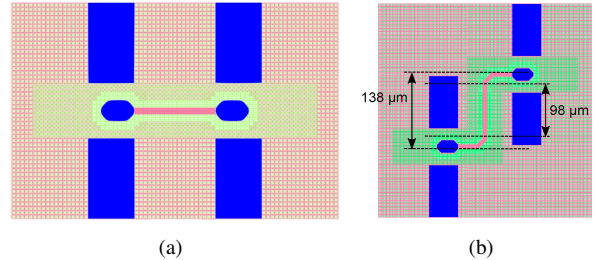


Fig. 2. Top view of the classic thru is shown in panel (a) and shifted thru is shown in panel (b). The dimensions in  $\mu\text{m}$  is indicated in shifted thru.

elementary mesh of the meander lines [4]. All measurements were made with 3 sets of Cascade Infinity probes up to 330 GHz.

## III. RESULTS AND DISCUSSION

### A. DUT: Passive Structure

First, the passive elements are studied, beginning with the transistor-open (i.e. open de-embedding structure). In Fig. 3, with shifted RF pads, a net improvement in the measurement on the coupling capacitance  $C_{12}$  is observed above 140 GHz along with improvement in  $C_{11}$ . No negative values of  $C_{12}$  are observed compared to the standard method above 140 GHz. However, it can be observed that the crosstalk is not completely corrected – a slight frequency dependence of  $C_{12}$  occurs – and it is different from one probe to another. Below 60 GHz, the coupling within the Cascade Infinity Probe appears to be weaker, but above that value a sudden drop in  $C_{12}$  indicates that significant coupling is occurring. This is correlated with a drop in the magnitude of  $S_{11}$  (not shown here) which can be explained by a coupling of the probe to the substrate [5]. Panel (c) and (d) of Fig. 3 shows the results of transistor-short measurements which shows improvement with use of shifted calibration kit. A better agreement with expected  $L_3$  value (intrinsic HFSS) using shifted calibration can be observed.

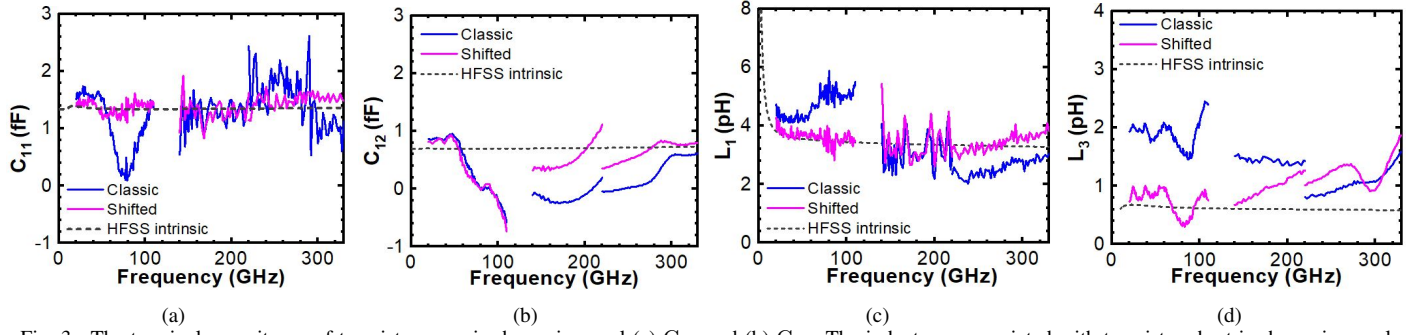


Fig. 3. The terminal capacitance of transistor-open is shown in panel (a)  $C_{11}$  and (b)  $C_{12}$ . The inductance associated with transistor-short is shown in panel (c) and (d). After application of on-wafer TRL on DUTs, the measurement reference plane is located near via descent. The ideal expected behavior of shown quantities are obtained by EM simulation of intrinsic part of the DUT.

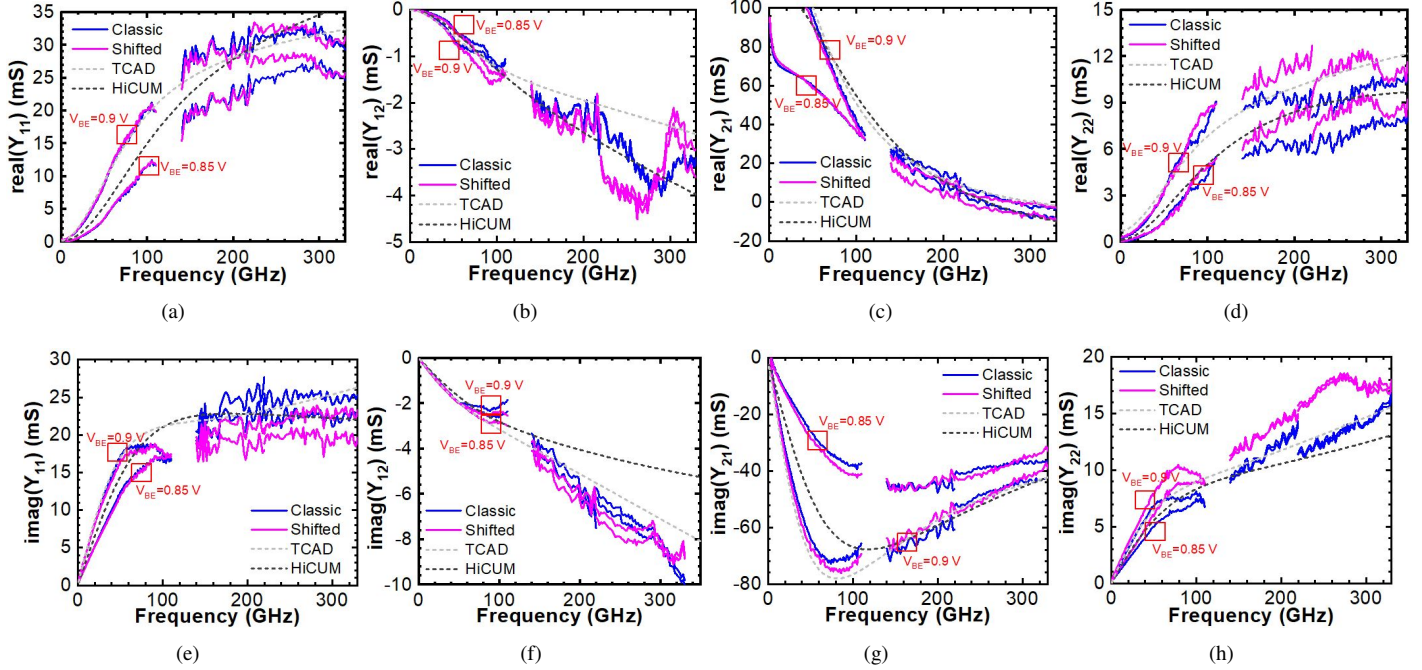


Fig. 4. Transistor Y-parameters at  $V_{BE} = 0.9, 0.85$  V and  $V_{CB} = 0.0$  V. TRL: reference plane is located near the via descent followed by a short-open de-embedding. TCAD and HiCUM simulation are given at  $V_{BE} = 0.9$  V and  $V_{CB} = 0.0$  V.

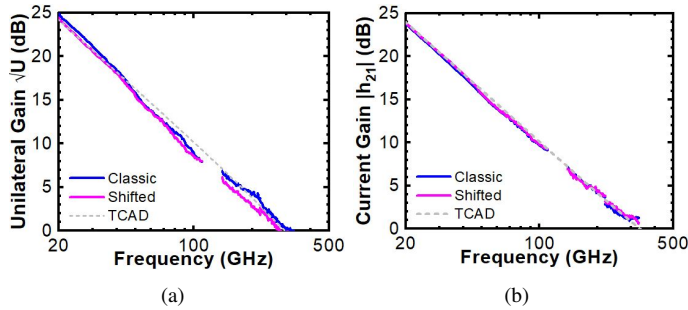


Fig. 5. Current gain  $h_{21}$  and Mason's gain  $U$  of the transistor at  $V_{BE} = 0.9$  V and  $V_{CB} = 0.0$  V are shown in panel (a) and (b), respectively. After applying the on-wafer TRL calibration, measurement reference plane is shifted near the descent of vias which is followed by a short-open de-embedding.

### B. DUT: Transistor

The second part is focused on on-wafer measurement of the SiGe HBT [6]. As stated earlier, on-wafer TRL using

8-term error model does not correct the crosstalk but the de-embedding step applied to the transistor partially corrects it. The results of transistor measurements in form of Y-parameters are presented in Fig. 4 after applying a short-open de-embedding. This figure summarizes on-wafer measurement data from the classic calibration kit and the shifted calibration kit. In addition, the results are compared to TCAD and HiCUM compact model results [7]. The figure shows a convergence of the results. Nevertheless, slight differences can be observed on the parameters  $\text{real}(Y_{22})$ ,  $\text{imag}(Y_{22})$  or  $\text{imag}(Y_{11})$ : in these cases, no clear trend emerges separating the data impacted by crosstalk (classic) and data without it (shifted). We therefore attribute these differences to measurement error. We can see that the  $\text{imag}(Y_{12})$  parameter, which is very sensitive to crosstalk, gives almost similar results regardless of the calibration method. These results suggest that despite the lack of crosstalk correction in TRL and thanks to Open

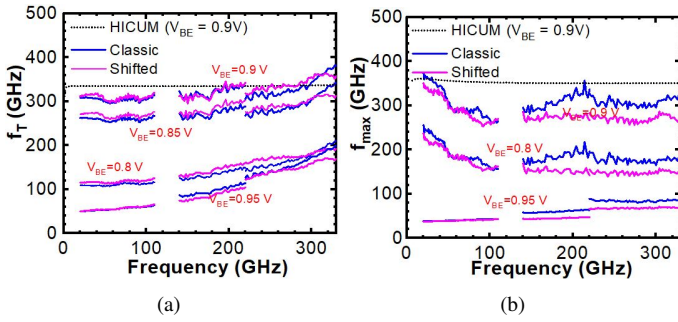


Fig. 6. (a) Transit frequency  $f_T$  and (b) maximum oscillation frequency  $f_{max}$  of the transistor at different base-emitter bias points and  $V_{CB} = 0.0$  V. After applying the on-wafer TRL calibration, measurement reference plane is shifted near the descent of vias which is followed by a short-open de-embedding.

de-embedding, the employment of standard TRL calibration structures provides correct results for on-wafer transistor measurements. Finally, Fig. 6 represents the two figures of merit extracted from  $h_{21}$  and  $U$  shown on Fig. 5, i.e.  $f_T$  and  $f_{max}$ . Nonetheless, a smoother behavior of  $f_{max}$  beyond 140 GHz can be observed applying the shifted calibration kit.

#### IV. CONCLUSION

Improvement in the on-wafer measurement is observed using the innovative on-wafer calibration kit on the coupling capacitance  $C_{12}$  of an open transistor and on the mutual inductance  $L_3$  of the short transistor, compared to a standard TRL approach. It has to be underlined that  $C_{12}$  measured with the TRL is still strongly marked by the probe-substrate coupling which hides the impact of crosstalk. In transistor measurements, the open de-embedding step partially corrects the crosstalk and the use of standard TRL calibration structures is still possible to obtain correct device results.

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