Charge sensing properties of monolithic CMOS pixel sensors fabricated in a 65 nm technology

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Abstract

In this work the initial performance studies of the first small monolithic pixel sensors dedicated to charged particle detection, called CE-65 , fabricated in the 65 nm TowerJazz Panasonic Semiconductor Company are presented. The tested prototypes comprise 64×32 matrices of square analog-output pixels with a pitch of 15 µm. The various pixel types explore several sensing node geometries and amplification schemes, which allows for various biasing voltage of the detection layer and hence depletion conditions and electric field shaping. Laboratory tests conducted with a ^{55}Fe source demonstrated that the CE-65 sensors reach equivalent noise charge in the 15 to 25 e^- range and excellent charge collection efficiencies. While substantial charge sharing among pixels is observed for a standard diode, modifying the diode geometry can mostly cancels such sharing. It is also shown that the depletion of the thin sensitive layer saturated after 5 V of bias voltage.

Keywords: monolithic CMOS pixel sensors, 65 nm TPSCo

1. Introduction

Monolithic CMOS pixel sensors have become a key technology for high energy physics detectors and recent roadmaps [1, 2] foresees their further development. Decreasing the CMOS process feature size is expected to enhance their overall performance, in terms of time and spatial resolutions, power dissipation and hit handling capabilities. CERN has organized the access to the 65 nm TowerJazz Panasonic Semiconductor Company (65 nm TPSCo) process, which is currently investigated by a large consortium as a potential technological candidate for the design of sensors to be used in a wide range of future detectors, the closest in time being the ALICE-ITS3 project [3].

This paper covers both a report on the design as well as the early characterization of several test pixel matrices implemented in sensor prototypes named CE-65 and fabricated during the first submission of the aforementioned consortium.

2. Design overview

The CE-65 detectors family was designed to explore the charge collection properties of the 65 nm TPSCo process. It consists of four different chips equipped with exactly the same readout-out electronics, but featuring two pixel pitches (15 and 25 µm) and various sensing node geometries. This work includes studies on two of them, called further basic and optimized diode, both in the pitch of 15 µm µm. The first variant implements a standard small collection well, being a reference sensing diode structure. The optimized diode is a modification following ideas introduced in [4] and targets the development of a lateral electric field at the pixel edges to speed-up charge collection.

2.1. Pixel matrix

A high level functional block diagram of the CE-65 chip is shown in Fig. 1. The chip is built of several major blocks: pixel matrix, column and row selectors, column buffers and output buffer. For the two variants reported in this paper the matrix size is 64×32 and consists of square pixels of 15 µm pitch.

The matrix is read out in rolling shutter mode with the configurable integration time down to 50 µs, translating to readout speed up to 40 MHz, although presented results have been obtained with the read-out clock frequency lowered to 10 MHz. The signal is digitized outside the chip by a fast 16-bit Analog-to-Digital Converter, defining the signal arbitrary digital unit (ADU).

2.2. Pixel architecture

Pixel matrix comprises of three sub-matrices that incorporate different in-pixel electronics architectures. The following input stages has been implement: AC coupled pre-amplifier

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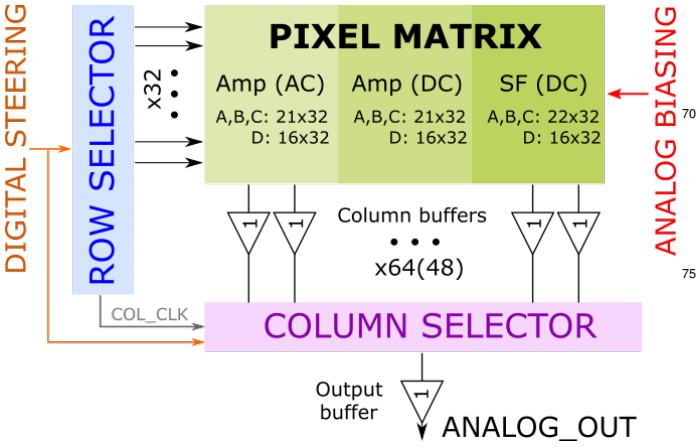

Figure 1: High level functional block diagram of CE-65 showing the arrangement of the different in-pixel electronics.

(AC-AMP), DC coupled pre-amplifier (DC-AMP) and DC coupled source follower (DC-SF).

The AC-AMP and DC-AMP in-pixel circuitry is shown on the left side in Fig. 2. In the AC-AMP the sensing node (reversely biased diode to substrate) is DC separated from the input stage of the readout electronics by the capacitance C_{SEP} (~ 10 fF). Thanks to that the voltage applied to the resetting diode (*HV_RESET*) is not limited by the electronics supply voltage and so much higher depletion voltages can be applied to the collection node. The second sub-matrix DC-AMP exploits the same in-pixel electronics, with the pre-amplifer followed by level shifter. The sensing node is directly connected to the gate of input transistor. Thus, the reset diode is no longer present and the input node voltage is determined by the pre-amplifier operating point. In the third approach shown on the right side in Fig. 2 a simple 3-T like Source-Follower architecture has been utilized. The reset diode has been implemented similarly as for AC-AMP , but the reset voltage is directly transferred to the gate of the input stage, so *VRESET* can not exceed the supply limits.

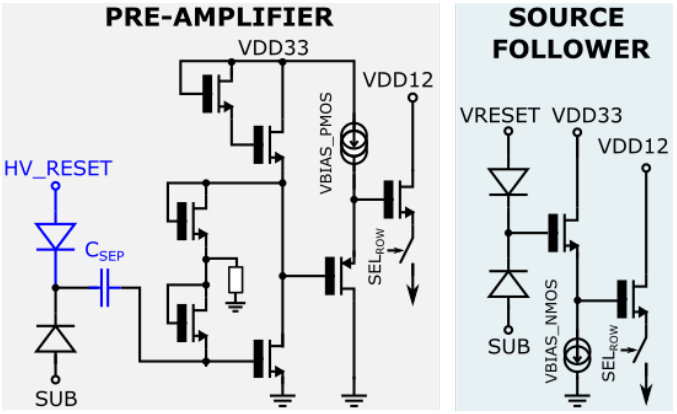

Figure 2: Schematic of source follower in-pixel circuitry (right) and DC preamplifier (left). AC preamplifier scheme is analogous with AC coupling added (blue).

3. Analysis results

The initial laboratory tests presented here are focused on comparing the basic and optimized diode performance. Measurements have been done with ^{55}Fe radioactive source at room temperature. The substrate back bias voltage was set to 0 V. Data samples have been processed so that the final signal value of each pixel is extracted from the difference between its raw amplitudes of two consecutive frames. Hits from impinging particles are identified from seed pixels with a signal over noise ratio larger than 10. Then clusters are build from the set of 3×3 pixels surrounding seed pixels.

3.1. Baseline and noise

The baseline and Equivalent Noise Charge (ENC) performance for both basic and optimized diodes are showing no significant differences as expected from the design, thus Fig. 3 presents plots only for the basic structure. The baseline map

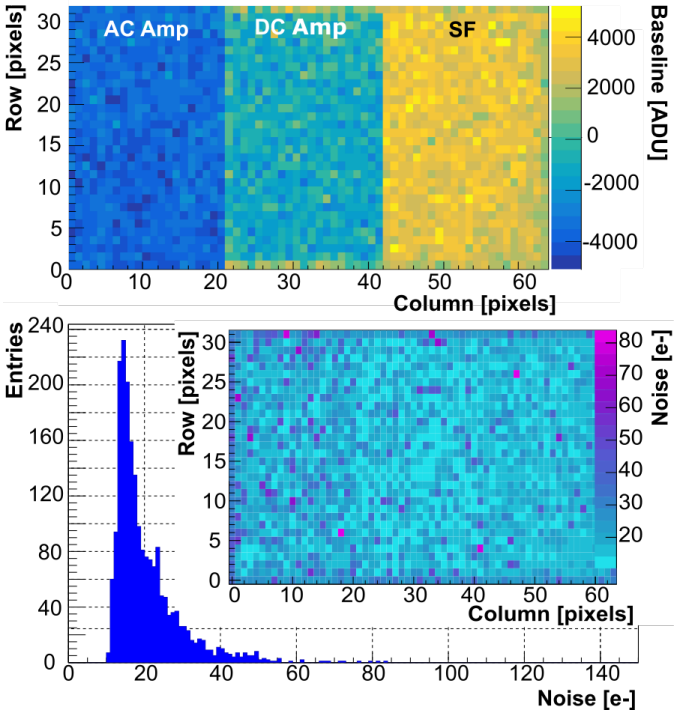

Figure 3: Baseline (top) and noise (bottom) distributions for the basic diode.

reveals clearly the sub-structure corresponding to different in-pixel circuits. However, among the submatrix the baseline is uniform, showing only small degradation towards the edges. ENC was calibrated based on the ^{55}Fe spectrum (see next subsection) and no significant differences are observed between submatrices. Preliminary results shows that the noise performance depends on the settings optimization and biasing condition but in most of the cases the measured ENC values are within the range of 15 to 25 e^-.

3.2. ^{55}Fe energy spectrum

The ^{55}Fe energy spectra is obtained from single pixel clusters, where the seed pixel signal almost saturates the cluster

signal. The spectra are shown for the DC-SF submatrix with optimized diode, but results obtained with other in-pixel circuitry are very similarly.

Fig. 4 displays the ^{55}Fe spectrum for one pixel selected from the SF-matrix. This approach allows to get rid of the pixel-to-pixel gain variation at the cost of a reduced statistics. A clear separation between the two characteristic ^{55}Fe X-rays lines Fe-K$_\alpha$ (5.90 keV) and Fe-K$_\beta$ (6.49 keV) is observed and confirms the low pixel noise as well as a promising energy resolution.

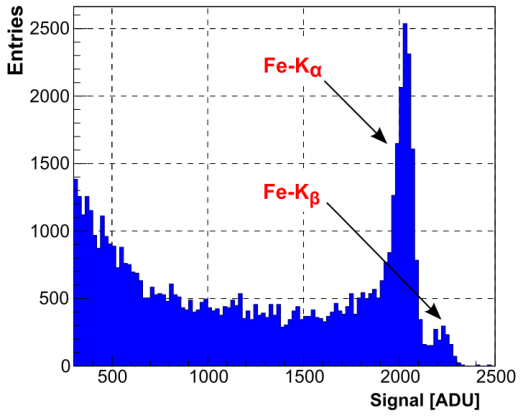

Figure 4: Iron source spectrum of single pixel clusters from one source follower pixel – optimized diode.

In Fig. 5, the single pixel cluster spectrum is presented for the whole DC-SF submatrix. The peaks are clearly smeared by the gain variations between pixels, but still both Fe-K$_\alpha$ and Fe-K$_\beta$ lines are distinguishable. However, the larger statistics reveals two additional energy lines: the Si-K$_\alpha$ (1.74 keV) and silicon escape peak (4.16 keV). The peak positions obtained from

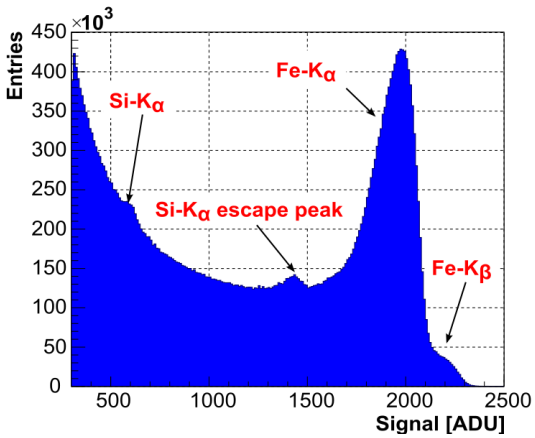

Figure 5: Iron source spectrum of single pixel clusters from whole DC-SF submatrix for optimized diode.

Fig. 5 allow to extract the detector energy calibration curve, depicted in Fig. 6. A high linearity is observed with an intercept close to zero.

3.3. Charge collection and sharing

Including all clusters in the ^{55}Fe data analysis allows additional observations. The comparison of the spectra obtained

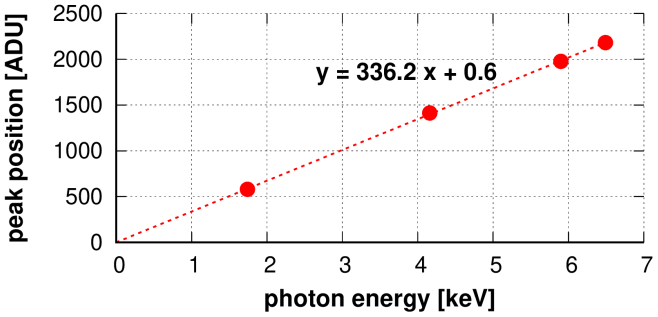

Figure 6: Calibration curve photon energy to ADU for DC-SF optimized diode, superimposed with a linear fit (dashed line).

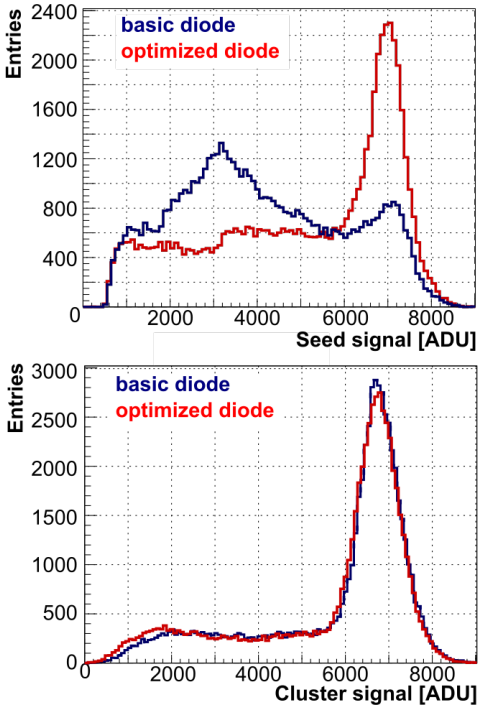

Figure 7: Basic (blue) and optimized (red) diode comparison: signal contribution from seed pixel (top) and total cluster signal (bottom).

with the basic and optimized diode geometries from the AC-AMP pixels with a bias voltage of 10 V, are shown in Fig 7, where the signal carried by the seed pixel only and the total cluster signal are plotted respectively.

For both collection nodes, the Si-K$_\alpha$ peak is easily visible at the end of the seed pixel signal distribution, corresponding to single pixel clusters. The total cluster signal is almost located at the Si-K$_\alpha$ position in ADU in both cases, indicating that the two diodes feature an excellent charge collection efficiency.

However, the seed pixel signal distributions display divergent features. For the optimized diode, both the cluster and seed pixel spectra look very similar with a single peak at the Si-K$_\alpha$ line location, indicating that the vast majority of the total charge is systematically collected by the seed pixel. In contrast for the basic diode, the seed pixel spectra features an additional broad peak with slightly less than half the total cluster signal. This is a strong sign that a significant fraction of the charges is shared

with neighbouring pixels.

A more quantitative comparison of the respective charge sharing observed with basic and optimized collection nodes is provided by the maps of the average pixel contribution to the total cluster signal, as presented in Fig 8. The significant charge sharing for the basic diode structure is confirmed, since the seed pixel collects in average slightly less than half of the total cluster signal. The design of the optimized diode, introduced to shape the sensor electric field towards the sensing electrodes, strongly suppressed the charge sharing and the seed pixel signal exceeds in average 80 % of the total cluster signal.

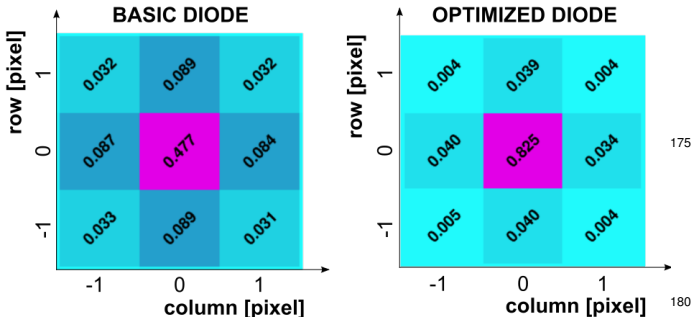

Figure 8: Average contribution to cluster signal for individual pixel in 3×3 clusters.

3.4. Depletion studies

Depletion of the sensor volume can be achieved by applying negative back bias voltage to the substrate or utilizing AC coupling and directly biasing collection node. Since applying substrate potential other than ground has been causing significant shift of electronics operating points and affecting the detector performance, for studying the development of the depletion in the sensitive layer, only the second method was exploited.

The Fe-K_α peak position with respect to the applied biasing voltage (for all investigated cases) is shown in Fig 9. Focusing on the results for AC-AMP , one observes that for both diode geometries depletion develops up to about 5 V and afterwards saturation is reached. At low polarization voltages the optimized structure shows higher amplitude degradation than basic one, corresponding to faster increase of the sensor capacitance. Marginal conclusions could be made for submatrices DC-AMP and DC-SF, for which biasing voltage is fixed by design. One could however notice, that the ratios between optimized and basic structures are preserved, as one would expect. The differences in gain between submatrices are also in agreement with the simulations, showing that DC-AMP have about 5 times higher gain than DC-SF while for the AC versions it is only 3 times higher (due to parasitics introduced by the separation capacitance).

4. Conclusions

This work presented the initial performance studies of the CE-65 monolithic CMOS sensors fabricated in the 65 nm TPSCo process, during the first submission organised by CERN

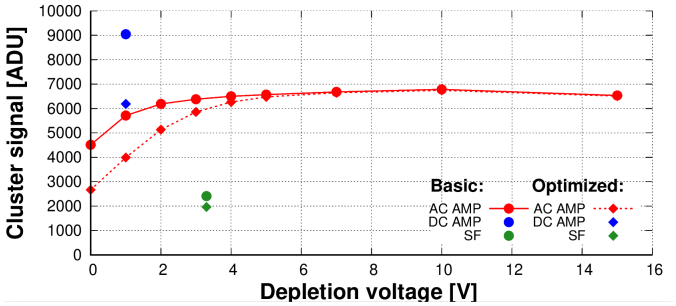

Figure 9: Evolution of Fe-K_α peak signal amplitude in function of the reverse bias voltage across the sensing node for the various CE-65 pixel structures.

to explore this technology. The tested CE-65 variants, with a 15 µm pixel pitch, displayed low noise operation and uniform pixel baseline among submatrices. Excellent charge collection efficiency was verified. While significant charge sharing has been measured with a basic collecting diode, an optimized structured was demonstrated to strongly mitigate this effect. As a consequence, the basic diode might be more appropriate for applications targeting outstanding spatial resolution. On the other hand, charges are more focused on a single collection node for the optimized structure, which is beneficial for the time resolution and tolerance against radiation generating displacement damages.

Complementary results characterizing CE-65 will come from irradiated samples and on-going test-beam analyses. In addition, further studies will be conducted with the next submission of CE-65 prototypes.

Acknowledgement

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