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Design of a test package for high voltage SiC diodes

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Abstract—A custom package for SiC diodes is presented. It is designed to accommodate "research-grade" devices (available in small quantities, with large variations in characteristics, and, in our case, poor topside metallisation). It allows testing of the diodes at high voltage (> 5 kV) and high current (600 A). The packaged diodes described here are used as a drop-in replacement for Si diode modules in a double-pulse setup.

The packaging design is based on a "sub-package" approach, to achieve high production yield and facilitate exchange of devices failing during the tests. Packaging technologies include silver sintering for the die attach and the use of an original die topside pressing system with spring probes. Experiments validate the concept of the package.

Index Terms—packaging, silicon carbide, diode, silver sintering

I. INTRODUCTION

Silicon Carbide (SiC) is a very attractive material to build high voltage power semiconductor devices. In particular, it features a wide bandgap (3.26 eV), and a critical electric field of 2 to 3 MV cm⁻¹ (vs. 1.1 eV and 0.11 to 0.22 MV cm⁻¹ for silicon – Si –, respectively) [1].

Regarding SiC power diodes, Schottky barrier diodes (and related structures such as the Merged Pin Schottky, MPS) are most often encountered up to 3.3 kV. Above this value, bipolar diode (PiN structures) offer better performance (in particular a lower dynamic resistance) [2]. Compared to their Si counterparts, SiC PiN diodes feature very good reverse recovery characteristics, such as lower losses, lower stored charge, and faster reverse recovery. This is explained by the fact that silicon carbide diodes have a thinner base region (for the same blocking voltage, thanks to the bandgap and critical field) and therefore a lower quantity of stored charge. Their use would allow higher frequency operation and lower losses in high voltage power electronics converters.

With the improvement in material quality and manufacturing processes, it becomes possible to produce the high voltage, high current PiN diode chips required in large power converters (such as the 10 kV/50 A chips used in this article). As with Si devices, many chips can then be assembled in power modules to further increase current capability. Here, we present the design, manufacturing and test of a diode module package rated at 600 A and 8 kV, dedicated to high

power pulse tests within a Si IGCT test setup [3]. Because this package is used as a drop-in replacement for a Si diode module, it shares the same footprint. Another key feature of this package is that it is intended to host devices with a low maturity level (typically research devices, designed in small batches and with possibly poor metallisation as it is the case here). This means that it is designed to maximise production yield and be processed in a lab environment.

To maximise yield, a "sub-package" approach is chosen: smaller packages, hosting 4 chips each, and rated at 200 A, are assembled and tested. Three of these sub-modules are then screwed together to form the full module. Also, chip contact is made using a spring-loaded mechanical pressing system. This makes for a reversible contact with the chip, can accommodate poor topside metal layers, and theoretically offers better current distribution and thermal buffering.

The diode dies and their characteristics used in this work are presented in section II. In section III, the packaging solution is presented, including the specific constraints to be considered, the package design and its manufacturing. Finally, test results (static characterisation and double-pulse waveforms) are presented in section IV.

II. THE 10 kV SiC PiN DIODES

The diodes dies used here are the result of previous research projects conducted by SuperGrid Institute and Laboratoire Ampère. This section summarises the results of these studies which are detailed in [4], [5].

The diodes are designed to withstand a blocking voltage of 10 kV and a forward current of 50 A. Die size is 10×10 mm², with a total thickness of 500 μ m. The low doped epitaxial layer is 110 μ m thick, n-doped at a level of 7×10^{14} cm⁻³. The theoretical breakdown voltage limit of this structure is 13.2 kV [4] (using the infinite plane-parallel junction model). The measured voltage breakdown of these devices is lower, owing to imperfections in the manufacturing process, and ranges from more than 11 kV down to less than 5 kV. A voltage map of a typical wafer is displayed in Fig. 1. Here, diodes with a breakdown voltage ranging from 2 to 8 kV are considered for packaging as they are considered to be good enough for some of the electrical tests to be conducted, and because a sufficient number of them is available (32 in total, plus some dummy chips for process setup).

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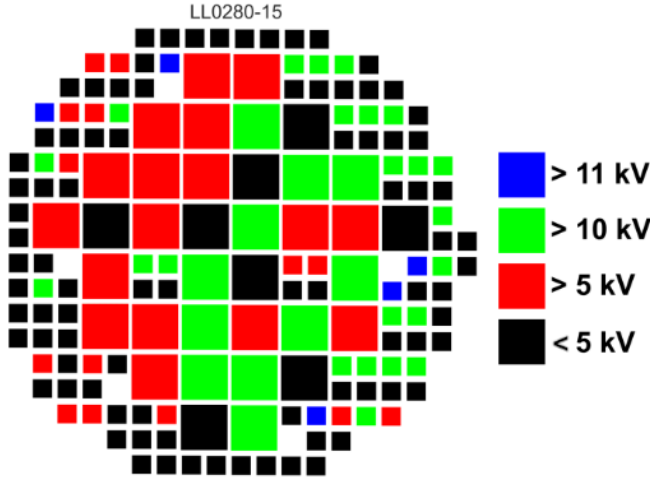


Fig. 1: Mapping of the breakdown voltage of one of the 4 inch wafers of the PiN diodes (the largest chips are $10 \times 10 \text{ mm}^2$) [4].

TABLE I: Diode Die Typical Parameters Values [4]

Characteristic	Typical Value
$V_F(50 \text{ A})$	4.98 V
$V_F(80 \text{ A})$	5.68 V
R_{on}	23.3 m Ω
$C_j(60 \text{ V})$	594 pF
$C_j(3 \text{ kV})$	82.2 pF

Some typical characteristics of the diodes are given in Tab I: forward voltage at 10 and 50 A; on-state resistance; junction capacitance at 60 V and 3 kV. The on-state resistance of 23.3 m Ω , for an active area of 59 mm 2 (die size without the edge terminations), corresponds to a resistivity of 13.8 m Ωcm^2 .

III. PACKAGING OF THE SiC DIES

A. Package ratings

1) *Voltage rating*: As described above, the dies hosted in this package have a breakdown voltage of up to 8 kV. For such voltage, the IEC 61800-5-1 standard indicates a clearance distance of 25 mm and a creepage distance of 32 mm (assuming pollution degree I, independently of the insulating material group).

2) *Current rating*: The nominal current of each die is 50 A. This value is used to design interconnects (busbars, spring contact probes, conductive layers in the PCB). However, because the modules are designed to be tested in a double pulse setup [3], joule heating is not a major concern.

3) *Temperature ratings*: The maximum case temperature considered is 120 $^{\circ}\text{C}$ (this temperature is applied externally during the double-pulse tests). This value has an impact on the selection of the materials, especially regarding the plastic case and encapsulant.

Self-heating of the dies is considered negligible (because of the double-pulse test sequence, assumed to be conducted with a very low duty cycle). As a consequence, the thermal resistance of the package is not required to be particularly low.

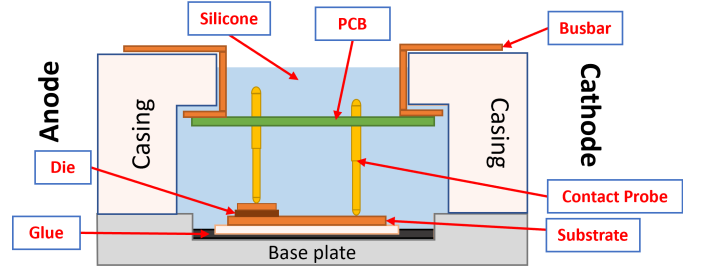


Fig. 2: Sub-package, sectional view, simplified schematic.

B. Package design

Because of limitations in the processing capability and in the number of available dies, and for mechanical reasons, the package concept implements the following approaches:

- The final package must have the same footprint (baseplate dimensions, mounting holes and terminals position) as the commercial diode module it replaces.
- Due to the small quantity of available diode dies, the large spread in their voltage ratings, and limited confidence in the packaging operation, the package is divided into sub-packages hosting a limited number of dies each (4) to increase yield. 3 Sub-packages are then assembled together with screws to form a complete 12-die package.
- Due to the poor condition of the top face of the diode dies, a local pressing system ensures connection on top of the dies using spring contact probes rather than classic bonding wires.

A simplified sectional view of a sub-package can be found in Fig. 2. This schematic only displays one diode die (out of 4) and one contact spring probe per side (instead of 4 per die on the anode side – 16 in total – and 14 on the cathode side). The different parts are detailed below.

1) *Ceramic substrate*: Aluminium Nitride (AlN) substrates from a previous project [6], [7] are used because they have proven to be able to withstand the maximum voltage level. Their dimensions are $32 \times 43 \text{ mm}^2$, with a thickness of 1 mm.

2) *Baseplate/substrate bonding*: Classically, solder is used to attach ceramic substrates to the baseplate [8]. However, this requires a suitable finish on the surfaces to be joined, and the solder reflow may cause stress on the components as well as oxidation. As a consequence, glueing is considered here because it is easier to implement (the downside being a higher thermal resistance compared to solder). A high conductivity, high-temperature epoxy glue (Duralco 133) is used.

3) *Baseplate*: Although little heat dissipation is expected from the power devices (because of the double-pulse operation, as opposed to continuous operation), metal is preferred for the base plate, as it offers good thermal conductivity, good mechanical strength and easy machinability. The base plate (Fig. 3) is machined in aluminium (6061-T6). A central cavity hosts the substrate to provide accurate positioning of the substrate with respect to the baseplate (required to ensure

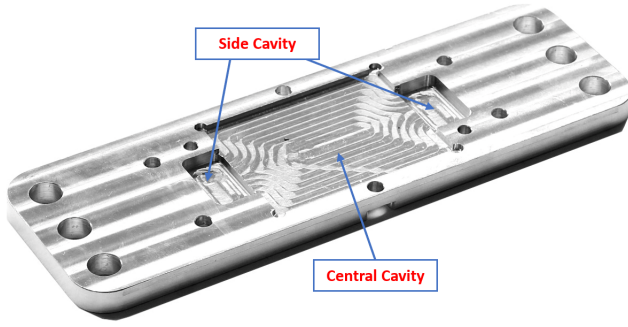
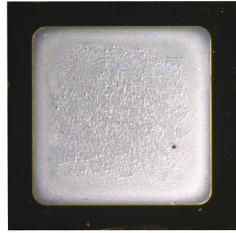
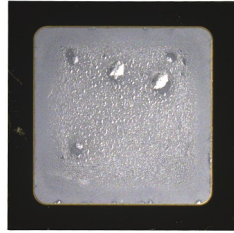


Fig. 3: Base plate.



(a) Diode a.



(b) Diode b.

Fig. 4: Typical top face (anode) of the diode dies.

alignment of the die pressing system, see below). Deeper side cavities serve as retention pools to absorb any excess glue.

4) *Die attach*: Silver sintering is chosen for die-attach as it allows good position control of the dies (because it is a solid-state process, dies cannot move around during sintering as it can be the case for soldering), which is important to maintain alignment with the die pressing system. Furthermore, this process had previously been used in our group [9]. The Ag-paste used here (mAgic PE338 ASP338-38 F150, Heraeus) is compatible with both the substrate (bare Cu) and the backside of the dies (Ag). A pressure-assisted process in a nitrogen atmosphere is used to ensure good adhesion and prevent oxidation of the substrates.

5) *Interconnects*: Because of processing issues, the dies used here exhibit defects in their topside metallisation (Ti/Al) (Fig. 4). The surface is irregular and presents blisters. Because of this, wire bonding is avoided to prevent any risk of tearing up the top metallisation. Instead, we use a custom Die Pressing System (DPS) for the top contact (Fig. 5).

The DPS comprises 4 spring contact probes soldered together on a copper platelet which is in contact with the diode die. The copper plate is small enough ($6 \times 6 \text{ mm}^2$) to fit within the top pad of the dies, with 1 mm margin on each side to allow for some misalignment. 4 individual DPS are then mounted on a Printed Circuit Board (PCB) together with 14 probes for direct contact with the substrate (cathode) (Fig. 6).

a) *Printed Circuit Board*: The contact probes are standard items with a small nominal current (reference S-2-J-10-G from Smiths Interconnect, nominal current: 3 A). However, in

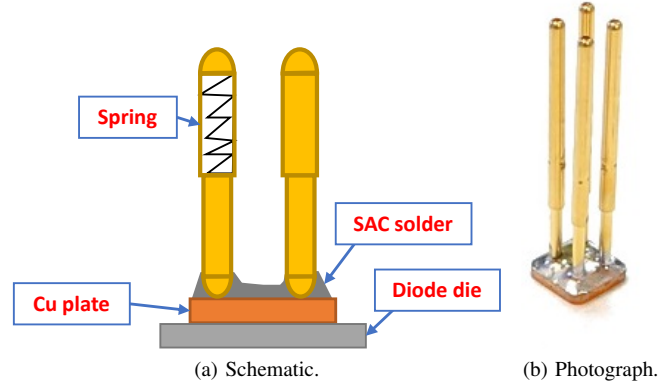


Fig. 5: Custom Die Pressing System (DPS).

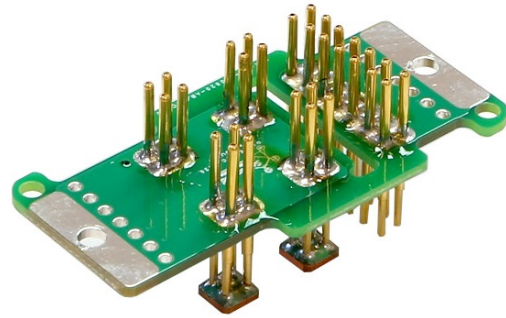


Fig. 6: Printed Circuit Board for one sub-package.

the DPS they are soldered onto a copper platelet (increasing their contact surface area) and used with a very low duty cycle. Tests conducted using a high power curve tracer (Iwatsu CS 5400) demonstrated that a single-die DPS could maintain contact up to at least 500 A (400 μs pulses).

6) *Case*: A review of insulating materials which can be used in the case of a power module is presented in [7]. Here, polycarbonate (PC) is selected, as it offers high glass transition temperature (140 $^{\circ}\text{C}$), high dielectric strength (at least 15 kV mm^{-1}), and mechanical strength (enabling, for example, to form strong threads in the casing). Furthermore, the case can be formed by machining commercially available PC blocks. Machining is much more suited to small production batches than injection moulding (a more common technique to manufacture cases which has high set-up costs and is suitable for mass-production),

As the power module is designed to operate in a clean environment (pollution degree 1), and because its external dimensions are dictated by those of the commercial power module it replaces, no special geometrical feature is required to increase creepage and clearance distances.

As depicted in Fig 2, the casing is used to apply pressure on the spring pins through the interconnected PCB. To ensure a homogeneous distribution of the compressive stress in the package and to avoid PCB bending, reinforcements (circled in

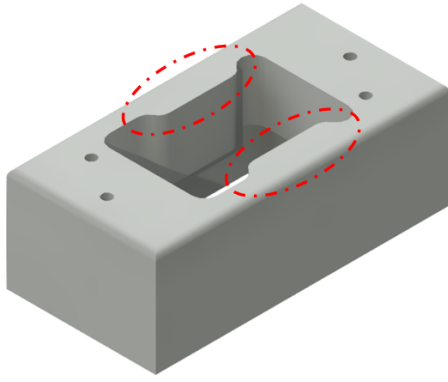


Fig. 7: Plastic casing design, 3D rendering.

red in Fig. 7) are added to the case design.

C. Packaging process

1) *Die attach*: Initially, the ceramic substrates (Rogers-Curamik) have copper (300 μm -thick) bonded on both sides: one side with a plain copper area (26 \times 38 mm² and one side with a more complex pattern. This pattern is removed using ferric chloride etching, leaving a flat surface. The remaining copper surface is cleaned to ensure good adhesion between the silver paste and the copper. First, the copper surface is deoxidised by exposing it to hydrochloric acid (HCl) vapor, followed by a rinse in deionized water and drying with a nitrogen blow nozzle (Fig. 8a).

After deoxidation of the substrate, it is placed in a custom jig (the same as shown in Fig. 8d), to allow for accurate positioning of a 100 μm -thick stainless-steel stencil (openings in the stencil are 100 μm smaller than the dimensions of the dies, to allow for some spreading of the paste). Ag-Paste is then printed (Fig. 8b) and dried (140 $^{\circ}\text{C}$, 20 min in N₂ atmosphere, using a Jipelec JetFirst oven, Fig. 8c).

For the actual sintering step, the substrate is replaced in the jig (Fig. 8d), and a second stencil (this time with an opening 200 μm wider than the size of the dies) is added on top using alignment rods. This stencil is used to position the dies (Fig. 8e). A polyimide sheet (to protect the dies from damage and distribute pressure during sintering) and an aluminium guide are then placed on top of the stack (Fig. 8f), also using the alignment rods. Finally, an aluminium "piston" is inserted into the guide (Fig. 8g).

The stack from Fig. 8g is then placed in the sintering oven (Jipelec JetFirst with a custom pressing fixture). Because of limitations (the pressing fixture can only apply up to 1.3 kN), the sintering pressure at die level cannot exceed \approx 3 MPa (i.e a force of 1.3 kN distributed over 4 1 cm² dies), much less than the value recommended by the paste manufacturer (10 to 30 MPa). To compensate for this low pressure, a high temperature (280 $^{\circ}\text{C}$) and a longer duration (10 min instead of 3–5 min) are applied. Here again, N₂ atmosphere is used to prevent oxidation of the substrate metallisation.

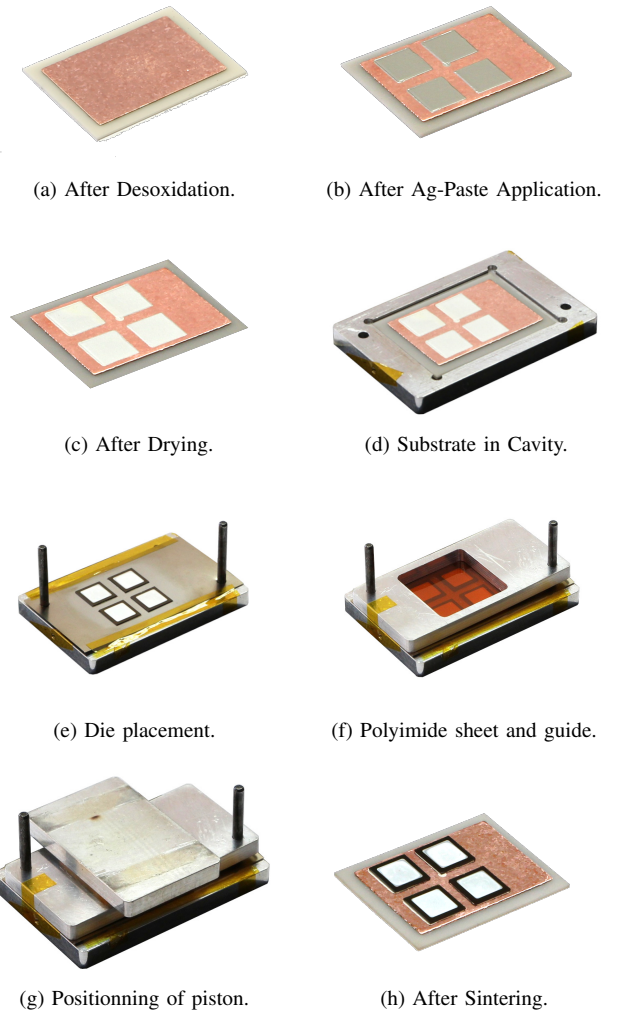


Fig. 8: Die attach process.

To ensure good bonding quality, a cleaning step is found to be required for the dies. Although no definitive conclusion could be reached regarding the nature of the problem (despite investigations using SEM, X-ray fluorescence, and Raman microscopy), we could not get a good attach using the dies directly (maximum shear strength of 1.6 MPa measured using an XYZTech Condor Sigma tester). Considering this adhesion issue could be related to organic contamination of the dies, plasma cleaning is investigated as recommended in [10]. Among some of the possible configurations of time and gases [11], tests show that 150 s O₂ plasma followed by 150 s Ar plasma (1000 sccm flow, 300 W power, and 100 mTorr pressure in both steps) provide good cleaning and no visible oxidation of the dies backside. Following this cleaning procedure, shear force is found to reach the limit of the test system, at 180 kgf, i.e. a shear strength of more than 18 N mm⁻².

2) *Assembly of the package*: 1 g of adhesive (Duralco 133) is placed in the central cavity of the baseplate. The substrate and its dies is then placed in the cavity, with 500 g weights

on top (to ensure good contact between the substrate and the baseplate, and to make sure the surface of the substrate is flush with that of the baseplate). The stack is then placed in an oven at 121 °C for 4 h for the adhesive to cure.

Individual DPS (contact probes + copper platelets) are assembled using SAC solder. A first custom jig ensures that the pins are perpendicular to the platelets and that they are accurately positioned. A second alignment jig maintains the 4 DPS and 14 pins in the PCB so they can be soldered.

Two alignment rods are then placed in the baseplate/substrate. The PCB/DPS assembly then slides along the rods. The case and busbars are placed on top, also using the rods for alignment. The case is screwed against the baseplate, putting the DPSs in compression. At this stage, the sub-package can be tested for forward conduction.

Finally encapsulation is performed: 2-part silicone gel (Sil-Gel 612, Wacker) is mixed (1:1), degassed under vacuum until no bubble can be seen (≈ 15 min). It is then poured in the case, degassed again (30 min), and placed in an oven at 100 °C for 15 min to cure. SilGel 612 insulation capability is quoted at 23 kV mm⁻¹, consistent with the requirements of the dies (their edge termination is 1 mm wide, and must withstand up to 8 kV).

Fig. 9a show the final sub-package. A total of 8 sub-package, numbered # 01 to 08, is built, each of them containing 4 dies with similar breakdown voltages (as explained in section II, dies breakdown voltages range from 2 to 8 kV). The complete package comprises 3 sub-packages, connected in parallel using copper parts, as shown in Fig. 9b. This package has 4 terminals (2 anodes, 2 cathodes), as the Si diode module it mimics.

IV. EXPERIMENTAL CHARACTERISATION OF THE SUB-PACKAGES

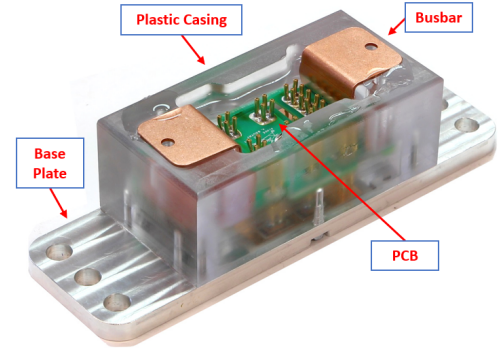
A. Static characteristics

The forward characteristics of each diode sub-package are displayed in Fig. 10a. The voltage drop of 2.7 V is consistent with [4], as is the dynamic resistance of 6.5 m Ω (at 200 A for a whole sub-package, i.e. 4 dies): in [4] the dynamic resistance of each diode die is found to be 24 m Ω . The resistance of the package can therefore be estimated to be a much lower value than the diode dies resistance value. Finally, sub-package # 04 is tested up to 1 kA (Iwatsu CS 5400, 400 μ s pulses) with no noticeable damage.

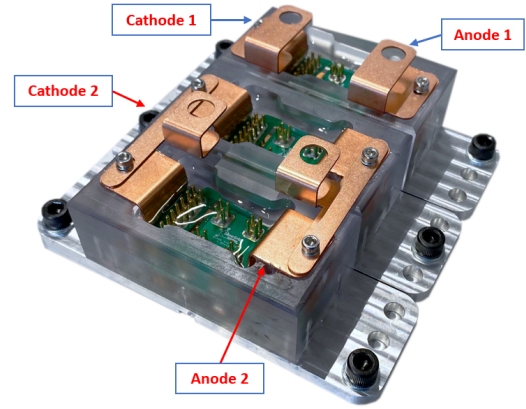
The reverse characteristics (Fig. 10b) exhibit some uncommon behaviours, which can probably be caused by the dies themselves (as discussed in section II, the dies used here did not meet the initial specifications of 10 kV. However, although the submodule tests can only be conducted up to 5 kV (maximum voltage of the Iwatsu CS 5400 tester), the package itself seems to behave satisfyingly (with a reverse current of less than 1 μ A for diodes # 06 and 07).

B. Double Pulse Experiment

The packaged diode is tested in a double-pulse test setup, together with a Si IGCT (more details on this IGCT study



(a) Sub-package.



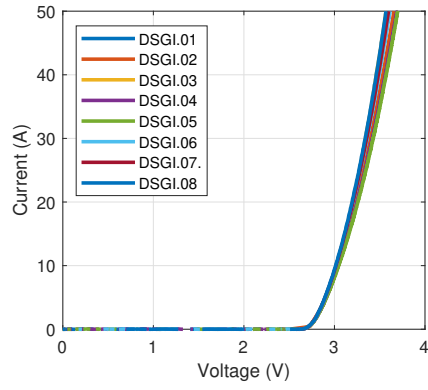
(b) Full diode package.

Fig. 9: Final Design of the diode package.

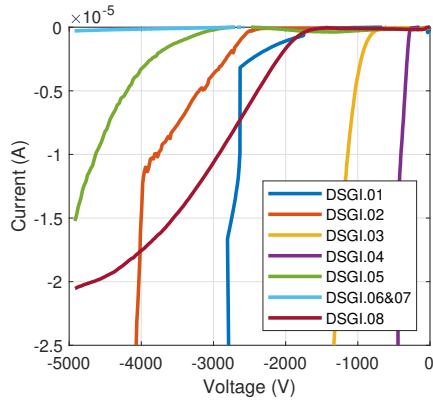
in [3]). The power circuit of the test setup is displayed in Fig. 11. Fig. 12 presents some pulse test results: turn-off at 2.8 kV/250 A (3 sub-packages in parallel), and turn-on under 600 V/500 A (1 sub-package only). This latter test is used to stress the diode at a high current density (211 A cm⁻² on average). Turn-off tests (Fig. 12a) show a noticeable reverse recovery (which is to be expected with PiN diodes). However, compared with Si diodes, it is much shorter and much smaller ($t_{rr} < 250$ ns; $I_{rr} \approx 200$ A). The package has also been successfully tested up to 120 °C baseplate temperature. Tests at higher current/voltage are currently underway.

V. CONCLUSION AND PERSPECTIVES

An original package, designed to host research-grade SiC PiN diodes, to be built in small quantities, and tested at high voltage/current, is presented here. It is formed of sub-packages that can be connected in parallel to theoretically reach a nominal current of 600 A and a breakdown voltage of more than 5 kV. Pressed die contact (DPS) is used as a workaround for defects in the dies' metallisation, but also as a way to provide reversible, high current interconnects. Detailed information is given regarding the concepts of the package as well as the manufacturing steps.



(a) Forward characteristic.



(b) Reverse characteristic.

Fig. 10: I-V characteristics of the 8 obtained sub-packages.

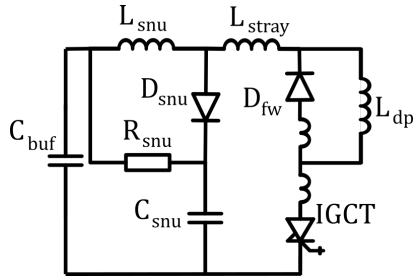
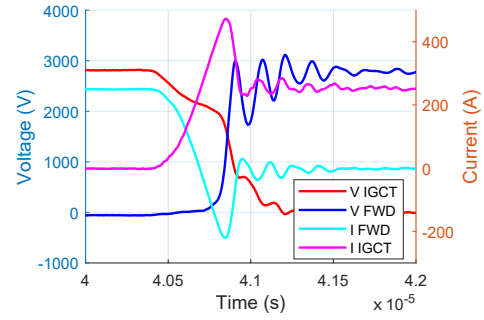


Fig. 11: Double test circuit diagram, including the diode under test (D_{fw}), an IGCT and its associated snubber ($L_{snu}, R_{snu}, C_{snu}, D_{snu}$). $C_{snu} = 5 \mu\text{F}$, $R_{snu} = 0.5 \text{ m}\Omega$, $L_{stray} = 450 \text{ nH}$, $C_{buf} = 0.8 \text{ mF}$.

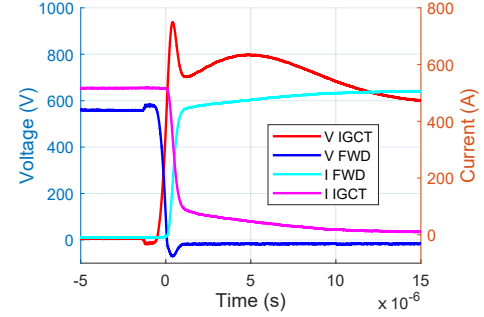
This package is then successfully tested (static characteristic, double pulse test) and used as a replacement for a commercial Si diode. Compared with standard packaging techniques, its main limitation is the thermal management, as only low-duty, double pulse testing is investigated here.

REFERENCES

[1] B. Jayant Baliga. *Fundamentals of Power Semiconductor Devices*. Springer, 2008.



(a) 2.8 kV/250 A diode turn-off, 25 °C. Full package (3 sub-packages).



(b) 600 V/500 A diode turn-on, 25 °C. One sub-package.

Fig. 12: Different waveforms obtained with the SiC packaged diode. V_{IGCT} , V_{FWD} : voltage across the IGCT and D_{fw} ; I_{IGCT} , I_{FWD} : current through the IGCT and D_{fw} .

[2] José Millán, Philippe Godignon, Xavier Perpiñà, Amador Pérez-Tomás, and José Rebollo. A Survey of Wide Bandgap Power Semiconductor Devices. *IEEE transactions on Power Electronics*, 29(5):2155–2163, May 2014.

[3] Arthur Boutry. *Theoretical and experimental evaluation of the Integrated gate-commutated thyristor (IGCT) as a switch for Modular Multi Level Converters (MMC)*. Theses, INSA Lyon, December 2021.

[4] Asllani, Morel, Phung, and Planson. 10 kV silicon carbide PiN diodes—from design to packaged component characterization. *Energies*, 12(23):4566, nov 2019.

[5] Besar Asllani, Dominique Planson, Pascal Bevilacqua, Jean Baptiste Fonder, Beverley Choucouteu, Hervé Morel, and Luong Viet Phung. Advanced electrical characterisation of high voltage 4h-SiC PiN diodes. *Materials Science Forum*, 963:567–571, jul 2019.

[6] Hugo Reynes, Cyril Buttay, and Herve Morel. Protruding ceramic substrates for high voltage packaging of wide bandgap semiconductors. In *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. IEEE, oct 2017.

[7] Hugo Reynes. *Conception d'un module électronique de puissance pour application haute tension*. PhD thesis, INSA Lyon, 2018.

[8] William W. Sheng and Ronald P. Colino. *Power Electronic Modules: Design and Manufacture*. CRC, 1st edition, June 2004.

[9] Amandine Masson, Wissam Sabbah, Raphaël Riva, Cyril Buttay, Stephane Azzopardi, Hervé Morel, Dominique Planson, and Régis Meuret. Die attach using silver sintering. practical implementation and analysis. *European Journal of Electrical Engineering*, 16(3-4):293–305, aug 2013.

[10] STMicroelectronics. Recommendation for die sintering with Ag finishing. Technical report, STMicroelectronics, 2020.

[11] Leong Ching Wai, Wen Wei Seit, Eric Phua Jian Rong, Mian Zhi Ding, Vempati Srinivasa Rao, and Daniel Rhee MinWoo. Study on silver sintered die attach material with different metal surfaces for high temperature and high pressure (300°C/30kpsi) applications. In *2013 IEEE 15th Electronics Packaging Technology Conference (EPTC 2013)*. IEEE, dec 2013.