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A CMOS Compatible Thermoelectric Device made of Crystalline Silicon Membranes with Nanopores

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Abstract

Herein, we report the use of nanostructured crystalline silicon as a thermoelectric material and its integration into thermoelectric devices. The proof-of-concept relies on the partial suppression of lattice thermal conduction by introducing pores with dimensions scaling between the electron mean free path and the phonon mean free path. In other words, we artificially aimed at the well-known “electron crystal and phonon glass” trade-off targeted in thermoelectricity. The devices were fabricated using CMOS-compatible processes and exhibited power generation up to 5.5mW/cm² under a temperature difference of 280 K. These numbers demonstrate the capability to power autonomous devices with environmental heat sources using silicon chips of centimeter square dimensions. We also report the possibility of using the developed devices for integrated thermoelectric cooling.

Keywords: Silicon, Silicon-on-Insulator, CMOS, Thermoelectricity, Energy Harvesting, Phonon Scattering, Peltier cooling

Introduction

The blooming of the Internet of Things (IoT) and wireless autonomous sensor nodes has been delayed owing to the lack of reliable, safe, and low-cost energy sources [1]. Thermoelectric generators (TEG) have these advantages [2]. Silicon has the advantages of being abundant, non-toxic. Numerous facilities and CMOS technological processes for low-cost mass production exist for silicon while conventional thermoelectric materials (Bi, Sb, Te, Pb alloys) are far less developed. The research for Si-based TEG [3–5] has attracted increasing interest. However, silicon is an inefficient thermoelectric material owing to its high thermal conductivity of 150W/mK [6], whereas bismuth telluride alloys exhibit hundred times lower conductivity (~1.5W/mK) [7]. Moreover, the dimensionless figure of merit zT which characterizes the thermoelectric efficiency, is approximately 1 for Bi₂Te₃ at room temperature [8] and below 0.01 for bulk silicon [9]. At temperature T , zT is defined as

$$zT = \frac{\sigma \cdot S^2}{\kappa} \cdot T \quad (1)$$

σ , S and κ being the electrical conductivity, Seebeck coefficient, and thermal conductivity, respectively. The thermal conductivity accounts for the performance gap between the Si and Bi₂Te₃ micro-TEGs (Figure 1). Efforts are oriented towards cutting the phonon part of heat transport, which is the dominant contribution in semiconductors [10]. The phonon contribution is evaluated in the diffusive regime

as

$$\kappa_{ph} = \frac{c \cdot v \cdot \Lambda}{3} \quad (2)$$

where c , v and Λ are the specific heat, group velocity (average elastic wave velocity), and phonon mean free path, respectively. The heat capacity depends on the atomic density of the material, and thus cannot be modified. Group velocity modulation would require modifying the atomic structure of the crystal to induce coherent effects, unexpected at room temperature. Suppression of the lattice contribution can be achieved by reducing the phonon mean free path through diffusion through artificial defects and boundaries. This process can be obtained by the use of thin films [6], nanowires [11], the addition of impurities or polycrystalline silicon [12], and silicon nanopatterning [13,14]. Previous studies have shown that holey structures can further decrease the thermal conductivity with a minor impact on the electrical conductivity [15]. The combination of thin films and phonon scattering by nanometric pores lowers the thermal conductivity to 34 W/mK [13] and even to 2 W/mK [14,15] depending on the specific design. The first value was for samples with partially perforated patterns and thus constitutes a conservative hypothesis. The lowest value represents the amorphous limit of silicon thermal conductivity [16], which makes it a very ambitious limit that can probably be obtained only at the cost of substantial material defects.

In addition to reducing the thermal conductivity of silicon, research in recent years has dealt with the development of silicon-based (mainly polysilicon and silicon nanowires) thermoelectric micro-harvesters or generators. Figure 1 reports the main results [3,5,17–20] from state-of-art silicon-based micro-harvesters with respect to state-of-art bismuth telluride harvesters [21]. The silicon TEGs exhibit output power in the $\mu\text{W}/\text{cm}^2$ range against mW/cm^2 for vertical Bi₂Te₃ [21,22] TEG for same temperature differences. The thermoelectric properties of these materials primarily explain this gap.

In this study, we demonstrate a proof-of-concept thermoelectric device using patterned silicon membranes. The device consists of a silicon frame equipped with planar configuration thermopiles. For the sake of demonstration, the hot source is emulated by resistive heaters. A thermoelectric converter could be made from this device, by adding a silicon cap, mounted onto the hot source and etched in order to distribute the heat flow at the locations of the resistive heaters. An example of such configuration is given by Ziouche et al. [17]. In the following section, we present the fabrication process and discuss its performance with respect to plain membranes devices and especially according to the state-of-

art presented in Figure 1. We also mention modeling results reported in [23] that suggests that the performance of PE Si-based TEG compares favorably with that of Bi₂Te₃ based TEG when the heat flow is not controlled by a bulky heat sink (*i.e.*, in the specific use case for IoT, which is deeply constrained by compactness and low form factor requirements).

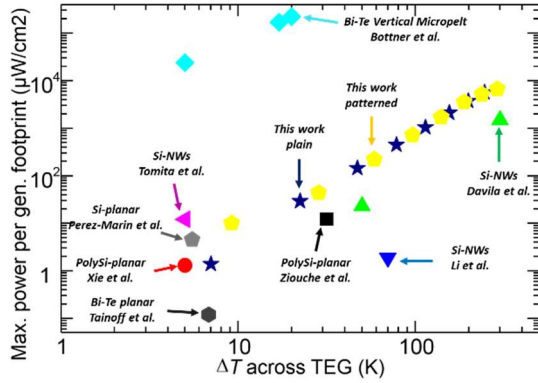


Figure 1: State-of-art micro-harvesters' maximum output power per footprint area as a function of the temperature difference across the generator [3,5,17,19–22,24]

Experimental Methods

The devices were fabricated from SOI wafers using the conventional CMOS processes (Figure 2). The process is mainly based on previous work carried out to reduce the thermal conductivity of silicon by means of silicon thinning coupled to pore lattices [13,25]. The departure point is an SOI wafer with a 70 nm thick active layer (a) high-resolution e-beam lithography and Cl₂/Ar reactive ion etching (RIE) was performed to define the pore patterns (b). Then, the silicon is *p*-boron and *n*-phosphorus doped by ion implantation with a target of 10¹⁹ cm⁻³. Sheet resistivity measurements give 2.34×10⁻² Ω.cm and 6.38×10⁻³ Ω.cm for *p* and *n*-type respectively corresponding to an effective doping level of 6×10¹⁸ cm⁻³ and 9×10¹⁸ cm⁻³ (c). A low-stress silicon nitride was then deposited (d) to insulate the thermopiles from the central platinum resistive heater emulating the devices' hot source. Silicon nitride also aims at improving the mechanical strength of structures. Cavities are etched around the thermopiles as apertures for subsequent suspension (e). Metallic sensors and leads are obtained by platinum and gold evaporation (f). Metallic sensors and leads are obtained by platinum and gold evaporation (f). Metallic sensors and leads are obtained by platinum and gold evaporation (f).

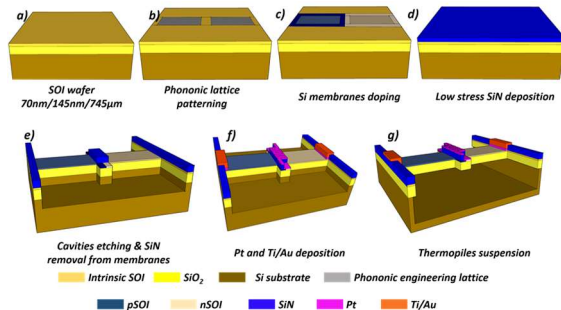


Figure 2: Patterned silicon membranes thermoelectric devices' fabrication process.

Before metallization, the Si membranes a thermal oxide layer is grown to protect them from xenon-difluoride (XeF₂) etching (g). This last step of the process ensures thermal insulation of the Si membranes from the wafer. The device

was made of five thermopiles connected electrically in series and thermally in parallel (Figure 3-a). It was equipped with four pads to supply heating power and I-V measurements. Each thermopile (50µm long, 10µm wide and 205 nm thick) was composed of two *n*- and *p*-doped membranes, as shown in Figure. 3-b. The membrane stack is composed of the following components: 15nm SiO₂/62 nm Si/ 145 nm SiO₂. At the center, two platinum straps electrically short-circuit the *p*-*n* boundary (Figure 3-c). Platinum resistive heaters were deposited over the silicon nitride layer to avoid current leakage (Figure 3-b, c, d). On half of the devices, a lattice of 40 nm diameter pores and 100 nm pitch patterns was etched (Figure 3-e, f). These dimensions are chosen as a compromise between technological capabilities and minimizing the pitch size, neck size and maximizing the porosity in order to enhance the effect of thermal conductivity reduction [26,27]. The electrical continuity of the thermopiles was ensured using a metallic Pt strap between adjacent thermopiles.

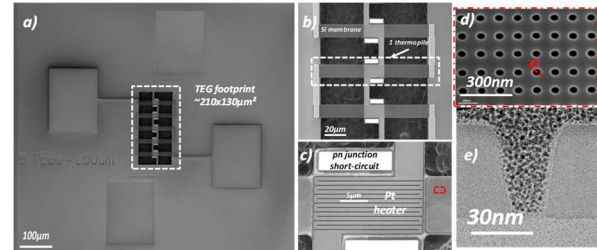


Figure 3: (a) Scanning Electron Micrograph of a thermoelectric device made of 5 suspended thermopiles. (b) Close-up view of three thermopiles. (c) Platinum resistive heater. (d) Detail of the membranes pore patterns. (e) Cross section Transmission Electron Micrograph of the membrane.

The devices were studied both in terms of energy harvesting under a temperature gradient (Seebeck effect) and thermoelectric cooling when current flows across thermopiles (Peltier effect). Regarding Seebeck effect, the devices were characterized by a thermo-resistive methodology [14,15,28]. Indeed, Pt is known to have a significant temperature-dependent coefficient of resistance $\alpha=2.5 \times 10^{-3}/K$ in this case. This value differs from the bulk value because the Pt film is 30 nm thin and was systematically measured for each sample before the thermometry measurement. Infrared imaging (Figure 4-b) demonstrates the functionality of these heaters. The electrical power (P_H) produced at the center of the thermopiles is converted into heat flux (Q_H) and, in the first approximation, equally diffuses across the thermopiles (Figure 4-c) to the cold ends. Measurements were performed under vacuum to eliminate conducto-convective fluxes on in air and guide heat flux into the membranes. During the measurements, the frame wafer was maintained at a constant temperature of 25°C. Because the thermopiles were etched from the SOI substrate, efficient heat coupling was achieved at the cold ends. This assumption is supported by the high thermal conductance of the frame wafer and the infrared thermometry. It follows that the cold sides of the membranes are at the same temperature as the substrate, which was verified by IR imaging. The characterization was performed in two steps: i) by variation of the Pt heating current, a $V-\Delta T$ characteristic enables measurement of the Seebeck voltage, and ii) at a constant Pt heating current, the I-V curves characterize the power generation. To capture the Peltier effect, a current was applied to the thermopiles and imaged using IR thermometry in ambient air. This electrical current should produce heat absorption or generation at the center of the thermopiles depending on its direction.

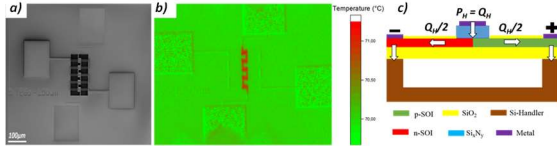


Figure 4: SEM view of a 5 thermopiles device (a) IR imaging (performed in ambient air) after Pt resistive serpentine voltage bias (b) and cross-sectional scheme of a thermopile.

Results & Discussions

First, the heaters are calibrated in order to achieve a given temperature difference. We note that patterned thermopiles sustain a higher temperature difference for a given amount of heating power. There is a two-fold interest in this result. First, the use of a thin-film planar device significantly increases the thermal resistance to approximately 10^6K/W . This value governs the temperature difference in a TEG and should be compared to the typical Bi_2Te_3 TE legs of 10^4K/W [22] (10^2K/W for bulk Si with typical leg dimensions of $1 \times 1 \times 5 \text{ mm}^3$). In addition to the thin-film geometry, patterning enhances thermal resistance by a factor of 1.8. The reduction in thermal conductivity [13,14] with patterning explains this gain. Figure 5 shows the Seebeck voltage generated as a function of temperature difference across the thermopiles. Again, characterization was performed on plain and patterned samples. As expected, the Seebeck voltage increased linearly with the temperature gradient. Furthermore, the plain devices produced an electrical voltage close to the value expected by a Finite Element Method (FEM) software using a Seebeck coefficient $S_p - S_n = 545 \mu\text{V/K}$. The FEM cannot model the physical effect of pore patterning, therefore, the modeling results can only be compared to those of plain devices. The measurements showed Seebeck coefficients per thermopile of $570 \mu\text{V/K}$ and $590 \mu\text{V/K}$ for the plain devices and $820 \mu\text{V/K}$ and $840 \mu\text{V/K}$ for the patterned devices.

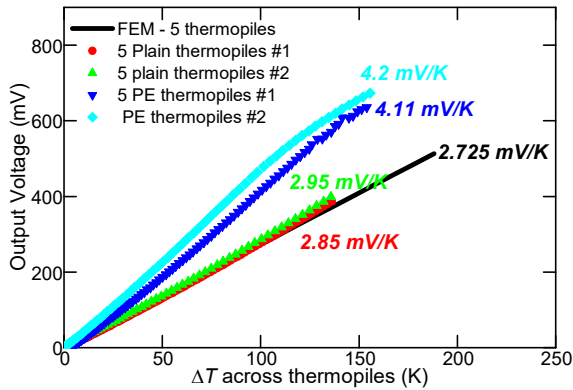


Figure 5: 5 plain thermopiles (black squares & red dots) and 5 patterned thermopiles (green & blue triangles) output voltage with respect to the temperature difference across thermopiles

Power generation was investigated by studying the I-V characteristics of the thermopiles as a function of the applied temperature difference. Figures 6-a and -b report respectively the plain and patterned thermopiles I-V curves for ΔT from 0 to 282 K temperature differences, respectively. Typical thermoelectric characteristics were obtained, and a generator regime ($IV < 0$) was observed. The electrical current is given by

$$I = \frac{V_{Gbias} - V_S(\Delta T)}{R_G} \quad (3)$$

where V_{Gbias} is the thermopile bias voltage, $V_S(\Delta T)$ is the Seebeck voltage at a given temperature difference across the

thermopiles, and R_G is the devices' internal resistance, which is approximately $130 \text{k}\Omega$ and $260 \text{k}\Omega$ for plain and patterned thermopiles, respectively. This increase of electrical resistivity with patterning is confirmed by independent four-probe resistivity Van-der-Pauw measurements on dedicated areas of the wafer. Because the dimensions of the patterned lattice are much larger than the typical electron mean free path (a few nanometers [29]), it is unlikely that the resistivity is significantly affected by the pore patterns. We note that the change of resistivity between plain and patterned membranes can be evaluated as an effective change of the dopant concentration. (see Suppl. Material) A concomitant increase in the Seebeck coefficient and resistivity is then expected from the Mott relation [30,31] which order of magnitude is quite in agreement with the 1.4 times increase of the Seebeck coefficient.

From the I-V curves, we calculated the output power corresponding in the generation regime and extracted the maximum output power. Figures 6-c and -d present the maximum output power densities with respect to the temperature difference across the thermopiles (Figure 6-c) and according to the heating power of the Pt heaters (Figure 6-d). Figure 6-c shows that compared to the temperature difference across the thermopiles, the plain and patterned devices exhibit comparable performance. This observation reflects that the Seebeck effect is enhanced by patterning while the electrical resistance is increased, leading to a constant power factor. The maximum output power is given by (4), and at a given temperature difference, it depends only on the Seebeck coefficient and electrical resistance.

$$P_{MAX} = \frac{V^2}{4 * R_G} = \frac{S^2 * \Delta T^2}{4 * R_G} \quad (4)$$

where S and ΔT are the Seebeck coefficient and the temperature difference across the thermopiles, respectively. Globally, patterning would therefore have no impact on generator performance. Figure 6-c also shows a comparison between the measurements and FEM modeling showing perfect agreement with the measurements.

The patterned and plain devices were compared again, but this time with respect to the heating power of the Pt heaters (Figure 6-d). Under these conditions, we can notice that, compared to the heating power, patterned devices exhibit better performance than plain thermopiles. This highlights the benefits of thermal gradient management for thermoelectric harvesting. Indeed, (5) gives the maximum output power, which depends not only on the Seebeck coefficient and electrical resistance that compensate each other, but also on the temperature difference across the thermopiles. The temperature difference across the PE thermopiles was higher for a given heating power (see Suppl. Material).

$$P_{MAX} = \frac{V^2}{4 * R_G} = \frac{S^2 * Q^2 * r_{TEG}^2}{4 * R_G} \quad (5)$$

$$\Delta T = Q * r_{TEG}$$

Q and r_{TEG} are the heat gradient across the thermopiles (or heating power) and the thermal resistance of the thermopiles, respectively. Figures 6-c and -d highlight then the fact that the main benefit of pore patterning is better thermal gradient management, especially owing to a thermal conductivity reduction [13–15]. The gap between the patterned and plain thermopiles in figure 6-d can be improved with a better patterns design. From the range of output power, we can

easily imagine the use of a few cm^2 of such generators to supply power to autonomous sensor nodes [32]. Moreover, compared to the state-of-the-art (Figure 1), with respect to the silicon-based thermoelectric microharvesters, the developed devices mainly exhibit better performance for the same temperature differences. The material crystalline structure and harvester architectures can explain this difference in

performance. Polysilicon has lower electrical resistivity than crystalline silicon. Low-dimensionality systems, such as silicon nanowires, feature improved thermoelectric efficiency. Tomita et al. [19] managed to develop Si nanowire (NWs)-based harvesters exhibiting state-of-the-art performance.

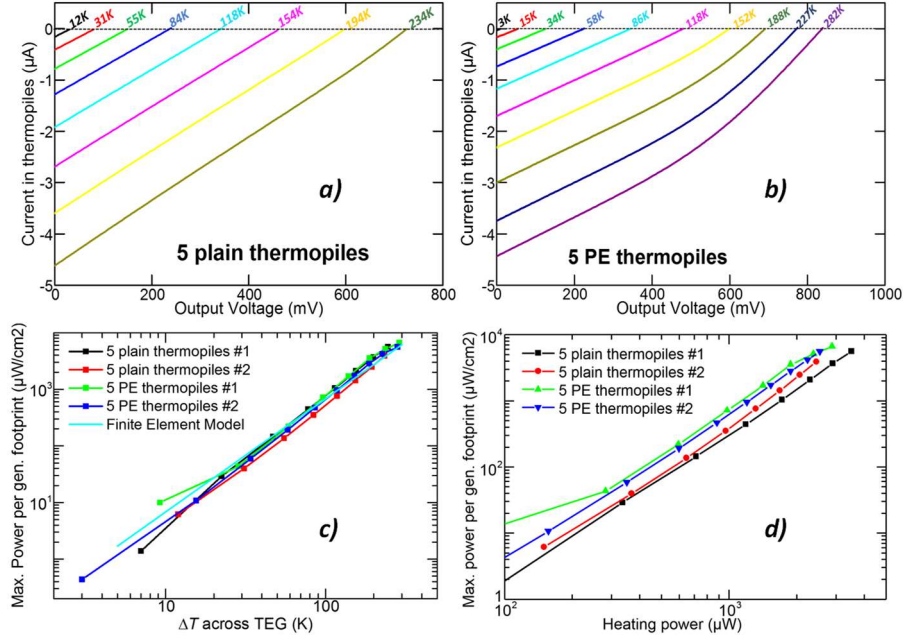


Figure 6: 5 plain (a) and PE (b) thermopiles I-V curves with temperature gradient and measured maximum output power density versus temperature difference across thermopiles (c) and versus the Pt heaters' heating power (d)

As expected, the performance of the vertical bismuth telluride micro harvesters [21] is four orders over the developed devices. This is related to several causes. First, bismuth telluride legs feature lower electrical resistance, less than 1Ω , against tens of $\text{k}\Omega$ per leg for the developed devices. Secondly, the bulk Bi_2Te_3 parts exhibit low thermal conductivity. However, these performances are greatly diminished when the heat cooling capacity is low. This cooling capacity is quantified by an effective conducto-convective transfer rate h ($\text{W}/\text{m}^2/\text{K}$) (see Suppl. Material).

The characterization of the devices is completed with the observation of Peltier cooling. Figure 7 shows infrared (IR) images of a device biased at $\pm 7.5\text{V}$. The left picture represents the result of current propagation from p to n end, and the right picture represents the current propagation from n to p end. The figure shows that, depending on the current direction, heat generation or absorption is observed at the center of the thermopiles, which is characteristic of the Peltier effect.

Conclusion

In summary, a phonon scattering approach was used to reduce the heat conduction in crystalline silicon thin membranes. The fabrication and demonstration of thermoelectric conversion using crystalline silicon was shown. The device principle relies on better use of the available thermal difference in a planar thin membrane architecture and additional pore patterning. The results

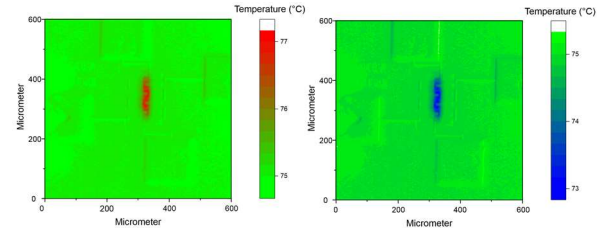


Figure 7: IR imaging pictures of the device with respect to the electrical current direction in the thermopiles in Peltier mode. Left: current for p end to n end and right: current from n end to p end.

The heat generation and absorption were only observable at the center of the thermopiles because, first, the sample was maintained at 75°C during all the experiments, and second, the silicon membranes were too thin to absorb IR waves. The Peltier effect and, in particular, Peltier cooling, is then possible on silicon technologies, opening the way to a possible integration of thermoelectric coolers. However, it is worth noting that the TEG device was not designed for Peltier cooling, which is naturally much lower than Joule heating.

demonstrated the benefits of patterning. Moreover, phonon scattering induces an increase in the Seebeck coefficient compensated by an increase in electrical resistance and better thermal gradient management through the thermopiles. The net gain remains positive and we report $400\text{nW}/\text{cm}^2$ under $\Delta T = 3\text{K}$ up to $5.5\text{mW}/\text{cm}^2$ under $\Delta T = 282\text{K}$ according to the temperature difference across the thermopiles. This CMOS-

compatible device opens perspective in the relevant range (cm² footprint, mW power) for IoT power supply. In addition, the studied devices can be considered as state-of-the-art

silicon micro-harvesters. This study also highlights the feasibility of using integrated crystalline silicon thermoelectric coolers.

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Data availability statement

All data that support the findings of this study are included within the article. More details regarding the fabrication process and characterization methodology can be found in the supplementary material.

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