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Interpretation of 28 nm FD-SOI quantum dot transport data taken at 1.4 K using 3D Quantum TCAD simulations

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Abstract— **Reliable operation of nanoscale CMOS quantum dot devices at cryogenic temperatures fabricated with standard manufacturing techniques is of great importance for quantum computing applications. We investigated the behavior of an Ultra Thin Body and Buried oxide (UTBB) Fully Depleted Silicon-On-Insulator (FD-SOI) quantum dot device fabricated using the standard fabrication process of STMicroelectronics at very low temperatures. The performance of the quantum dot device is simulated and analyzed using the 3D Quantum Technology Computer Aided Design (QTCAD) software recently developed by Nanoacademic Technologies, achieving convergence down to 1.4 K. In this paper we present preliminary simulation results of this work and compare them with actual experimental data collected from measurements of the same device.**

Keywords- *FD-SOI CMOS, silicon quantum dots, quantum computation, 3D TCAD simulations, cryogenic temperatures*

I. INTRODUCTION

Quantum computers, which use quantum bits (qubits) as their building blocks, harness the phenomena of quantum mechanics to deliver disruptive advantages over a wide range of classical technologies. A promising approach to the implementation of a physical qubit is via silicon quantum dot architectures, in which the quantum system used for quantum information processing is the spin of an electron or a hole confined in a quantum dot [1, 2].

Qubits based on silicon quantum dots in conventional CMOS technologies promise to enable reproducible, high-yield industrial manufacturing and co-integration with classical control hardware, two decisive steps toward scalability [3-5]. In addition, by shortening R&D cycles, industrial spin-qubit production promises to accelerate the development of novel devices coupling several qubits together for large scale, high-fidelity logical operations.

Our goal towards a scalable qubit architecture is to develop a silicon-based qubit structure fabricated using exclusively CMOS industrial manufacturing techniques.

More precisely, our device is based on the 28nm Ultra-Thin Body and Buried oxide (UTBB) Fully Depleted Silicon-On-Insulator (FD-SOI) technology node of STMicroelectronics which has already demonstrated functional operation at cryogenic temperatures [6-9]. In order to define a consistent and fast design flow for the device, it is crucial to predict its performance at cryogenic temperatures and to understand the electrical and quantum phenomena that will occur in the device in a simulation environment, before actually fabricating the device. This is a key step to avoid lengthy fabrication-and-measurement optimization loops that would be extremely time-consuming due to the long fabrication and characterization cycles. For this reason, in this work we demonstrate the use of a 3D Quantum Technology Computer Aided Design (QTCAD) simulation tool for modeling our quantum dot device at cryogenic temperatures [10].

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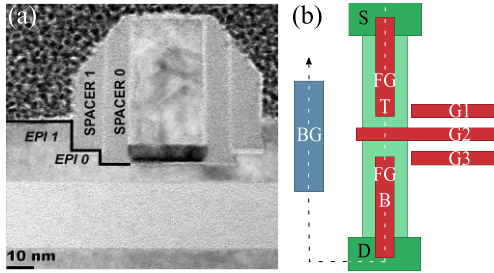


Figure 1. (a) TEM image illustrating the cross-section of a typical FD-SOI MOSFET. Image taken from [11]. (b) Schematic representation showing the top view of the quantum dot architecture developed and studied in this work. The source (S), drain (D), back gate (BG), and the polysilicon gates (FGT, FGB, G1, G2, G3) are indicated in the figure.

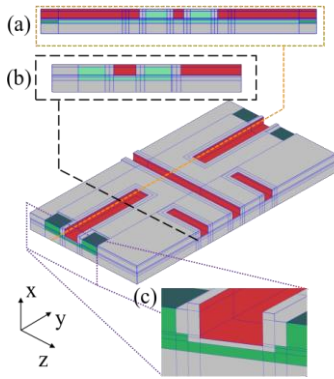


Figure 2. 3D model of the FD-SOI nanostructure from the layout used for fabrication of the device via Gmsh [12] and the QTCAD simulation tool. The device is used to form electrostatically defined quantum dots under the electrodes for quantum computing applications. (a) Cross-section along the y-axis illustrating the two parts of the front gate (red), the gate G2 (red) and the silicon channel (pale green) grown on the BOX (gray). (b) Cross-section along the x-axis illustrating the channel, the front gate lying on the silicon film and the gate G3 that lies on the oxide. (c) Cross section along the x-axis presenting the channel, the epitaxially grown source and drain, the spacers, the gate stack and, finally, the gate oxide. The darkest green shade indicates surfaces at which Ohmic boundary conditions are imposed in the simulations.

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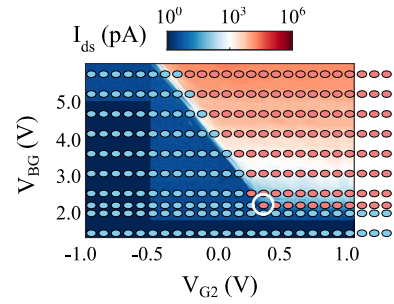


Figure 3. Measured current as a function of V_{BG} and V_{G2} forming the charge stability diagram. Density plot: experimentally measured current. Blue dots: numerical calculations of the band diagram predicting blocked transport. Red dots: numerical calculations predicting allowed transport. In the device measured at 1.4 K, a transport apex is identified at $(V_{G2}, V_{BG}) = (0.34, 2.24)$ V (white circle). In the simulated device, it is identified at $(V_{G2}, V_{BG}) = (0.0, 3.7)$ V. The numerical data have been shifted in the V_{G2} and V_{BG} axes by 0.34V and -1.46V, respectively, so that these two apexes fit together.

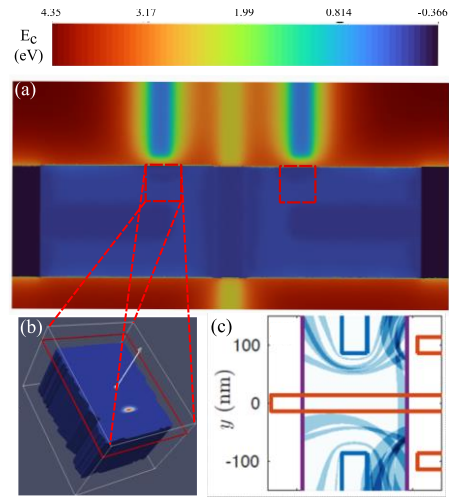


Figure 4. Experimental evidence and numerical simulations supporting the presence of corner dots near G1 and G3. (a) Numerical calculation of the conduction band edge. (b) Numerical calculation of the ground state of single electrons near G1. (c) Experimental triangulation of the quantum dots. Quantum dots are expected to form where the blue shade is the darkest.

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