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Design methodology of a 28 nm FD-SOI Capacitive Feedback RF LNA based on the ACM Model and Look-up Tables

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Abstract— The race to reduce the size and improve power consumption in new transistor technologies has given rise to design trade-offs that are difficult to address with standard methodologies that require an iterative process. This paper proposes a design methodology based on the ACM model and look-up tables to quickly size a 28 nm FD-SOI RF LNA. The design incorporates different tuning knobs that can be useful for optimizing design constraints and, in particular, adapting the circuit performances at very low temperatures.

Keywords- FD-SOI; ACM model; Look-up table design; LNA RF.

I. INTRODUCTION

As the size of silicon transistors is scaled down, there is a notable increase in performance regarding the speed of operation and power consumption of the device. Although there are important improvements seen with length reduction, such improvements are accompanied by the amplification of intrinsic parasitics and physical phenomena not perceived in large-length transistors. Classical design techniques become inadequate to deploy an effective design environment, forcing the designer to follow an iterative design process that heavily depends on simulation software. This type of approach can prove to be time-consuming and lacks insight regarding the working of the transistor.

The above-stated limitations can be tackled by using an adequate model that covers the behavior of the transistor at different working regions and which can be efficiently integrated on existing numerical computing environments together with Spice-based simulation software. We use for this the Advanced Compact MOSFET (ACM) model together with a Look-Up Table (LUT) in a co-simulation environment with MATLAB and Spice models [1,2]. In this paper, we will describe this approach for the design of a capacitive feedback radio-frequency (RF) Low Noise Amplifier (LNA) designed to minimize power consumption and noise figure with suitable S-parameters at a working frequency of 7 GHz.

With respect to the state-of-the-art of CMOS LNAs working in a similar frequency range (6.77-7.55 GHz), our design presents an important reduction of power consumption, almost a factor of 10. Since we are also

interested in studying the behavior of this LNA at very low temperatures for which circuit models are not yet available to us, different voltage bias are considered as tuning knobs to optimize and adapt the circuit performances as the temperature decreases.

II. CAPACITIVE FEEDBACK RF LNA

The amplifying stage of a capacitive feedback LNA is shown in Figure 1. This architecture allows, in principle, the matching of the input impedance via the passive components L_g and C_F while the stage gain is defined by the sizing of the transistor as we have done in [3] for lower frequency designs. Since there will be an output stage, neglecting C_L with respect to C_F , the LNA gain is given by

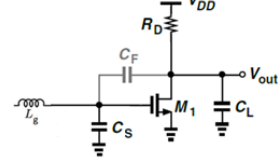


Figure 1. Capacitive Feedback LNA

$$G_{LNA} = \frac{sR_D C_F - g_m R_D}{s^3 R_D C_F C_S L_g + s^2 [C_F L_g (1 + g_m R_D) + C_S L_g] + s R_D C_F + 1} \quad (1)$$

with DC gain $A_{v0} = -g_m R_D$ and the presence of a zero in the numerator that typically will occur well beyond the working frequency. The expression of the poles in the denominator is complicated. A Zero-Value Time (ZVT) constants analysis allows a conservative estimation of the first cut frequency as

$$f_h \approx \frac{1}{2\pi R_D C_f + g_m L_g} \quad (2)$$

where the time constant $R_L C_f$ is dominant. Real and imaginary components of input impedance are given by

$$R_e \approx \frac{R_D C_F}{C_F (1 + g_m R_D) + C_S} \quad (3)$$

$$I_m \approx s L_g + \frac{1}{s [(1 + g_m R_D) C_F + C_S]} \quad (4)$$

These first order equations allow to set the gain, input impedance and working frequency as a function of the design parameters R_D , g_m , C_S , C_F and L_g . Parasitic

components of the inductance and amplifying transistor M_1 play an important role. We have considered a π model of the inductance including parasitic capacitors and resistors, and the LNA behavioral equations have been developed, but we will not describe them here for lack of space. In addition to these design equations, the simultaneous optimization of noise figure, gain and power consumption depends on the inversion level of transistor M_1 which will be set as discussed next.

III. DESIGN METHODOLOGY

We must first characterize the technology using the ACM model and a LUT in MATLAB. With extracted technology parameters, the inversion level of transistor M_1 is set while the different design specifications are addressed sequentially to arrive at the transistor sizing. As a departure point for setting the inversion level, the minimum noise figure that can be obtained at the input of transistor M_1 is given by

$$F_{min} \cong 1 + \frac{\omega}{\omega_t} \quad (5)$$

where ω_t is the transit frequency [4]. This frequency depends on the transistor sizing and represents a lower end of the noise level obtained for strong inversion and minimum bias. Power consumption, working frequency, and noise figure can be simultaneously considered by using the following Figure of Merit (FoM)

$$FoM = \frac{f_t g_m}{I_D} \quad (6)$$

where I_D is the bias current of transistor M_1 and g_m/I_d defines the inversion level. The DC gain, the load resistance, the bias current and the transistor sizing are related by

$$A_{v0} = - \frac{\frac{g_m}{I_D}}{\frac{1}{V_{EA}} + \frac{1}{I_D R_D}} \quad (7)$$

where V_{EA} is the Early voltage technological parameter. The LUT table allows to plot: (1) F_{min} as a function of g_m/I_d for different values of M_1 drain-source voltage V_{ds} , (2) FoM as a function of g_m/I_d for different values of the transistor length L , and (3) A_{v0} as a function of V_{ds} for different values of g_m/I_d and the transistor length L . The use of these graphs and the behavioral model of the LNA allows the sizing of the transistor and the different components to meet the design specifications while minimizing power consumption.

IV. SIMULATIONS RESULTS

We have designed a 28 nm FD-SOI capacitive feedback LNA shown in Fig. 2. The schematics of the LNA in Fig. 2(a) show also the bias and output buffer blocks. In the layout of the test chip in Fig. 2(b), the LNA is placed in the top part. The performances of the LNA for a post-layout simulation (PLS) at 233.15K are shown in Fig. 3(c) and summarized in Table I. This is the lowest temperature

for which we could carry on trustable electrical post-layout simulations (PLS).

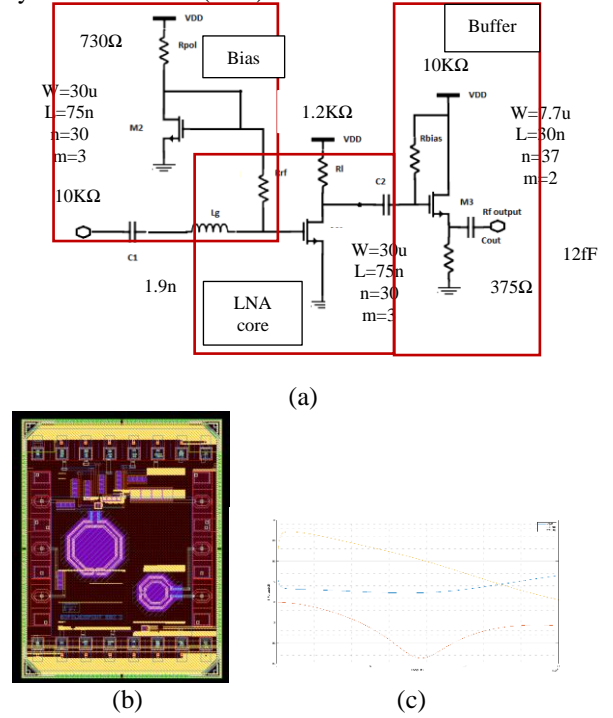


Fig. 2. Capacitive feedback LNA test chip: (a) schematics, (b) layout of the test chip, and (c) post-layout simulation.

TABLE I. PLS RESULTS FOR THE LNA

Gain (dB)	Noise Figure (dB)	PW (μ W)	Center Frequency (GHz)	Gm (mS)	Gm/ID (V^{-1})
11.2	2.3	655	7	20	28

Additional circuit elements (resistance, capacitance, inductance, transistor) are placed in the bottom part of the test chip for characterizing them at temperatures below the standard ones for which we do not have a model. We have multiple tuning voltages in the design which are intended to help for adapting the LNA performances as the temperature decreases to very low values, in particular the body bias of the amplification stage, the body bias of the output buffer, and the voltage bias of each stage.

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