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Analysis of an Inverter Logic Cell based on 3D Vertical NanoWire Junction-Less Transistors

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***Abstract*—Vertical Nanowire Junction-less Transistors (VNWFET) are a promising technology for designing energy-efficient neural networks. This work presents the first results for 3D VNWFET logic cell design taking into account the influence of intra-cell parasitic interconnects on circuit performances. The proposed methodology is used to investigate the performance of a CMOS inverter through co-simulation of the VNWFET SPICE compact model coupled with the circuit parasitic netlist extracted from 3D TCAD simulations using a standard circuit simulator.**

***Index Terms*—Junction-less nanowire transistors, 3D logic cells, compact model, TCAD simulation, parasitic interconnects.**

I. Introduction

The technology for emerging computing has tremendorsly evolved recently. With increasing demand for energy-efficient hardware, we are entering a new era of artificial intelligence (AI) using neural networks (NN). While AI requires dense NNs to work efficiently, conventional planar technology starts to show its limits in terms of compactness due to 2D architecture. One of these crucial limiting factors is the transfer rate between computational and memory units in conventional von Neumann architectures. It is thus necessary to combine the computational and memory units in an innovative 3D architecture for efficient artifical neural networks. This can be achieved using 3D logic cells based on an emerging technology of vertical nanowire junctionless transistors (VNWFET). Due to the inherent 3D nature of this technology, design of the related logic cells is far from being optimized and contains layout-dependent distributed parasitic elements arising from the interconnects. The objective of this work is to analyze an inverter logic cell based on the VNWFET technology and understand the influence of parasitic interconnects on the logic cell performance.

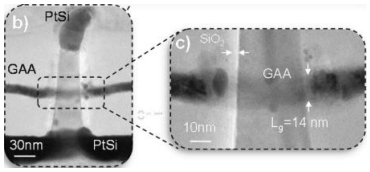

Fig. 1: VNWFET device showing a single vertical nanowire [1].

II. VNWFET Technology Background

A. Technology description

The VNWFET device [1] *(Fig.1)* has a junction-less (JL) architecture composed of a vertical nanowires that are homogenously doped with high Boron concentration ($2x10^{19} cm^{-3}$) with 14nm of effective channel length. The Gate-All-Around architecture offers better gate electrostatic control and higher immunity to short channel effects.

B. Compact Model

JL nanowire channel in the off state remains fully depleted due to a transverse electric field generated by the electrostatic coupling between the gate and the channel. As gate bias is increased beyond the threshold voltage, the device operates in partial depletion through bulk (nanowire core) conduction and beyond flatband voltage, the device enters accumulation with surface conduction and a fully formed conducting channel. The associated compact model formulation [2] is based on a unified charge-based control model (UCCM) [3]. The model formulation principally relies on the analytical solution of total mobile charge decoupled between depletion and accumulation modes. In addition, correction in the drain current calculation due to short channel effects and Schottky S/D contact modeling have also been taken into account [4].

C. Circuit description

The circuit under study is a CMOS inverter based on the VNWFET technology (schematic in *Fig 2a.*). The inverter is designed using an NFET and 3 PFETs each with a $14nm$ nanowire (NW) channel of $22nm$ diameter (*Fig 2b.*).

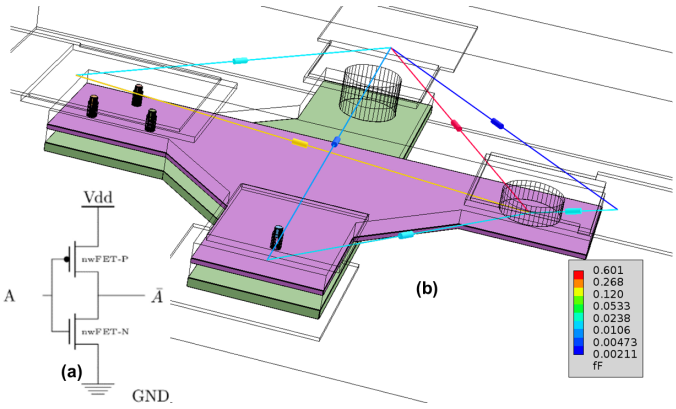

Fig. 2: Schematic and 3D layout with parasitic network of the inverter.

We used a 3 times higher mobility for the NFET compared to the PFETs. This leads to a natural gate swinching symmetry. Furthermore, parasitic elements due to the interconnects are also taken into account since they can limit the switching delays dedicated to non-optimized 3D cell layouts. These parasitic elements have been extracted (PEX) using the GTS DTCO flow for this technology [4]. *Fig 2b.* illustrates the

equivalent electrical network of these parasitic capacitances and resistances, located between the transistors and metal vias. The capacitances between the NWs are neglected since they have little influence on the circuit behavior due to their electrodes being at the same potential.

III. Methodology

A. Transistor level validation

The circuit analysis methodology used in this work relies on coupling SPICE compact model with automatically generated netlist of the parasitic interconnect network for 3D logic circuit simulation. To do so, the SPICE compact model has been validated against measurements and TCAD simulation of the 3D transistor (*Fig 3*). Then, the 3D cell design using the TCAD model has been used to generate the SPICE netlist of the intra-cell parasitic network that is coupled with the compact model in the Advanced Design System (ADS) circuit simulation environment.

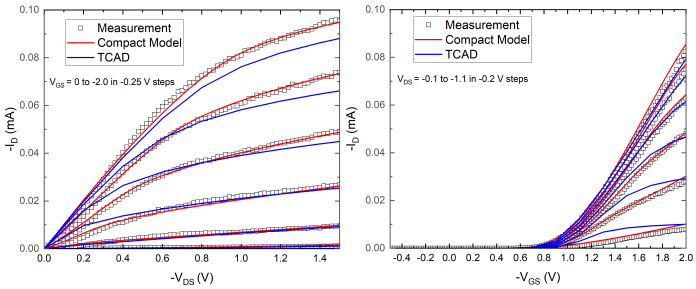

Fig. 3: Comparison between measurements, compact model and TCAD for a VNWFET with 16 NWs of 22nm of diameter.

B. Circuit Level Analysis

The work flow applied here combines TCAD simulation and compact model on ADS to perform transient simulations of inverter logic cells following standard design rules (section II.C). As a reference, an ideal inverter is first simulated (without PEX) using the Verilog-A compact model. Then, the complete schematic including the transistor compact model and the parasitic netlist was analyzed via transient simulation. Both simulations were performed for a duration of $20\mu s$ (with a $5ps$ resolution) for a $1V$ input signal with $10ns$ of rise/fall time. To analyse the inverter performance metrics, the following parameters are extracted : Output transition times $t_r = t|_{out=0.95V_{dd}} - t|_{out=-0.05V_{dd}}$ and $t_f = t|_{out=0.05V_{dd}} - t|_{out=1.05V_{dd}}$, the delay time $t_{mid} = t|_{out=0.5V_{dd}} - t|_{in=0.5V_{dd}}$, the transition energies $E_t = E_tr + E_tf$ with $E_tr = V_{dd}\int_{t|_{out=0.95V_{dd}}}^{t|_{out=0.05V_{dd}}} I_{dd}dt$ and $E_tf = V_{dd}\int_{t|_{out=0.05V_{dd}}}^{t|_{out=0.95V_{dd}}} I_{dd}dt$, and the average power calculated by $P_{AVGr/f} = \frac{E_{r/f}}{T}$ where $E_{r/f}$ is the energy calculated over a period of $T = 2us$ interval centered around each transition.

IV. Results

Figs. 4a and 4b show the evolution of the inverter output during both rising and falling input transitions while *Table 1* summarizes the performance parameters values. The results for the ideal scenario (without parasitic network) show that the inverter is correctly balanced with $t_r \cong t_f$. The inverter output waveform shows an overshoot voltage before each transition due to the charging of the intrinsic gate overlap capacitances. Output transitions exhibit different overshoots between 8ns and 12ns (*Fig. 4*), indicating the presence of distributed overlap capacitances intrinsic to the NW transistors. The simulation results including PEX present additional transition delay times with subsequent increases in average power and energy, compared to the ideal inverter. Due to these parasitic contributions, the rising input energy consumption is higher than that of the falling input transition for the non-ideal inverter.

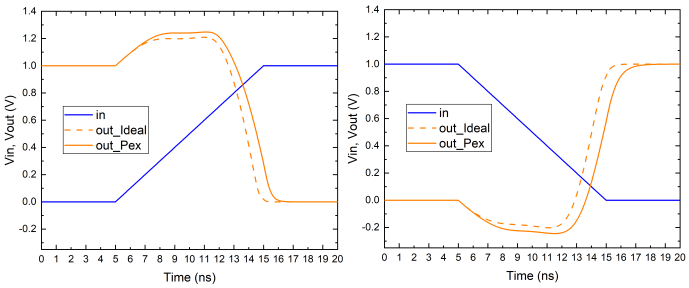

Fig. 4: Voltage output with and without PEX as a function of time for (a) rising (b) falling input.

	Ideal Inverter	Inverter with PEX
t_r(ns)	9.62	10.78
t_f(ns)	9.22	10.06
$t_{mid}r$(ns)	4.06	4.86
$t_{mid}f$(ns)	3.84	4.52
E_t(fJ)	1.2178	2.2768
$P_{AVG}rise$(pW)	663	1214
$P_{AVG}fall$(pW)	300	467

TABLE I: Transition and Delay time, Transition Energy, Average Power

V. Conclusion

Performance figures of merit of a CMOS inverter logic cell based on the 3D VNWET technology were analyzed using SPICE circuit simulation. Transistor compact model and TCAD simulations were calibrated against experimental data. Compared to intrinsic overlap parasitic capactiances, intra-cell parasitic interconnects were shown to not influence the transition delay significantly while mainly influencing power consumption due to increased resistances. The extraction of overlap gate capactiances is thus very important for understanding their influence on the fabricated inverter circuit. This is also crucial for accurate performance estimation of realistic computational logic circuits for emerging computing paradigms and validation of our proposed methodology.

Acknowledgment

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