



**HAL**  
open science

## **Circuit Design Flow dedicated to 3D vertical nanowire FET**

Cristell Maneux, Mukherjee Chhandak, Marina Deng, Bruno Neckel Wesling,  
Lucas Réveil, Zlatan Stanojevic, Oskar Baumgartner, Ian O'Connor, Arnaud  
Poittevin, Guilhem Larrieu

► **To cite this version:**

Cristell Maneux, Mukherjee Chhandak, Marina Deng, Bruno Neckel Wesling, Lucas Réveil, et al..  
Circuit Design Flow dedicated to 3D vertical nanowire FET. IEEE Latin American Electron Devices  
Conference (LAEDC 2022), Jul 2022, Puebla, Mexico. 10.1109/LAEDC54796.2022.9908233 . hal-  
03765071

**HAL Id: hal-03765071**

**<https://hal.science/hal-03765071v1>**

Submitted on 10 Nov 2022

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# Circuit Design Flow dedicated to 3D vertical nanowire FET

Cristell Maneux, Chhandak Mukherjee,  
Marina Deng, Bruno Neckel Wesling,  
Lucas Reveil  
IMS, University of Bordeaux,  
CNRS UMR 5218,  
Talence, France  
[first\\_name.last\\_name@ims-bordeaux.fr](mailto:first_name.last_name@ims-bordeaux.fr)

Zlatan Stanojevic, Oskar Baumgartner  
Global TCAD Solutions,  
Vienna, Austria  
[z.stanojevic@globaltcad.com](mailto:z.stanojevic@globaltcad.com)  
[o.baumgartner@globaltcad.com](mailto:o.baumgartner@globaltcad.com)

I. O'Connor, Arnaud Poittevin,  
Lyon Institute of Nanotechnology,  
CNRS UMR 5270, Ecole Centrale de  
Lyon, Ecully, France  
[first\\_name.last\\_name@ec-lyon.fr](mailto:first_name.last_name@ec-lyon.fr)

Guilhem Larrieu  
LAAS-CNRS, Université de Toulouse,  
Toulouse, France  
[guilhem.larrieu@laas.fr](mailto:guilhem.larrieu@laas.fr)

**Abstract**— To continue transistor downscaling beyond lateral 7nm devices, gate-all-around (GAA) junction-less vertical nanowire field effect transistors (VNW-FET) represent a promising option. This invited paper presents the circuit design flow based on a vertical junctionless transistor technology. On the basis of state-of-the-art junctionless nanowire transistors (JLNT), DC characterization, compact modelling, EM simulation and parameter extraction are described in details. Using this circuit design flow, a set of innovative 3D circuit architectures are explored.

**Keywords**— Compact modelling, DC characterization, parasitics extraction, EM simulation, VNW-FET, 3D logic circuit simulation.

## I. INTRODUCTION

Nanowire transistors are being considered as crucial building blocks for the ultimate scaling of MOS transistors, capable of sustaining extreme miniaturization and complex architectures compatible for 3D vertical integration, owing to their physical and geometrical properties. In particular, nanowires' suitability for forming a gate-all-around (GAA) configuration offers an optimum electrostatic control of the gate over the conduction channel and a better immunity against the short channel effects (SCE). Junction-less nanowire transistors (JLNT) [1-5] have been proposed to further circumvent the problems due to SCE. JLNTs are accumulation mode transistors that are fully depleted below threshold. Above threshold the current flows through the bulk while an accumulation channel forms for sufficiently large gate voltages [1-2, 4]. However, many issues still remain unaddressed regarding:

- The impact of the transition from 1D scaling to transistors scaled in all dimensions.
- The development of dedicated test structures to support the compact model parameter extraction that might use electromagnetic (EM) simulation to ensure parasitic extraction.
- The development of compact models and full design kit (PDK) to support the circuit design process.
- The design, build and test of 3D logic blocks based on stacked regular fabrics of vertical NWFETs and prove enhanced logic functionality and logic circuit operation.

Hence, if the gate-all-around (GAA) junction-less vertical nanowire field effect transistors (VNW-FET) technology could be considered as the prime candidate for demonstrating new concepts at transistor and circuit level which bring the potential of highly improved performance for generic applications, today, the acceptability of new logic paradigms based on emerging technologies is hindered by the lack of proof that such approaches actually work.

This invited paper provides consistent elements of a circuit design flow dedicated to 3D vertical nanowire FET and demonstrates its implementation to set-up an innovative 3D logic circuit design.

First, section II briefly describes the state-of-the-art Vertical GAA JLNTs. Then, section IV gives its compact model main features while section III is dedicated to the extraction of the associated test structure allowing robust parameter value procedure to feed the compact model. Finally, section V leverages the developed compact model to assess the performance metrics of a conventional inverter Boolean logic cell implemented in the VNW-FET technology.

## II. VERTICAL GAA JLNTS

Vertical JLNTs with nanoscale metallic GAA (~14nm) have been demonstrated [6] including symmetrical silicided source and drain contacts (Fig. 1). These scaled device [7] shows very good immunity against short channel effect with NW diameter up to 40 nm and Ion/Ioff ratio up to 5 decades. Multi-VT technology platform by varying NW diameters can be simply achieved with this vertical architecture [8], offering opportunities at the design level.

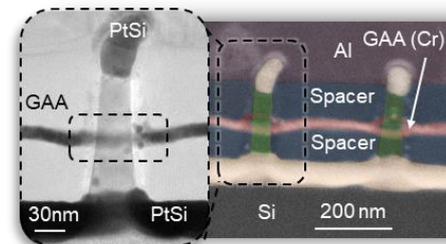


Fig. 1. Vertical JLNTs with 14nm GAA and S/D silicided contacts (adapted from [LAR13] [8]).

### III. EM SIMULATION AND PARAMETER EXTRACTION

On-wafer test structures (fig. 2) of the devices contain parasitic elements introduced by the RF pads and interconnects that are necessary to probe the devices under test (DUT). The standard procedure to characterize the parasitic effects of a device at high frequencies can be divided into two parts. Firstly, the measurement system needs to be calibrated so that the reference plane is at the probe tips. This can be done using standard calibration techniques such as SOLT (Short-Open-Load-Thru). At this point, all the parasitic elements associated with the pads and interconnects are still included in the measurements. In the second step, S-parameters of the open and short structures are measured which are then used to remove the parasitic elements external to the DUT, through a subtraction process known as de-embedding [9].

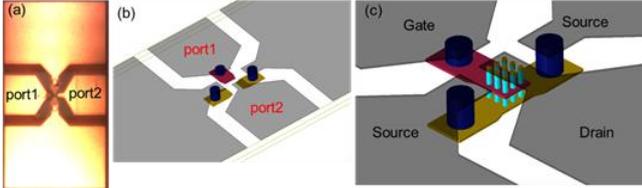


Fig. 2. VNWFET test structures (a) Open structure for S-parameters measurements, (b) a 3-D view of the open structure created using ADS MOMENTUM and (c) the drawing of the VNWFETs showing the nanowires. (adapted from [10]).

Although the process of parasitic extraction is widely used in technologies targeted for high frequency applications, this process can also be applied for technologies such as the VNWFET that are mainly designed for computing applications to improve the modelling accuracy, which normally just relies on DC measurements [11]. Moreover, an accurate modelling of the parasitic elements allows the designer to optimize the 3D layout of the logic circuits and interconnects, thereby improving performance metrics such as compactness and energy-delay product of the technology.

We have elaborate a dedicated methodology for extracting the extrinsic interconnect parasitic network associated with the unconventional vertical and inherently 3D test structures of the VNWFETs. This methodology is detailed in [10] and the results are summarized in Figure 3, 4 and 5. These results from the RF measurements and electro-magnetic (EM) simulations are used for the extraction of parasitic elements of the electrical equivalent circuit of an open test structure.

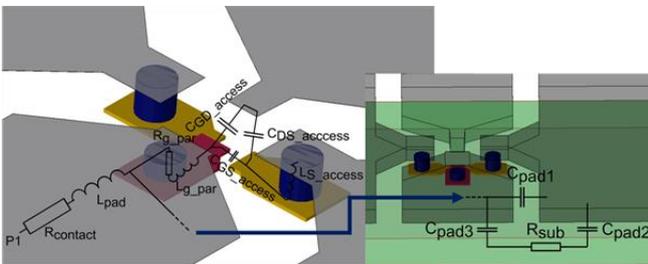


Fig. 3. 3D view of the distributed model

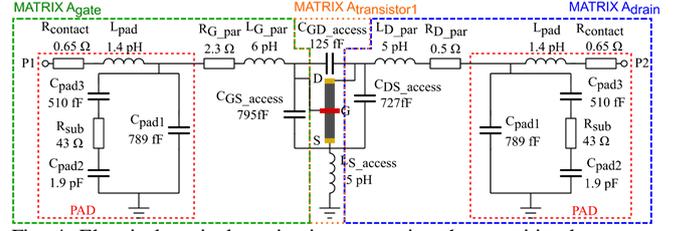


Fig. 4. Electrical equivalent circuit representing the parasitic elements obtained from the open test structure that is used for the de-embedding of VNWFET.

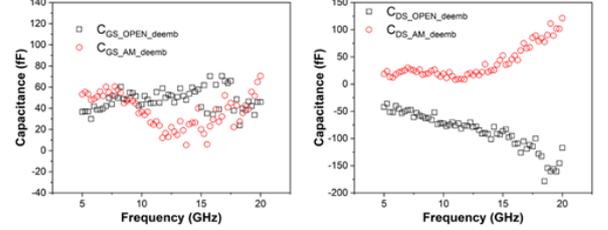


Fig. 5. Small signal capacitances as a function of frequency for the de-embedded transistor at a VGS = -1V and VDS = -0.1V.

### IV. COMPACT MODELING

The model formulation is based on the unified charge-based control model (UCCM) elaborated in [12] for long-channel devices, which furthers the physical basis of the JLNT model presented in [13]. To overcome the limitations of the latter model, specifically in terms of the piece-wise continuous drain current model that requires additional smoothing functions and fitting parameters to bridge the depletion and accumulation modes of operation, the explicit and non-piece-wise solution in [12] treats the mobile charge ( $Q_m$ ) as decoupled between the depletion ( $Q_{DP}$ ) and complementary ( $Q_C$ ) components. In the depletion mode the UCCM expression has been formulated as [12],

$$Q_{DP} = Q_{eff} LW \left\{ \frac{Q_{sc}}{Q_{eff}} \exp \left( \frac{V_g - V_{th} - \eta V}{\eta \phi_T} + \frac{Q_{dep}}{Q_{sc}} \right) \right\} \quad (1)$$

With the depletion charge,  $Q_{dep} = qN_D R/2$ , the effective charge during depletion,  $Q_{eff} = Q_{sc} \eta C_{ox} \phi_T / (Q_{sc} + \eta C_{ox} \phi_T)$ ,  $Q_{sc} = 2\epsilon_S \eta \phi_T / R$ ,  $R$  being the nanowire diameter,  $\eta$  being an interface trap parameter,  $\phi_T$  being the thermal voltage and  $V$  is the potential along the channel. Lambert W functions, LW, have been used in both [12] and [13] for developing the solution for total mobile charge in the JLNT. While the expression for  $Q_{DP}$  in (1) predicts the depletion contribution correctly (for  $V_g < V_{th}$ ), it underestimates the value of the drain current above the flat-band condition. So in accumulation mode, especially in high accumulation, with  $Q_C \geq Q_{dep}$ , the charge  $Q_C$  has been derived to act complementary to  $Q_{DP}$ , considering that the threshold voltage is pinned at  $V_{FB}$  in the accumulation region, in order to avoid using additional smoothing functions and improve simulation time. Under high accumulation  $Q_C \geq Q_{dep}$  and  $Q_C$  is simplified using another Lambert function as following [12],

$$Q_C = \eta C_c \phi_T LW \left\{ \frac{Q_{sc}}{\eta C_c \phi_T} \exp \left( \frac{V_g - V_{FB} - \eta V}{\eta \phi_T} \right) \right\} \quad (2)$$

With corrected electrostatic control through  $C_c = C_{ox} - C_{eff}$ ,  $C_{eff} = 1/C_{ox} + R/2\epsilon_S$ .

Having evaluated both the depletion and complementary parts of the mobile charge, one can formulate the non-pie-

wise continuous model of the total drain current in terms of the  $Q_{DP}$  and  $Q_{DC}$  at the source and the drain end,  $Q_{DP0}$ ,  $Q_{C0}$  and  $Q_{DPL}$ ,  $Q_{CL}$ , respectively,

$$I_{DS,0} = \mu_{eff} \frac{2\pi R}{L_{eff}} \phi_T \left[ \frac{Q_{DP}^2}{2\eta C_{ox} \phi_T} + Q_{DP} + \frac{Q_C^2}{2\eta C_c \phi_T} + 2Q_C \right]_{Q_{C0}}^{Q_{DP0}} \quad (3)$$

Here,  $\eta$  is an interface trap parameter with corrected electrostatic control in accumulation through  $C_c = C_{ox} - C_{eff}$ ,  $C_{eff} = 1/C_{ox} + R/2\epsilon_{Si}$ . The expression of drain current is free of any fitting parameters and can be evaluated based on the physical device parameters such as that of geometry and doping. Additionally, short channel effects were also taken into account considering velocity saturation, an effective mobility,  $\mu_{eff}$ , and incorporating an effective gate length,  $L_{eff} = L - \Delta L$ , where  $L$  is the physical device gate length and  $\Delta L$  is calculated following [14],

$$\Delta L = S \sqrt{\frac{\epsilon_0 \epsilon_{Si} R}{2C_{ox}}} \ln \left( \frac{(V_d - V_{deff}) \left( 1 + \sqrt{1 + \frac{2 \frac{v_{sat}}{\mu} \sqrt{\frac{\epsilon_0 \epsilon_{Si} R}{2C_{ox}}}}{V_d - V_{deff}}} \right)}{2 \frac{v_{sat}}{\mu} \sqrt{\frac{\epsilon_0 \epsilon_{Si} R}{2C_{ox}}}} \right) \quad (4)$$

With,  $v_{sat}$  being the saturation velocity and  $S$  being a parameter ensuring that  $\Delta L$  tends to zero below the threshold, defined as [14],

$$S = \sqrt{1 - \frac{1}{1 + B \frac{Q_{DP0} + Q_{C0}}{C_{eff} \phi_T}}} \quad (5)$$

Where  $Q_{DP0} + Q_{C0}$  is the total mobile charge at the source, given by the long channel expression and  $B$  is a smoothing parameter. Furthermore, the short channel corrections incorporates an effective drain voltage,  $V_{deff}$ , through (4) that reaches its maximum at  $V_{SAT}$ , the saturation voltage [14],

$$V_{deff} = V_{SAT} - V_{SAT} \frac{\ln \left( 1 + \exp \left( A2 \left( 1 - \frac{V_d}{V_{SAT}} \right) \right) \right)}{\ln(1 + \exp(A2))} \quad (6)$$

Here,  $A2$  is another smoothing parameter for the transition of the drain voltage to  $V_{SAT}$ . Considering that the source and drain access region resistances degrade the drain current above threshold, the final expression of the drain current can be written as a function of the long channel current ( $I_{DS,0}$ ), using (3), taking into account the corrections due to short-channel effects described by equations (4)-(6), as follows [14],

$$I_{DS} = \frac{I_{DS,0} NF}{1 + 2\pi \frac{R}{L_{eff}} NF \mu_{eff} (R_S + R_D) \left[ (Q_{DP0} + Q_{C0}) - \eta_1 (Q_{DP0} + Q_{C0} - (Q_{DP,VD,eff} + Q_{C,VD,eff})) \right]} \quad (7)$$

Here,  $R_S$  and  $R_D$  are the source and drain series access resistances, respectively;  $NF$  is the number of nanowires in parallel,  $\eta_1$  is a fine tuning parameter to take into account the drain-voltage dependence of the series access resistances and  $Q_{DP,VD,eff} + Q_{C,VD,eff}$  is the total mobile charge at the drain end (pinch-off) of the channel.

Additionally, considering formation of Schottky contacts at the source and drain access regions, the subthreshold leakage currents are also taken into account. Consequently, thermionic ( $I_{th}$ ), tunneling ( $I_{tun}$ ) and band-to-band tunneling (BTBT) contributions through gate-induced drain leakage (GIDL) are added as separate branch currents [15] to the total

drain current, in order to model the subthreshold behavior of the drain current. The expression used in the compact model for the BTBT current at the drain end reads [15],

$$I_{GIDL} = 2\pi R L_{Access} NF \cdot A_{GIDL} V_{DS} E_{segd}^2 \exp \left( -\frac{B_{GIDL}}{E_{segd}} \right) \quad (8)$$

With  $L_{Access}$  being the lengths of the source and drain access regions outside the channel,  $B_{GIDL}$  is a physics based parameter with a theoretical value of 21.3 MV/cm [15] and  $E_{segd}$  is the electric field in the drain overlap region, given as,

$$E_{segd} = \frac{C_{ox} \sqrt{V_{segd}^2 + (C_{GIDL} V_{DS})^2}}{\epsilon_0 \epsilon_{Si}} \quad (9)$$

Here,  $V_{segd}$  is the gate-drain voltages across the oxide and  $A_{GIDL}$ ,  $C_{GIDL}$  are two GIDL fitting parameters.

## V. INNOVATIVE 3D CIRCUIT ARCHITECTURES

The circuit under study is a CMOS inverter based on the VNWFET technology (schematic in Fig 5a.). The inverter is designed using an NFET and 3 PFETs each with a 14nm nanowire (NW) channel of 22nm diameter (Fig 5b.).

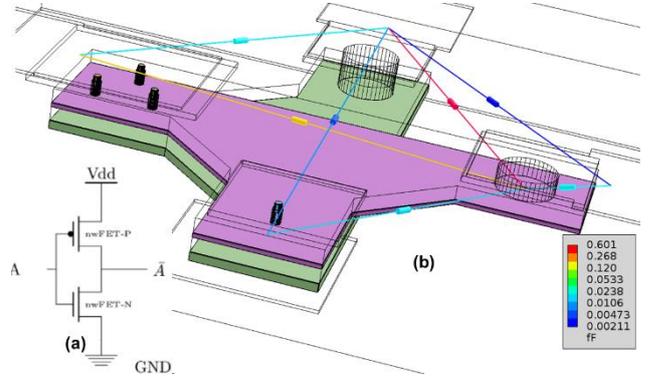


Fig. 5. Schematic and 3D layout with parasitic network of the inverter.

We used a 3 times higher mobility for the NFET compared to the PFETs. This leads to a natural gate switching symmetry. Furthermore, parasitic elements due to the interconnects are also considered since they can limit the switching delays dedicated to non-optimized 3D cell layouts. These parasitic elements have been extracted (PEX) using the GTS DTCO flow for this technology [11]. Fig 5b. illustrates the equivalent electrical network of these parasitic capacitances and resistances, located between the transistors and metal vias. The capacitances between the NWs are neglected since they have little influence on the circuit behaviour due to their electrodes being at the same potential.

The circuit analysis methodology used in this work relies on coupling SPICE compact model with automatically generated netlist of the parasitic interconnect network for 3D logic circuit simulation. To do so, the SPICE compact model has been validated against measurements and TCAD simulation of the 3D transistor (Fig 6). Then, the test structure 3D cell design using the TCAD model has been used to generate the SPICE netlist of the intra-cell parasitic network to be coupled with the compact model in the Advanced Design System (ADS) circuit simulation environment.

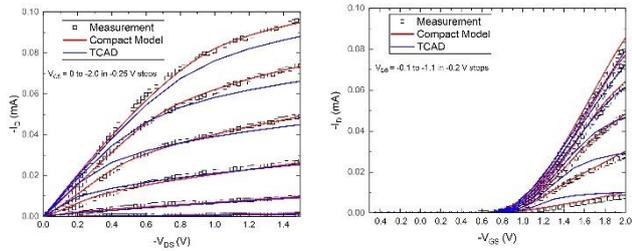


Fig. 6. Comparison between measurements, compact model and TCAD for a VNWET with 16 NWs of 22nm of diameter.

At this stage, the work flow combines TCAD simulation and compact model on ADS to perform transient simulations of inverter logic cells following standard design rules. As a reference, an ideal inverter is first simulated (without PEX) using the Verilog-A compact model. Then, the complete schematic including the transistor compact model and the parasitic netlist was analysed via transient simulation.

Both simulations were performed for a duration of 20 $\mu$ s (with a 5ps resolution) for a 1V input signal with 10ns of rise/fall time. To analyse the inverter performance metrics, the following parameters are extracted: the output transition times, the transition energies, and the average power.

Figs. 7a and 7b show the evolution of the inverter output during both rising and falling input transitions while Table 1 summarizes the performance parameters values. The results for the ideal scenario (without parasitic network) show that the inverter is correctly balanced since  $t_r \sim t_f$ . The inverter output waveform shows an overshoot voltage before each transition due to the charging of the intrinsic gate overlap capacitances.

Output transitions exhibit different overshoots between 8ns and 12ns (Fig. 7), indicating the presence of distributed overlap capacitances intrinsic to the NW transistors.

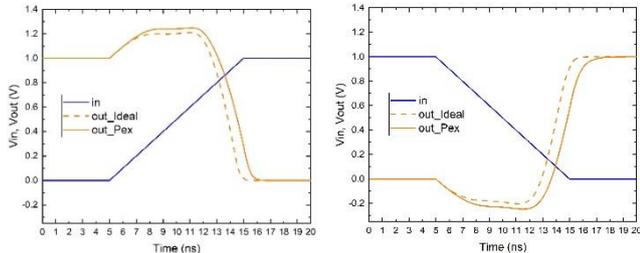


Fig. 7. Voltage output with and without PEX as a function of time for (a) rising (b) falling input.

The simulation results including PEX present additional transition delay times with subsequent increases in average power and energy, compared to the ideal inverter. Due to these parasitic contributions, the rising input energy consumption is higher than the falling input transition for the non-ideal inverter.

TABLE I: Transition and Delay time, Transition Energy, Average Power

	Ideal Inverter	Inverter with PEX
$t_r$ (ns)	9.62	10.78
$t_f$ (ns)	9.22	10.06
$t_{mid}^r$ (ns)	4.06	4.86
$t_{mid}^f$ (ns)	3.84	4.52
$E_t$ (fJ)	1.2178	2.2768
$P_{AVG}^{rise}$ (pW)	663	1214
$P_{AVG}^{fall}$ (pW)	300	467

Hence, the figures of merit of a CMOS inverter logic cell based on the 3D VNWET technology were analysed using SPICE circuit simulation. Transistor compact model and TCAD simulations were calibrated against experimental data. Compared to intrinsic overlap parasitic capacitances, intra-cell parasitic interconnects were shown to not influence the transition delay significantly while mainly influencing power consumption due to increased resistances.

## VI. CONCLUSION

Through consistent elements of a circuit design flow dedicated to 3D vertical nanowire FET, this paper has demonstrated the virtual implementation of an innovative 3D logic circuit design. The extraction of the overlap gate capacitances has been demonstrated to influence the inverter circuit performance. This is crucial for accurate performance estimation of real computational logic circuits dedicated to emerging computing paradigms.

## ACKNOWLEDGMENT

This work is supported by ANR LEGO (Grant 18-CE24-0005-01), Horizon 2020 FVLLMONTI (Grant N°101016776).

## REFERENCES

- [1] J.-P. Colinge and J. C. Greer, *Nanowire Transistors: Physics of Devices and Materials in One Dimension*. Cambridge University Press, 2016.
- [2] J. P. Colinge, C. W. Lee, A. Afzal, *et al.*, "Nanowire transistors without junctions", *Nat. Nanotechnol.* vol. 5, pp. 225-229, 2010.
- [3] D.-Y. Jeon, S. J. Park, M. Mouis, *et al.*, "Low-frequency noise behavior of junctionless transistors compared to inversion-mode transistors", *Solid-State Electronics*, vol. 81, pp. 101-104, March 2013.
- [4] D. Jang, J. W. Lee, C.-W. Lee, *et al.*, "Low-frequency noise in junctionless multigate transistors", *Appl. Phys. Lett.* Vol. 98, pp. 133502-1-3, 2011.
- [5] N. Clément, X. L. Han and G. Larrieu, "Electronic transport mechanisms in scaled gate-all-around silicon nanowire transistor arrays", *Appl. Phys. Lett.*, vol. 103, pp. 263504-1-5, 2013.
- [6] G. Larrieu XL Han (2013) *Nanoscale* 5 (6), 2437-2441.
- [7] G. Guerfi, G. Larrieu (2016) *Nanoscale research letters* 11 (1), 1-7.
- [8] G. Larrieu *et al.* (2017) *Solid-State Electronics* 130, 9-14.
- [9] M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, 'An improved de-embedding technique for on-wafer high-frequency characterization', in *Proceedings of the 1991 Bipolar Circuits and Technology Meeting*, Minneapolis, MN, USA, 1991, pp. 188–191. doi: 10.1109/BIPOL.1991.160985.
- [10] B. Neckel Wesling, M. Deng, C. Mukherjee, M. de Matos, A. Kumar, G. Larrieu, J. Trommer, T. Mikolajick, C. Maneux, "Extraction of small-signal equivalent circuit for de-embedding of 3D vertical nanowire transistor", *EUROSOI Ulis*, Udine Italy, 18-20 May 2022.
- [11] C. Maneux *et al.*, 'Modelling of vertical and ferroelectric junctionless technology for efficient 3D neural network compute cube dedicated to embedded artificial intelligence', *IEEE IEDM*, San Francisco, Dec. 11-15, 2021.
- [12] A. Hamzah, R. Ismail, N E. Alias, M. L. Peng Tan and A. Poorasl, "Explicit continuous models of drain current, terminal charges and intrinsic capacitance for a long-channel junctionless nanowire transistor", *Phys. Scr.* vol. 94, pp. 105813, 2019.
- [13] F. Lime, O. Moldovan and B. Iñiguez, "A Compact Explicit Model for Long-Channel Gate-All-Around Junctionless MOSFETs. Part I: DC Characteristics," *IEEE Trans. Electron Dev.*, vol. 61, no. 9, pp. 3036-3041, Sept. 2014. doi: 10.1109/TED.2014.2340441.
- [14] F. Lim, F. Ávila-Herrera, A. Cerdeira and B. Iñiguez, "A compact explicit DC model for short channel Gate-All-Around junctionless MOSFETs", *Solid State Electron*, vol. 131, pp. 24-29, 2017.
- [15] G. Zhu *et al.*, "Subcircuit Compact Model for Dopant-Segregated Schottky Gate-All-Around Si-Nanowire MOSFETs," *Trans. Electron Dev.*, vol. 57, no. 4, pp. 772-781, April 2010. doi: 10.1109/TED.2010.2041513.