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## **La<sub>2</sub>NiO<sub>4</sub>-Based Memristive Devices Integrated on Si-Based Substrates**

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Valence Change Memories, in which internal redox reactions control the change in resistance are promising candidates for resistive random access memories (ReRAMs) and neuromorphic computing elements. In this context, La<sub>2</sub>NiO<sub>4+δ</sub> (L2NO4), a mixed ionic-electronic conducting oxide, well known for its highly mobile oxygen interstitial ions, emerges as a potential switching material for novel L2NO4-based memristive devices. However, their integration in complementary metal oxide semiconductor (CMOS) technology still has to be demonstrated, as the major focus of previous studies has been carried out on epitaxial films grown on single crystals. In this work, we present the optimization of the deposition temperature and precursor solution composition, allowing to obtain high quality polycrystalline L2NO4 thin films grown by metal organic chemical vapour deposition on a platinumized silicon substrate, and to use these films to build memristive devices in vertical configuration with Ti top electrodes. A bipolar analog-type transition in resistance can be achieved in Ti/L2NO4/Pt memristive devices. While the “forming” process required for the devices based on non-optimized L2NO4 thin films is considered as a drawback, the Ti/optimized L2NO4/Pt devices are forming-free and exhibit a good cyclability. These results prove the switching response of L2NO4-based devices in vertical configuration for the first time.

### **1. Introduction**

Resistive Switching (RS) is described as the phenomena taking place in capacitor-like heterostructures (typically metal/insulator (or semiconductor)/metal stacks), in which resistance can be switched between a low resistance state (LRS) and a high resistance state (HRS) upon an appropriate applied electric field.<sup>[1]</sup> The study of RS on memristive devices has attracted considerable interest for redox-based Resistive Random Access Memory (ReRAM) applications since the reversible resistance change can be used to store logic states (e.g., values “0” and “1” of the binary system), as well as for other logic elements in novel computing paradigms.<sup>[2-7]</sup> In addition, in some cases, by applying suitable voltage pulses of controlled amplitude and duration, several different resistance states of the ReRAM cell can be written, read and erased, which paves the way for multilevel cell memories. Besides, a strong renewal of interest for non-von Neumann computing architecture has recently led to the development of solid state-based synapses dedicated to neuromorphic computing applications using memristive oxides as active layers.<sup>[8-12]</sup>

Oxide-based valence-change memories (VCMs), in which a field-driven oxygen motion triggers the resistance switching of the device by internal redox reactions (the local change of valence in the cation sublattice), are one of the most promising candidates for memory and artificial synapse applications. The valence change can occur in localized regions (filament-type RS) or over the entire memristor area (interface-type RS). Although the most common VCMs are based on filament-type switching, there are still challenging issues to overcome, such as variability, forming, etc.<sup>[13]</sup> In fact, the forming process is a prerequisite step, in which a relatively high electric field is applied to create the filament. This process is considered as a soft breakdown of the switching layer and is usually required before the memory cell works at a lower voltage. In addition, as the formation of the filament is a stochastic process, the variability (cycle-to-cycle or even device-to-device) of programmed resistance states is thus inevitable. Conversely, for artificial synapse applications in which the gradual resistance change can represent synaptic plasticity, analogue switching, provided by

gradual SET/RESET processes of interface-type RS is preferred,<sup>[3]</sup> as the number of stable and distinguishable resistance states is not limited by the abrupt set-event of filamentary switching.

Not only the switching layer but also the electrode material plays a significant role in the performance of VCMs. Indeed, by using oxidizable electrode materials, such as Ti,<sup>[14]</sup> Al,<sup>[15-16]</sup> and TiN,<sup>[17]</sup> the transport properties at the switching layer/electrode interface can be critically affected. For example, in Pt/Ti/Pr<sub>1-x</sub>Ca<sub>x</sub>MnO<sub>3</sub> (PCMO)/SrRuO<sub>3</sub>/SrTiO<sub>3</sub> and Ti/PCMO/Pt vertical heterostructures, the redox reaction occurring at the Ti electrode governs the RS, where the amount of fully oxidized Ti ions in the electrode determines the resistance state of the device.<sup>[18-20]</sup> It is widely accepted that the TiO<sub>x</sub> interlayer is spontaneously formed when Ti is evaporated on top of PCMO. Under positive bias applied at the active electrode, the accumulation of oxygen ions can cause further oxidation of the TiO<sub>x</sub> layer, leading to an added series resistance in the device and thus making it in HRS. The reverse process occurs when a negative voltage is applied and the LRS is achieved. This interlayer acts as an oxygen getter or oxygen reservoir and plays a key role in the memristive properties of the given device.<sup>[21-23]</sup>

A vertical configuration is commonly used for memristors due to its reduced dimensions, compactness and easiness for ReRAM devices fabrication, as well as compatibility for integration in cross-bar array architectures.<sup>[24]</sup> Nevertheless, given the small series resistance of the memristive layer, in particular for semiconducting oxides, which results from low film thickness (between a few nm to a few tens of nm), to avoid the device breakdown, the electrical current density should be carefully controlled by the current compliance.

In the last few years, there has been considerable recent research interest in the use of perovskite and perovskite-related oxides, such as GdBaCo<sub>2</sub>O<sub>5+δ</sub>,<sup>[25]</sup> GdBaCo<sub>2</sub>O<sub>5+δ</sub>/LaNiO<sub>3</sub>,<sup>[26]</sup> LaNiO<sub>3+δ</sub>,<sup>[17, 27]</sup> La<sub>2</sub>NiO<sub>4+δ</sub>,<sup>[28]</sup> Fe-doped SrTiO<sub>3</sub>,<sup>[29]</sup> La<sub>1-x</sub>Sr<sub>x</sub>MnO<sub>3-y</sub>,<sup>[30]</sup> for VCM applications due to their highly tunable ionic and electronic transport properties, potentially allowing for

multilevel resistance states. In this context, among the different materials proposed,  $\text{La}_2\text{NiO}_{4+\delta}$  (L2NO4) presents remarkable properties as an oxide switching layer for memristive devices<sup>[23, 28, 31]</sup>, including its mixed-ionic electronic conduction properties and its capability to accommodate a wide range of oxygen stoichiometry without decomposition. L2NO4 is the first member ( $n=1$ ) of the Ruddlesden-Popper (RP)  $\text{La}_{n+1}\text{Ni}_n\text{O}_{3n+1}$  series and can be described as the intergrowth of  $\text{LaNiO}_3$  layers between individual  $\text{LaO}$  rock-salt type layers. Different from the majority of oxides used as memristive layers, in which oxygen vacancies are often the dopant defects, L2NO4 is chosen due to its oxygen storage capability and high oxygen mobility thanks to the oxygen interstitial point defects present in the structure.<sup>[32]</sup> We recently reported on the significant electroforming-free analogue switching capabilities of epitaxial thin-film L2NO4-based devices grown on  $\text{SrTiO}_3$  single-crystal substrate, both as single  $\text{La}_2\text{NiO}_{4+\delta}$  layers<sup>[28]</sup>, and as  $\text{La}_2\text{NiO}_{4+\delta}/\text{LaNiO}_{3-\delta}$  bilayers.<sup>[31]</sup> Thus, combining L2NO4 with an oxidizable electrode opens the door to the development of new analogue memristive devices with gradual SET and RESET processes, able to provide multilevel resistance states, suitable for mimicking synaptic behavior in neuromorphic computing. The single-layer planar devices, designed with an active Ti electrode and an inert Pt electrode ( $\text{Ti}/200\mu\text{m-L2NO4}/\text{Pt}$ ), showed gradual set and reset transitions and memory transience, suitable for artificial synapse applications. Furthermore, we also showed that the structural cell parameters, the orientation of the L2NO4 films in the bilayers, and the memristive properties of single-layer and bilayer devices could be tuned by varying the oxygen stoichiometry ( $\delta$ ) of the L2NO4 thin films through a post-anneal treatment<sup>[23]</sup> or changing the  $p\text{O}_2$  of the deposition.<sup>[31]</sup> Remarkably, single-layer devices constructed using oxygen-rich L2NO4 films have a larger memory window and improved multilevel analogue-type programming capabilities. However, to integrate these promising memristors in real devices, the compact low-energy-consumption vertical configuration is greatly preferred. Therefore, a silicon-based structure, i.e.,  $\text{Pt}/\text{TiO}_2/\text{SiO}_2/\text{Si}$  (hereafter referred to as Pt) was used in this work to integrate

polycrystalline L2NO4 films into vertical memristive stacks. To grow high-quality L2NO4 films, we used the pulsed injection-metal organic chemical vapour deposition (PI-MOCVD) technique, as it enables to finely grow thin films over large areas with high uniformity and allows for a good control of film thickness by controlling the number of injected microdroplets of precursor solution thanks to an electric injector valve. Moreover, the precursor solution can be simply prepared by dissolution of metal-organic precursors and the stoichiometry of the film is easily adjusted by varying their concentration. Classical MOCVD<sup>[33]</sup> and PI-MOCVD<sup>[34-37]</sup> have been previously used for the growth of epitaxial and polycrystalline L2NO4. However, to the best of our knowledge, the deposition of this layered structure had never been achieved by PI-MOCVD before on platinized silicon, substrates that suffer from dewetting when exposed at the typical high deposition temperatures required for MOCVD deposition. This study focuses on the optimization of the deposition parameters to obtain homogenous, highly dense, phase pure and polycrystalline L2NO4 films, and on the building and testing of vertical L2NO4-based memristive devices for the first time.

## 2. Results and Discussion

Typically, high temperatures ( $\geq 650$  °C) are usually required for the deposition of crystalline layered oxide structures, which experimentally lead to the dewetting of the Pt bottom electrode. In order to avoid this limitation, in this work, we explore the optimization of the deposition conditions in two steps: i) by decreasing the deposition temperature to find the best compromise to avoid the Pt dewetting while maintaining the crystallinity of the film, and ii) by varying the precursor solution composition to obtain stoichiometric, homogenous and highly dense L2NO4 films. The deposition conditions used for the two optimization series are detailed in **Figure 1**, Supporting Information. In the first step, the La/Ni ratio in the precursor solution (R) was fixed to 5.00, while the deposition temperature was varied from 650 °C to 600 °C, with a step of 25 °C. Secondly, the deposition temperature was fixed at 600 °C and R was varied from 5.00 to 4.00, with steps of 0.25.

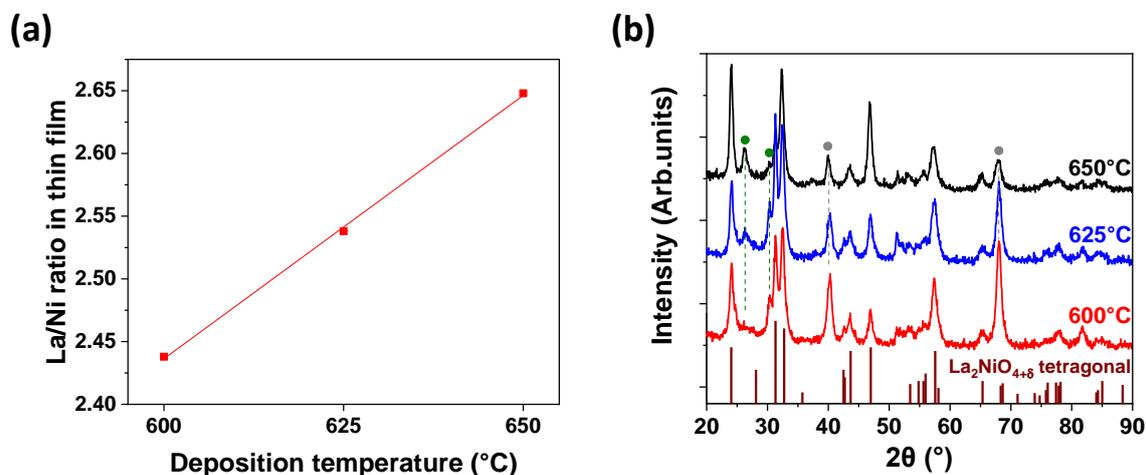
In addition, to be embedded in realistic devices in the future, the fabrication process should be CMOS-BEOL (back-end-of-line) compatible where the temperature is required to be lower than 450 °C. To overcome this challenge, the deposition of amorphous L2NO4 thin film at 400 °C followed by a fast laser crystallization treatment <sup>[38-40]</sup> is considered as a promising approach. Another route to avoid heating above 450 °C would be to build amorphous L2NO4-based memristive devices. However, as the functional properties (electronic and ionic transport) of the amorphous films are expected to be different, their memristive properties might largely differ from the crystalline counterpart. The effects of the deposition temperature and solution composition on the growth of L2NO4 films will be discussed in the following sections.

### **2.1. Effect of the temperature on the growth of polycrystalline L2NO4 films**

The influence of the deposition temperature in the film composition, crystallinity and morphology is assessed for deposition temperatures between 600 and 650 °C with a constant R of 5.00 (red dots in **Figure 1**). These sample's La/Ni ratios were measured by the electron probe microanalysis (EPMA) technique, which increase with increasing deposition temperature, as shown in **Figure 1a**. A clear linear relationship between these two parameters was obtained. The growth rates are 1.3 nm min<sup>-1</sup> and 1.5 nm min<sup>-1</sup> for depositions at 600 °C and 650 °C, which result in films of 43 ± 3 nm and 50 ± 3 nm by using 2000 pulses, respectively.

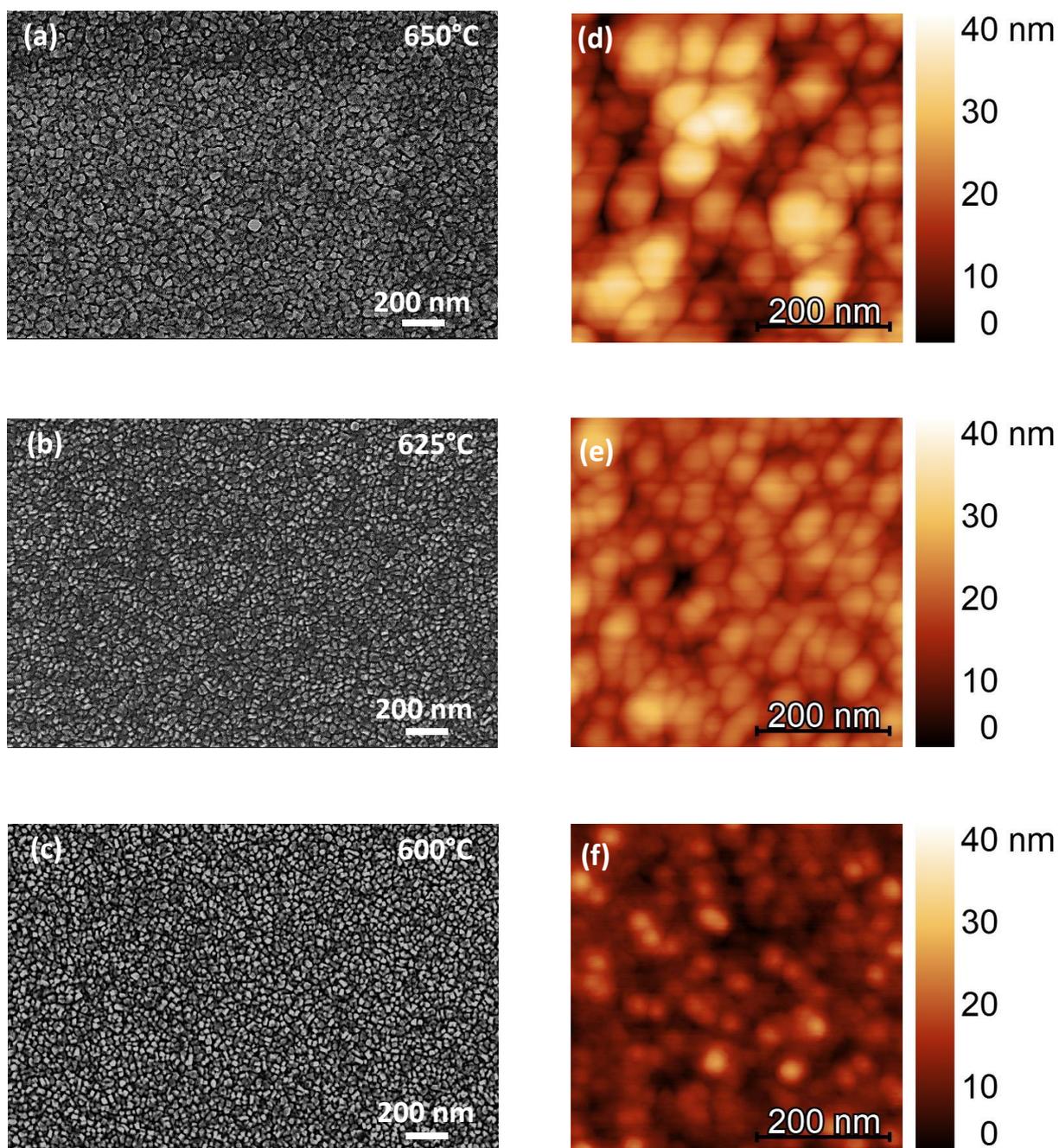
The grazing incidence X-ray diffraction (GI-XRD) patterns obtained for these three films are shown in **Figure 1b**. The Pt substrate peaks are indicated by gray dots. The main diffraction peaks observed are attributed to the L2NO4 tetragonal phase (space group *I4/mmm*, ICDD: 00-034-0314) in polycrystalline form (randomly oriented), with small peaks corresponding to the La<sub>2</sub>CO<sub>5</sub> phase. The intensity of the impurity phase decreases as the deposition temperature decreases, in agreement with the decrease of La/Ni ratio in films (**Figure 1a**). Moreover, an

amorphous thin film can be obtained by lowering the deposition down to 500 °C, while at 550 °C a mixture of the L2NO4 and La<sub>3</sub>Ni<sub>2</sub>O<sub>7</sub> phases is obtained, with a small contribution of the La<sub>2</sub>CO<sub>5</sub> phase (see Figure S2).



**Figure 1.** a) La/Ni atomic ratio measured by EPMA for the L2NO4 films as a function of the PI-MOCVD deposition temperature. b) GI-XRD patterns of L2NO4 films deposited on Pt at different temperatures using a La/Ni ratio of 5 in the precursor solution. The position of the tetragonal *I4/mmm* peaks for La<sub>2</sub>NiO<sub>4+δ</sub> (ICDD: 00-034-0314) has been added at the bottom for comparison. The positions for Pt peaks (gray dots) and impurity La<sub>2</sub>CO<sub>5</sub> phase (green dots) are indicated.

The top-view scanning electron microscopy (SEM) images of films deposited at 650, 625 and 600 °C are shown in **Figure 2a**, **Figure 2b** and **Figure 2c**, respectively. Their surface morphology is quite similar, formed by randomly oriented grains with small grain sizes of the order of 25 - 45 nm. All films are homogeneous, polycrystalline and dense. Moreover, no cracking nor pinholes were observed for any of the samples. It can be observed that the grain size is largest for the 650 °C deposition, and decreases for the lower deposition temperatures.



**Figure 2.** a-c) SEM top-surface and d-f) AFM images of the L2NO<sub>4</sub> films deposited at 650°C, 625°C and 600°C, respectively.

The corresponding atomic force microscopy (AFM) images of these L2NO<sub>4</sub> samples can be found in **Figure 2d**, **Figure 2e** and **Figure 2f**. The sample deposited at 650 °C presents larger particle sizes (root-mean-square (RMS) of 42.1 nm), compared to the films deposited at lower temperatures. At this temperature the small grains cluster to form larger ones, resulting in a film with a larger roughness. At lower temperatures the size of the individual particles is similar (RMS of 23.4 - 24.0 nm), and smaller than that observed for the sample grown at

650 °C, in agreement with the SEM observations. The L2NO4 films deposited at 625 °C and 600 °C are flatter, as measured by the RMS surface roughness, which decreases from 6.6 to 3.4 nm and, when the temperature is reduced from 650 °C to 600 °C (see **Table 1**). The higher roughness of the L2NO4 film deposited at 650 °C can be explained by the L2NO4 grain coarsening and by the evolution of Pt grains during the deposition under a relatively high temperature. The improvement (decrease) of surface roughness when decreasing the deposition temperature is also confirmed by the scanning transmission electron microscopy (STEM) cross-sectional images of L2NO4 films deposited at 600 °C (**Figure 4a**) and at 650 °C (**Figure S4**, Supporting Information)

**Table 1.** RMS surface roughness and average grain size of the L2NO4 films grown at different temperatures

Deposition temperature (°C)	RMS (nm)	Average grain size (nm)
650	6.6	42.1
625	3.6	24.0
600	3.4	23.4

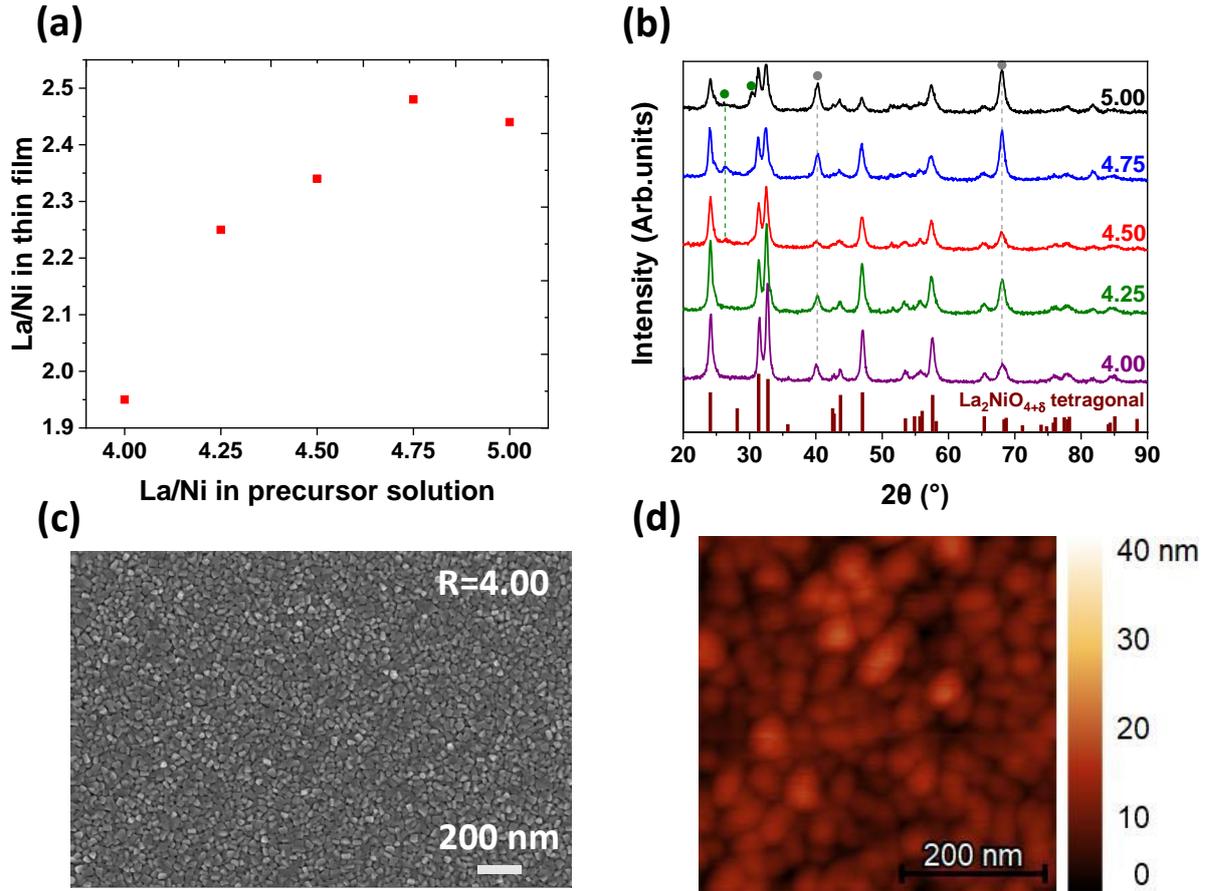
## 2.2. Effect of the solution composition on the growth of polycrystalline L2NO4 films

Due to the smaller film roughness and flatter surface, 600 °C was selected as deposition temperature to grow the L2NO4 films. However, under these deposition conditions, the films present the secondary La<sub>2</sub>CO<sub>5</sub> phase (red diffractogram, **Figure 1b**). In order to improve the film purity at this temperature, several films were prepared by varying R value from 4.00 to 5.00 (blue dots in **Figure S1**). The La/Ni ratios in thin film of these samples obtained by EPMA, together with the GI-XRD patterns of the different films are shown in **Figure 3a** and **Figure 3b**, respectively. By reducing R from 5.00 to 4.50, it is possible to eliminate the presence of impurities, which is confirmed by the absence of the La<sub>2</sub>CO<sub>5</sub> peaks. Thus, only the reflections of the L2NO4 tetragonal phase are observed in the films deposited at 600 °C using R values of 4.25 and 4.00. However, the film deposited at the R of 4.00 in the source exclusively gives a ratio of 1.95 in the L2NO4 film, which is close to the desired value of 2

for the highly pure L2NO<sub>4</sub> phase. Therefore, the optimized conditions which allowed preparing high-quality polycrystalline and flat L2NO<sub>4</sub> films on Pt, without dewetting are: deposition temperature of 600 °C and R of 4.00. These deposition conditions were selected for the film growth and subsequent vertical memristive device fabrication.

In terms of morphology, by decreasing the R value, no major difference is observed between, as shown in the SEM images of those samples, displayed in **Figure S3a-d**, Supporting Information.

The optimized film (i.e., deposition temperature at 600 °C with R of 4.00) was then used to construct the L2NO<sub>4</sub>-based memristive devices. SEM and AFM top-view images of the optimized film are shown in **Figure 3c** and **Figure 3d**, respectively. The morphology observed by SEM is similar to that of the film grown at 600 °C with R of 5.00 (shown in **Figure 2c**), suggesting that the La/Ni ratio in the precursor solution does not have an effect on the morphology of the film. An RMS value of 2.8 nm and an average grain size of 23.7 nm are calculated from the AFM measurements, which are in agreement with those reported for the films deposited at 600°C (**Table 1**).

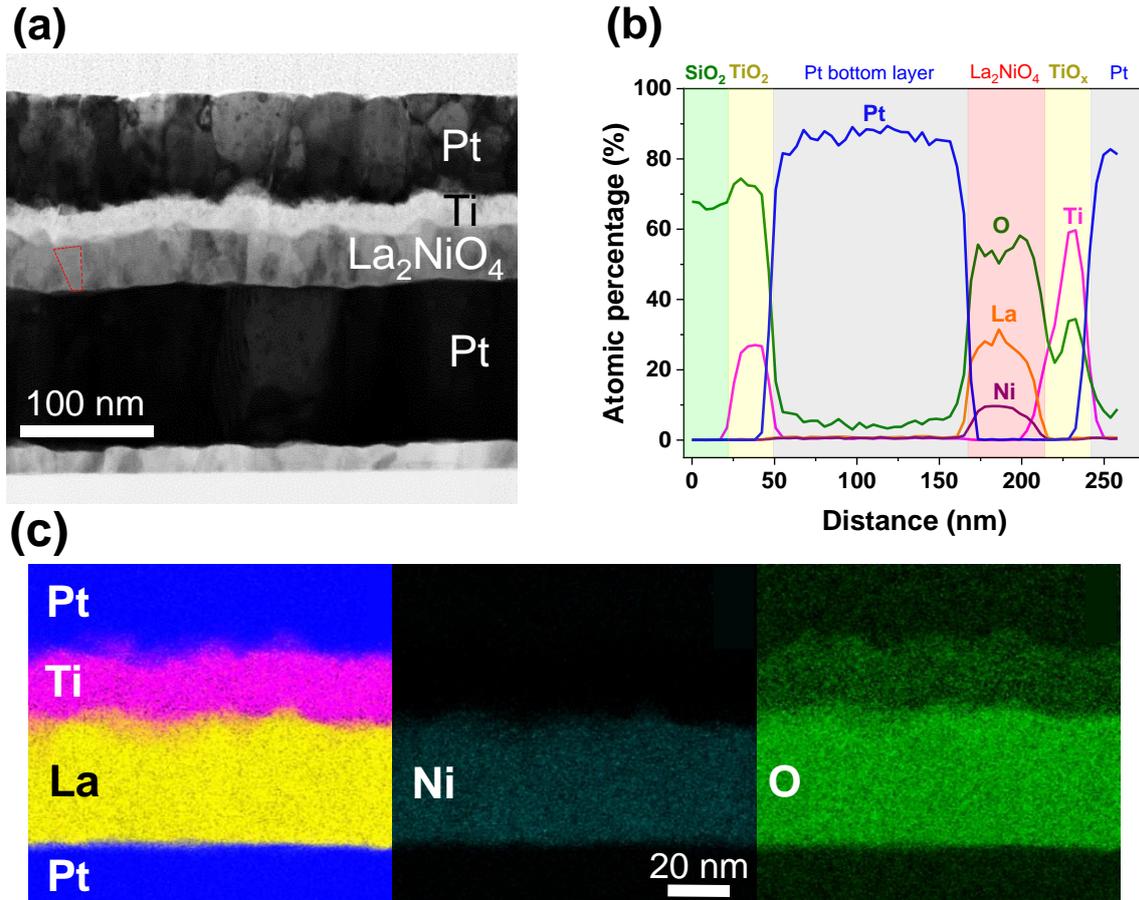


**Figure 3.** a) La/Ni atomic ratio in the L2NO4 films grown at 600°C vs La/Ni atomic ratio in the precursor solution. b) GI-XRD patterns of L2NO4 films deposited on Pt substrate at different precursor concentration ratios. The position of the tetragonal  $I4/mmm$  peaks for  $\text{La}_2\text{NiO}_{4+\delta}$  (ICDD: 00-034-0314) has been added at the bottom for comparison. The positions for Pt peaks (gray dots) and for the peaks corresponding to the  $\text{La}_2\text{CO}_5$  phase (green dots) are indicated. c) SEM and d) AFM top-view image of optimized L2NO4 film deposited on Pt substrate (at 600 °C with R of 4.00).

### 2.3. Microstructural characterization of the Ti/L2NO4/Pt memristive devices in vertical configuration

To build the memristive devices, electrodes consisting of a 25 nm of Ti covered by a 75 nm of Pt, were evaporated on top of the optimized L2NO4 film. In order to study the quality of the device heterostructure, a lamella across the whole stack (from the Pt layer of the top electrode to SiO<sub>2</sub> layer of the substrate) was prepared by focused ion beam (FIB) milling and the STEM image of the lamella is shown in **Figure 4a**. Continuous dense Ti and Pt layers on top of the L2NO4 thin film can be observed, with sharp L2NO4/Ti and Ti/ Pt interfaces, and without dewetting nor Pt diffusion. The grains of the L2NO4 layer increase in size with increasing

film thickness (V-shaped grains, as indicated by the red dashed-line in Figure 4a). Therefore, as can be observed in the image, the number of grains per 100 nm in-plane length decreases from approximately 6-8 grains at bottom part to 4-5 grains at top region. The size of the top grains is thus in good an agreement with the AFM results (i.e., 23.7 nm) shown in **Figure 3d**. Besides, 1 to 2 grains of varying length can be measured along the surface normal direction within 43-nm thick L2NO4 layer. The chemical composition of the lamella was characterized by energy-dispersive X-ray spectroscopy (EDX), as shown by the EDX atomic depth profile (**Figure 4b**) and EDX maps (**Figure 4c**) of the lamella cross-section. These results show, from top to bottom, a clearly-delimited Pt capping layer, a continuous Ti top electrode, the L2NO4 memristive oxide layer and the Pt bottom electrode, with sharp interfaces between the layers of the heterostructure and a uniform La and Ni composition within the L2NO4 film thickness. In addition, the presence of oxygen within the Ti layer can be detected. This observation suggests the spontaneous formation of a  $\text{TiO}_x$  interlayer when Ti electrode is put in contact with L2NO4 film, prior to any thermal treatment process.



**Figure 4.** Cross-sectional transmission electron microscopy of Ti/L2NO4/Pt memristive device: a) STEM image, b) EDX atomic depth profile, c) EDX elemental maps for Ti (pink), O (green), La (yellow), Ni (cyan) and Pt (blue) showing the presence of oxygen within the top Ti electrode.

#### 2.4. Memristive characteristics of the Ti/L2NO4/Pt devices in vertical configuration

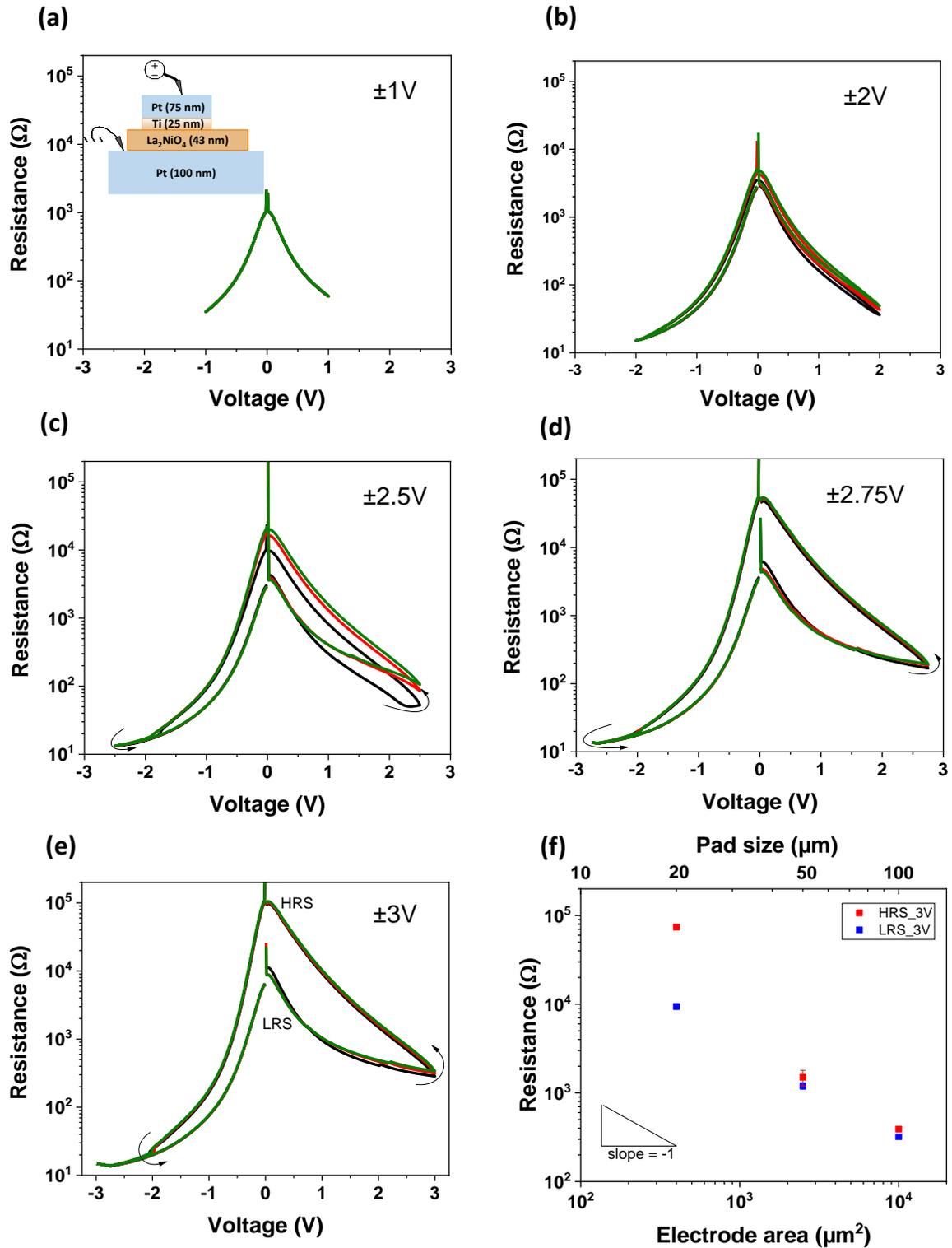
To study the RS behavior of the Ti/optimized L2NO4/Pt devices, beforehand the initial resistance states (IRS) were measured giving an average value of  $434 \Omega$  for the  $20^2 \mu\text{m}^2$  devices. The I-V characteristics were recorded by applying symmetric bipolar voltage sweeps ( $0 \text{ V} \rightarrow +V_{\text{max}} \rightarrow 0 \text{ V} \rightarrow -V_{\text{max}} \rightarrow 0 \text{ V}$ ). The HRS and LRS were read at  $+0.01 \text{ V}$  after each half-sweep. Firstly, an initialization process consisting of DC sweeps of increasing voltage amplitude (**Figure 5a-d**, plotted as R-V curves) was carried out to increase the Ti/L2NO4/Pt device to higher resistance state. Then the device operates at  $\pm 3 \text{ V}$ , as shown in **Figure 5e** (R-V plot). The first three sweeps between  $\pm 1 \text{ V}$  show non-linear and rectifying electrical properties (see **Figure 5a**) with a resistance of  $1 \text{ k}\Omega$  (read at low voltage). **Figure 5b** shows

that the resistance increases during the next three sweeps at  $|V_{\max}| = 2$  V and a small hysteresis starts to appear, however the two resistance states are not clearly distinguishable. A larger hysteresis with two noticeably different states is obtained for the Ti/L2NO4/Pt device when cycled between  $\pm 2.5$  V (**Figure 5c**). **Figure 5d** and **Figure 5e** show continuous R-V curves with gradual transition between resistance states at  $|V_{\max}| = 2.75$  V and  $|V_{\max}| = 3$  V, respectively, with a HRS/LRS ratio of around 11 for both working voltages. Thus it can be concluded that the Ti/optimized L2NO4/Pt devices can operate using  $|V_{\max}|$  in the range of 2.5-3 V. In all cases, the reset process takes place at positive voltages and the set process at negative voltages. A continuous gradual change in resistance during both the SET and RESET processes is observed, without any abrupt jumps, which is considered as a prerequisite of analogue-type device operation.

The observed RS is also compatible with a valence change mechanism taking place at the L2NO4/Ti interface. By the application of a positive voltage to the Ti electrode, the drift of oxygen ions would induce the further oxidation of the  $\text{TiO}_x$  interlayer, and the concomitant resistance increase. This oxidation would be reversed by the application of a negative voltage, leading to the reduction of the  $\text{TiO}_x$  interlayer and re-oxidation of the L2NO4 film. In addition, these results are in good agreement with the gradual memristive behaviour previously obtained on Pt/(epitaxial) L2NO4/Ti planar devices,<sup>[23, 28]</sup> which has now been successfully reproduced in vertical configuration for reduced dimensions devices and using lower operation voltages.

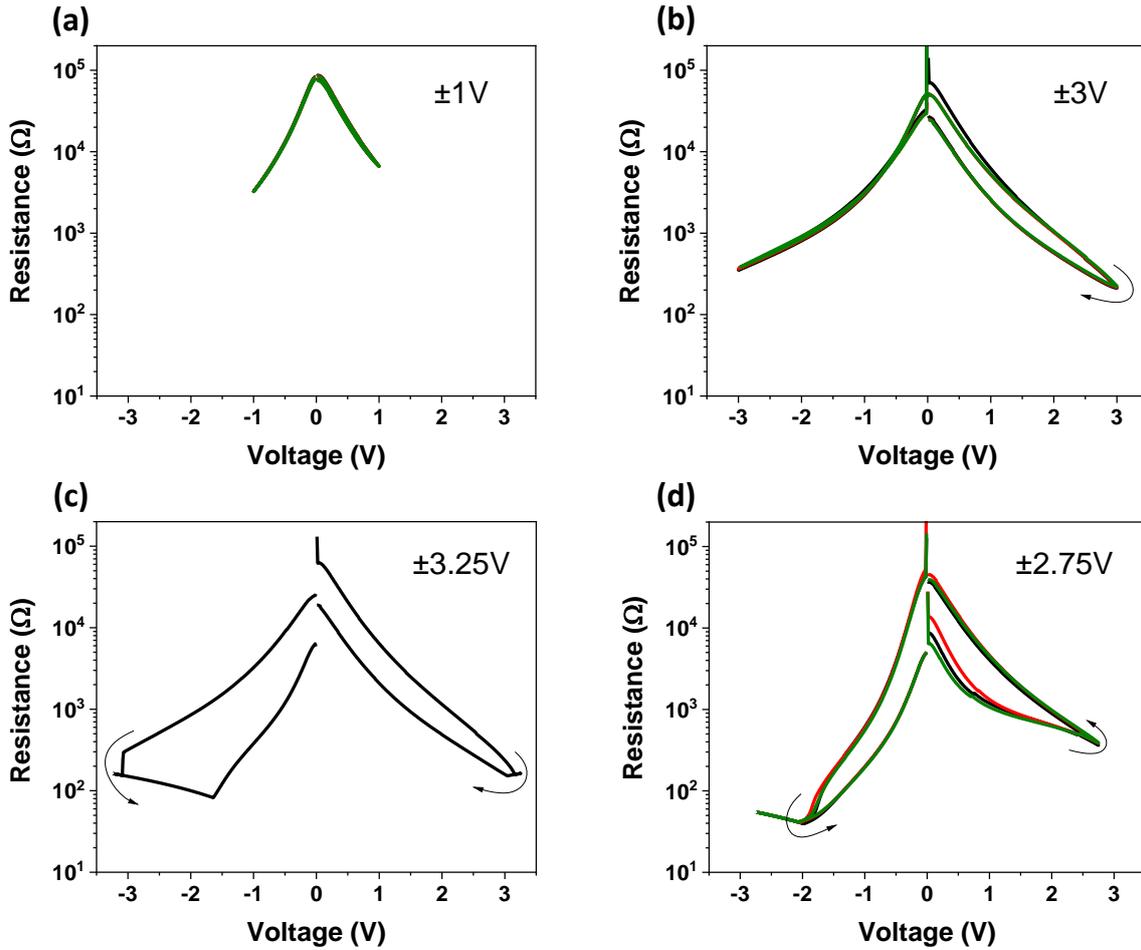
To verify the interfacial switching observed on Ti/optimized L2NO4/Pt devices, the electrode area dependence test was carried out. The HRS and LRS states were read at 10 mV after +3 V sweep and -3 V sweep, respectively, for different electrode sizes (i.e.,  $20^2 \mu\text{m}^2$ ,  $50^2 \mu\text{m}^2$ ,  $100^2 \mu\text{m}^2$ ). Three devices were measured for each pad size, except for the  $100^2 \mu\text{m}^2$  electrode, for which only one device measured because most of the  $100^2 \mu\text{m}^2$  suffered a breakdown at this operation voltage. This is most likely due to the presence of a leakage current resulting from

the presence of larger amount of defects in the larger device size, as often observed in the literature for other materials.<sup>[41]</sup> The average value of HRS and LRS are plotted as function of contact area in **Figure 5f**. This plot shows a clear decrease in HRS and LRS when increasing the pad size. The slopes are -1.66 and -1.05 for HRS and LRS, respectively. These results suggest that the change would not be limited to a single filament, but most probably takes place over the entire electrode area and, thus, the Ti/optimized L2NO4/Pt memristors present interface-type RS.



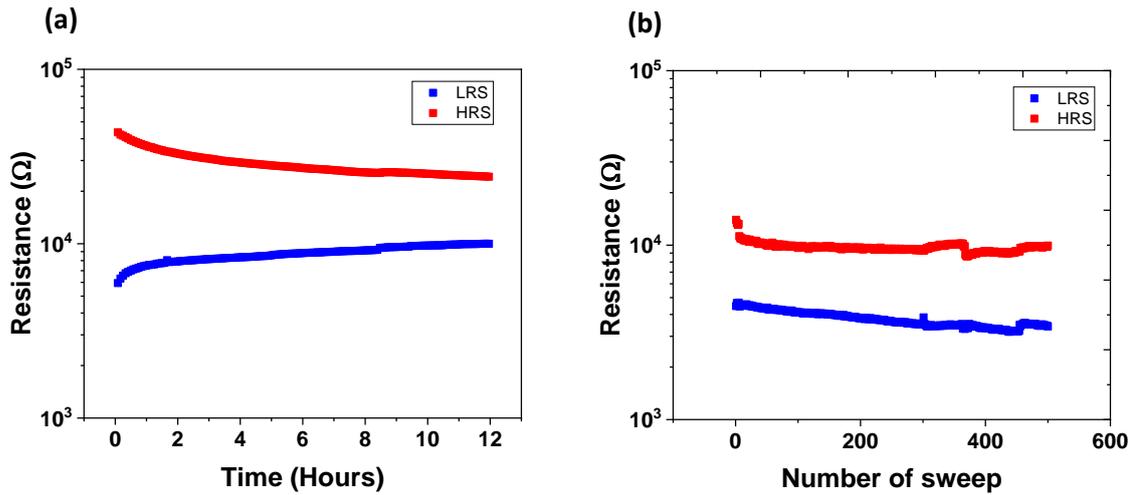
**Figure 5.** R-V characteristics of a Ti/optimized L2NO4/Pt device (size of device:  $20^2 \mu\text{m}^2$ , sketch shown as an inset) during the initialisation process: sweep cycles sequence  $0 \text{ V} \rightarrow +V_{\text{max}} \rightarrow 0 \text{ V} \rightarrow -V_{\text{max}} \rightarrow 0 \text{ V}$  for a)  $|V_{\text{max}}| = 1 \text{ V}$ , b)  $|V_{\text{max}}| = 2 \text{ V}$ , c)  $|V_{\text{max}}| = 2.5 \text{ V}$ , d)  $|V_{\text{max}}| = 2.75 \text{ V}$ . e) R-V characteristics at  $|V_{\text{max}}| = 3 \text{ V}$  after the initialisation process of the same Ti/L2NO4/Pt device and f) Electrode-area dependence resistance for  $|V_{\text{max}}| = 3 \text{ V}$  (average of 3 devices for the small pad sizes, while only 1 device is presented for the largest pad size). 1<sup>st</sup> sweep: black, 2<sup>nd</sup> sweep: red, 3<sup>rd</sup> sweep: green.

To compare the switching properties of memristive devices based on non-optimized L2NO4 films and the previously shown results on the optimized L2NO4 films, beforehand the IRS of the  $20^2 \mu\text{m}^2$  devices was measured giving the average value of  $48.8 \text{ k}\Omega$ . Then, standard IV sweeps with different  $|V_{\text{max}}|$  were carried out on the Ti/non-optimized L2NO4/Pt devices. **Figure 6a** presents the non-linear electrical properties with the resistance of roughly  $87 \text{ k}\Omega$ . Next, the sweeps at  $\pm 2\text{V}$ ,  $\pm 2.5\text{V}$ ,  $\pm 2.75\text{V}$ ,  $\pm 3\text{V}$  were carried out. The sweeps at  $\pm 3\text{V}$  are displayed (**Figure 6b**) in this article showing that, by increasing the  $|V_{\text{max}}|$ , the device resistance decreases. In the positive branch, the hysteresis starts to appear with eightwise switching sense. An abrupt change in resistance to lower values, hereafter referred to as ‘forming’ step, can be observed at  $\pm 3.25 \text{ V}$  sweep, as indicated in **Figure 6c**. After the ‘forming’, the device can operate at a lower working voltage range ( $|V_{\text{max}}| = 2.75 \text{ V}$ ) as shown in **Figure 6d**, with a HRS/LRS ratio of 6 in this case. We propose that, the much higher IRS measured for the non-optimized L2NO4 devices compared to the optimized L2NO4 devices ( $48.8 \text{ k}\Omega$  vs  $434 \Omega$ , respectively) could be due to the presence of the  $\text{La}_2\text{CO}_5$  impurity phase observed by XRD, and that the abrupt resistance change could be due to the breakdown of this impurity blocking layer, reaching then the standard operation cycles of the optimized L2NO4-based devices. It should be noted that this process is not the classical electroforming occurring in filamentary VCMs, where a conducting filament is created within the switching layer.



**Figure 6.** R-V characteristics of Ti/non-optimized L2NO4/Pt device in  $20^2 \mu\text{m}^2$  size a-b) before the forming, c) at the forming, d) after the forming. Sweep cycles following the sequence  $0 \text{ V} \rightarrow +V_{\text{max}} \rightarrow 0 \text{ V} \rightarrow -V_{\text{max}} \rightarrow 0 \text{ V}$  for a)  $|V_{\text{max}}| = 1 \text{ V}$ , b)  $|V_{\text{max}}| = 3 \text{ V}$ , c)  $|V_{\text{max}}| = 3.25 \text{ V}$ , d)  $|V_{\text{max}}| = 2.75 \text{ V}$ . 1<sup>st</sup> sweep: black, 2<sup>nd</sup> sweep: red, 3<sup>rd</sup> sweep: green.

In order to study the RS performance, another  $20^2 \mu\text{m}^2$  Ti/optimized L2NO4/Pt memristor was selected to test the data retention and the endurance. **Figure 7a** shows the retention of the device measured after an initialization process followed by 5 cycles at  $\pm 2.5 \text{ V}$ . A decrease of the HRS from 43.4 to 24.2 k $\Omega$  (56%) and an increase of LRS from 5.9 to 10.0 k $\Omega$  (169%) are observed after 12 hours. The dynamic resistance relaxation of HRS was previously observed in Ti/200 $\mu\text{m}$ -L2NO4/Pt devices and is attributed to the oxygen mass transport between p-type L2NO4 and n-type TiO<sub>x</sub>.<sup>[28]</sup> **Figure 7b** shows the resistances (read at 0.01V after  $\pm 2.5 \text{ V}$  sweep) as function of the number of sweeps (500 consecutive sweeps) showing no overlap of the HRS and LRS states.



**Figure 7.** a) Resistance vs time measured for the HRS (red square dot) and the LRS (blue square dot) with a reading amplitude of 10 mV. Resistance were measured at 0.01 V every 5 minutes. b) Endurance plot recorded by measuring 500 consecutive sweeps. The HRS and LRS were programmed by the sweeps at  $\pm 2.5$  V

### 3. Conclusions

Optimized flat and dense polycrystalline L2NO4 thin films (43 nm thick) have been deposited by PI-MOCVD on a platinized silicon substrate by PI-MOCVD, after an optimization process in which the deposition temperature and the La/Ni atomic ratio of the precursor solution were tuned. The purity of L2NO4 phase in thin film was confirmed by XRD pattern and by the measured La/Ni ratio of close to 2 using EPMA technique. Ti/L2NO4/Pt memristive devices have been fabricated in vertical configuration for the first time, using L2NO4 thin films deposited under the previously optimized conditions. A TiO<sub>x</sub> interlayer was observed by STEM-EDX analysis when evaporating Ti on top of L2NO4 memristive film. The Ti/L2NO4/Pt devices present gradual transitions between the HRS and LRS states, suggesting bipolar analog RS can be obtained. In addition, the Ti/optimized L2NO4/Pt memristive devices are forming-free with dynamic resistance relaxation during 12 hours and good cyclability; whereas the Ti/non-optimized L2NO4/Pt devices have a higher initial resistance and require a ‘forming’ step before exhibiting similar RS characteristics to the optimized ones. This work constitutes the first proof of the successful integration of vertical L2NO4-

based memristors on silicon-based wafers and allows for the future development of these promising redox-based memristive devices in applications such as artificial synapses for neuromorphic computing with bio-inspired learning

#### 4. Experimental Section

*Thin film deposition:* Polycrystalline  $\text{La}_2\text{NiO}_{4+\delta}$  (L2NO4) thin films were synthesized by PI-MOCVD.<sup>[34, 42]</sup>  $\text{La}(\text{tmhd})_3$  (tris(2,2,6,6-tetramethyl-3,5-heptanedionato)lanthanum(III)) and  $[\text{Ni}(\text{tmhd})_2]$  (bis(2,2,6,6-tetramethyl-3,5-heptanedionato)nickel(II)) from Strem Chemicals were used as precursors. They were mixed in a solution with m-xylene (1,3-dimethylbenzene) from Alfa Aesa. Pt (100 nm)/TiO<sub>2</sub> (20 nm)/SiO<sub>2</sub> (500 nm)/Si (750  $\mu\text{m}$ )/SiO<sub>2</sub> (500 nm) wafers (from CEA-Leti), cut in 1x1cm<sup>2</sup> chips, were used to grow the L2NO4 thin films. The growth conditions for L2NO4 thin films used in this work are detailed in Table 2.

**Table 2.** Deposition conditions used for the growth of L2NO4 thin films by PI-MOCVD

Parameters	Value
Precursors	$\text{La}(\text{tmhd})_3$ and $\text{Ni}(\text{tmhd})_2$
Solution concentration (mol/L)	0.02
Injection frequency (Hz)	1
Opening time (ms)	2
Number of pulses	2000
Evaporation temperature (°C)	220-280
Substrate temperature (°C)	600-650
Carrier gas (sccm)	218 (34% Ar) + 418 (66% O <sub>2</sub> )
Total pressure inside the reactor (Torr)	5

*Instrumentation:* To identify the phase and evaluate the structural crystal quality of the samples, X-ray diffraction was performed in a 5-circle Rigaku Smartlab diffractometer. GI-XRD was used to enhance the diffraction signal from the polycrystalline films and minimize the signal of the silicon-based substrates. The study of surface morphology was carried out by SEM in a SEM FEG ZEISS GeminiSEM 300. To investigate the film roughness, AFM images were performed using AFM D3100 Veeco Instrument in tapping mode with a Si<sub>3</sub>N<sub>4</sub> tip probe. The chemical film composition was analyzed by EPMA using a CAMECA SX100

spectrometer. Each film was measured at two different acceleration voltages: 12 keV and 16 keV and the data analysis was done by Strategem software. The TEM-EDX analyses were performed at 200 kV using a probe corrected Tecnai Osiris FEI microscope equipped with the Super-X detector system. Prior to the TEM examination, the sample was prepared by FIB milling using a FEI dual-beam Helios 450S. The lamella was covered by a platinum layer to ensure surface protection from the tails of the ion beam. A 30 kV operation voltage was used for the rough milling and then a reduction in the range 2-8 kV to limit the surface damages. Finally, the sample was cleaned with a very soft oxygen-argon plasma to remove surface hydrocarbon contamination, process from which no ion implantation is expected.

The device fabrication was carried out in clean-room facilities (PTA, Grenoble), including metal evaporation (Plassys MEB550) using laser lithography (Heidelberg instrument  $\mu$ PG 101). Metal electrodes were then patterned (by laser lithography) and evaporated on top of the L2NO4 thin films, i.e., 25 nm of Ti followed by 75 nm of Pt (Ti acts as the active electrode, covered by capping Pt layer in order to protect Ti from oxidation with the atmosphere).

The Ti/L2NO4/Pt devices were then exposed to a fast heating process (RTA) in Ar atmosphere consisting of a fast anneal at approximately 400 °C for 100 s. RTA is expected to supply the thermal energy required to further oxidize the  $\text{TiO}_x$  interlayer by the incorporation of oxygen from L2NO4 into the Ti layer.

The electrical measurements (triangular voltage sweeps) were performed under ambient conditions using a source-measurement unit (Keithley 4200 semiconductor parameter analyzer) and two external micromanipulators. For all the I-V plots shown in this work, the voltage was applied on the  $20 \times 20 \mu\text{m}^2$  Pt/Ti electrode while Pt bottom electrode was grounded. The bipolar triangular voltage sweeps always start from zero bias and follow this sense:  $0 \text{ V} \rightarrow +V_{max} \rightarrow 0 \text{ V} \rightarrow -V_{max} \rightarrow 0 \text{ V}$ . The resistance state (HRS and LRS) was read by applying a reading test  $0 \text{ V} \rightarrow +0.01 \text{ V}$  and measuring the corresponding current at 0.01 V after individual half sweep:  $0 \text{ V} \rightarrow +V_{max} \rightarrow 0 \text{ V}$  or  $0 \text{ V} \rightarrow -V_{max} \rightarrow 0 \text{ V}$ .

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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