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Thorough Investigation of Low Frequency Noise Mechanisms in AlGa_N/Ga_N and Al₂O₃/Ga_N HEMTs

R. Kom Kammeugne^{1,2}, C. Theodorou², C. Leroux¹, X. Mescot², L. Vauche¹, R. Gwoziecki¹, S. Becu¹, M. Charles¹, E. Bano² and G. Ghibaudo²

¹Univ. Grenoble Alpes, CEA-LETI F38054, Grenoble, France, email: romeo.komkammeugne@cea.fr

²Univ. Grenoble Alpes, Univ. Savoie Mont Blanc, CNRS, Grenoble INP, IMEP-LAHC, Grenoble, 38000, France

Abstract—This paper investigates the AlGa_N/Ga_N and Al₂O₃/Ga_N interface quality on Ga_N MIS-HEMT using low frequency noise (LFN) measurements. To address the issue of noise in the access resistance, we have also tested “non-gated” 2DEG devices. The LFN has a 1/f-like behaviour caused by trapping/de-trapping processes which has been well described by carrier number fluctuations (CNF) and correlated mobility fluctuation (CMF) models. The border trap density extracted in optimised devices is better than previously reported Ga_N data and close to silicon CMOS results. Finally, a noise model for Ga_N-HEMT with recessed MIS gate including a 2DEG access resistance noise source is proposed.

I. INTRODUCTION

AlGa_N/Ga_N-based High Electron Mobility transistors (HEMTs) have attracted a lot of attention in power electronics and RF applications. This is due to the high electron density in the 2D electron gas (2DEG), high electron mobility at AlGa_N/Ga_N interface, and large band gap of Ga_N [1]–[3]. Low frequency noise (LFN) is one of the key parameters in RF and analog circuit design, such as voltagecontrolled oscillators, mixers, and amplifiers [4]. In FET devices, the 1/f-like noise mainly stems from trapping-induced carrier number fluctuations (CNF), as described in the McWhorter model [5], but also from correlated mobility fluctuations (CMF) [6], [7]. These models are classically used for LFN analysis in intrinsic MOS transistors, but, as in Ga_N HEMTs ([8]–[10], [4], [10]), significant access resistance LF noise should also be included, justifying the use of a specific resistance noise contribution modelling [7]. In this study, we present for the first time a detailed analysis of the LF noise both in the 2DEG access resistance and in intrinsic Ga_N HEMT transistors. To this end, we first perform LFN measurements on non-gated 2DEG AlGa_N/Ga_N structures emulating the access resistance in HEMTs. Then, we measure the LFN in Ga_N MIS-HEMTs featuring various gate recess depths (Normally on/off) and different fabrication processes.

II. DEVICES AND EXPERIMENTAL SETUP

The electrical measurements were performed on different wafers processed with “non-gated” (Fig. 1a) and “gated” structures (both normally-On (Fig. 1b) and normally-Off (Fig. 1c)). Ga_N epitaxy is performed by Metal-Organic Chemical Vapor Deposition (MOCVD) on 200 mm diameter silicon (111) substrates. The structure is composed of an AlN nucleation layer, an AlGa_N based buffer, C-doped Ga_N buffer layers to ensure a high breakdown voltage, then an unintentionally doped (UID) Ga_N channel. The piezoelectric effect to form the 2DEG is obtained with the growth of AlN and Al_xGa_{1-x}N on the Ga_N channel, followed by in-situ deposition of a passivation layer [11], [12]. Test structures reported in this study were fabricated using two different process flows (Recipe 1, Recipe 2). Recipe 1 is simplified, and differences consist mainly in Ohmic contact and gate etching processes (Table 1).

Wafers 0 to 6 correspond to different gate recess depths, from no

gate recess (RD0) to deep gate recess (RD6). Fig. 2a shows the corresponding recess depths in arbitrary units. The MIS-HEMT Al₂O₃ gate oxide is deposited by Atomic Layer Deposition. Fig. 2b shows a cross sectional TEM image of the fully recessed MIS-gate with different typical interfaces. The noise measurements were performed on “non-gated” structures (Fig. 1a) having various distances between contacts (5 to 32 μm) and “gated” MIS structures (Fig. 1b and 1c) with different gate lengths (0.25 to 2 μm).

III. LFN OF “NON-GATED” GAN-BASED STRUCTURE

Noise measurements have been first performed on “non-gated” structures. Fig. 3a reports a typical LFN power spectral density (PSD) in log scale for different biasing. The slope close to 1 confirms the 1/f-like noise nature and the variation with bias corresponds to the well-known dependence with current squared (symbols in Fig. 4 b). In Fig. 3c, resistance values versus distance *d* between contacts are shown. A linear and constant dependence observed for recipe 2 (wafers #3 to #5) attests to the good control of 2DEG resistance and Ohmic contacts. For recipe 1, contact resistances are higher and more varied, especially for wafers #1 and #2. Equations 1.a, 1.b and 1.c summarize the LF noise CNF model for a “non-gated” device and accounting for 2DEG conductance fluctuations due to random trapping-detrapping (GR) of electron in traps located at the AlGa_N/Ga_N interface [13]. Equation (1.a) gives the corresponding PSD related to the trap time constant (τ) and variance ($\langle \Delta N_{\text{trap}}^2 \rangle$). With a Poisson law for the trap distribution, the variance equals the mean value of traps (Eq. 1.b). The condition of electro-neutrality implies a correspondence between trap number variation (ΔN_{st}) and 2DEG carrier density variations (ΔN), yielding a PSD equation with areal trap density N_{st} (Eq. 1.c) [13], [14]. Fig. 4a shows that the 1/f conductance PSD properly scales with resistance length, as confirmed by normalized plot in Fig. 4(b) for a given frequency. The slight increase of the normalised PSD for smaller lengths could be related to specific noise in the contact. Wafer 1 and 2 have the most degraded contact resistance (Fig. 3(c)), such that, in this case, the LF noise is no longer scaling with dimension and is dominated by contact resistance noise (Fig. 5). The resistance noise $S_R = R_{\text{on}}^{-2} (S_I)^2$, is compared for the different wafers in Fig. 6(a). Using Eq. 1.c, the corresponding areal trap density N_{st} has been extracted, showing the impact of the recipe (Fig. 6(b)). Extraction of N_{st} is not meaningful for wafers 1 & 2 where LF noise is dominated by a large contact resistance.

IV. LFN OF “GATED” GAN MIS-HEMT

Capacitance versus bias (C-V) measurements for the different recess depths are shown in Fig. 7a. Normally-On devices exhibit CV double plateau behaviour for accumulation, first at the AlGa_N interface and then at the Al₂O₃ interface. The maximum capacitance C_{ox} at 0 V for normally-On and 6 V for normally-Off devices (Fig. 7b) is a function of the distance between channel and metal gate. The associated channel mobility (Fig. 7c) is clearly reduced in the case of a Ga_N/Al₂O₃ interface. The LFN spectra were measured for the (L_g). Fig. 8 (a) reports LFN for a “gated” structure (HEMT)

at different gate lengths. Fig. 8b illustrates the influence of process for a given gate length. Although RD2 and RD3 are close (Fig. 2a), the difference in their process flow significantly affects the noise level. The variability of current and noise has been investigated on 25 devices. Even if a certain distribution can be observed due to mobility, threshold voltage and access resistance, $(g_m/I_d)^2$ normalized characteristics are close (Fig. 9a). Similarly, input referred gate noise spectra ($S_{V_g}=S_{I_d}/g_m^2$) follows the same trend (Fig. 9b) typical of its architecture and design that we will investigate through modelling.

A. Diagnostic of the LFN source in GaN based HEMTs

The MOSFET 1/f-like noise has been classically interpreted by McWhorter CNF model for S_{I_d}/I_d^2 (see Eq. 2.a) [5], [6] which includes the flat band voltage spectral density, $S_{V_{fb}}$. The model for $S_{V_{fb}}$ (Eq. 2.b) accounts for the impact of trapping/de-trapping on the flat band voltage. It depends on the spatial trap density (N_{trap}), the effective channel area ($W \cdot L_{eff}$), the frequency (f), and the tunnelling constant between channel and traps (λ) (Eq. 2.c) [15]. A more advanced model [6], [7] proposes to account for the correlated mobility fluctuations (CMF) (Eq. 2.d). Notice that a specific term (S_{RSD} / R_{ON}^2) related to the access resistance has also been added. The CMF model implies a correlated mobility factor (Eq. 2.c, $\Omega=\alpha_{SC}\cdot\mu_{eff}\cdot C_{ox}$). To remove the effect of access resistances on the HEMT gain, a Y-function-based method [16]–[18] was used to evaluate μ_{eff} and intrinsic HEMT gain I_d/g_{m0} (Eq. 2.d) and input referred gate noise spectra (Eq. 2.e). Fig.10 (a) and (b) report the normalized drain current noise at 20 Hz for two different gate lengths and the same wafer (# 4). As can be seen, the CNF/CMF model accounts well for the noise variation across the whole range of current. For this wafer, the level of noise related to the access [$S_R = R_{ON}^2(S_I/I^2)$] is low and the scaling of the noise PSD with gate area is well verified for the different gate lengths. The square root of input referred noise is expected to depend linearly on intrinsic gain factor (Eq. 2.e). This is verified experimentally and fitted by the CNF/CMF model at different gate lengths and recess depths (Fig. 11), enabling extraction of the correlated mobility factor Ω . For recipe 1, the degraded access resistances affect the noise results (Figs. 12a and 12b). The extracted access noise levels SRSD (Fig.12c) are comparable to the values measured on “non-gated” structures (Fig. 6a). The dependence of $\sqrt{S_{V_g}}$ versus I_d/g_{m0} (Fig. 11) also enables the extraction of $S_{V_{fb}}$ and thus trap densities for the different wafers (Fig. 13). For both recipes, an increase of trap densities is seen with recess depth. The effect is larger for recipe 1 as we go to normally-Off transistors (Fig. 13a), but it is moderate for recipe 2 (Fig. 13b). Measurements at different temperatures confirm the validity of the CNF model and thus extracted values (Fig. 13c). The different values of spatial trap densities obtained on this wafer are benchmarked to values reported in the literature for various GaN [4], [8], [10], [19]–[24] and silicon CMOS [25]–[27] technologies (Fig. 14). The N_{trap} obtained in this study is significantly better than previously reported GaN results (except wafer 2) and comparable to silicon based MOSFETs. In Fig. 15, the different correlated mobility factors measured at different recess depths and gate lengths are summarized. The observed decrease of Ω with mobility is not expected $\Omega=\alpha_{SC}\cdot\mu_{eff}\cdot C_{ox}$ but the “three transistors model” presented below will explain this behaviour.

V. NEW CNF/CMF NOISE MODEL FOR HEMT WITH RECESSED MIS-GATE

To build a complete model for normally-Off GaN HEMTs, we rely on our previous I_d - V_g characteristics analysis which accounts for three transistors in series [28]. This model includes two access resistances at the source and drain, two edge transistors due to the recess structure and an intrinsic transistor as a bottom channel, all placed in series. In such a model, the total device resistance, $R_{ON}(V_g)=R_{Access}+R_{Edge}(V_g)+R_{Channel}(V_g)$ where edge and intrinsic transistors have their own transconductance parameters. The total LFN is thus obtained by adding the independent PSD of each resistance. This leads therefore to 3 terms for the normalized PSD (Eq. 3.a), where the noise induced by edge and intrinsic transistors is depicted by the CNF/CMF model with proper parameters (Eq. 3.b, Eq. 3.c and Eq. 3.d). The $I_d(V_g)$ curves and the normalized current PSD have been well modelled (see Fig.16a and b). For “non-gated” structures we find $N_{st}=2\times 10^{12}eV^{-1}cm^{-2}$ For the bottom channel and the edge transistors, the border trap densities are respectively $N_{Trap_Ch}=2.5\times 10^{17}eV^{-1}cm^{-3}$ and $N_{Trap_Ed}=1.1\times 10^{18}eV^{-1}cm^{-3}$ and the Coulomb scattering coefficients transistors $\alpha_{SC_Ch}=4\times 10^4 (V.s)C$ and $\alpha_{SC_Ed}=9.2\times 10^4 (V.s)C$. Note that it is the same set of parameters that enables a good fit for the different gate lengths.

VI. CONCLUSION

A thorough LFN analysis of GaN HEMT has been presented for “non gated” (access) and “gated” structures in linear regimes for different device architectures and process flows. The density of traps (surface traps at AlGaIn/GaN interface and spatial traps into the gate oxide) extracted from LF noise analysis is at the state-of-the-art for GaN devices and close to values reported for Silicon based MOSFETs. Finally, a new LFN model has also been developed for recessed GaN MIS-HEMTs, enabling both DC $I_d(V_g)$ and LFN detailed analysis of access, edge recess and intrinsic bottom channel contributions.

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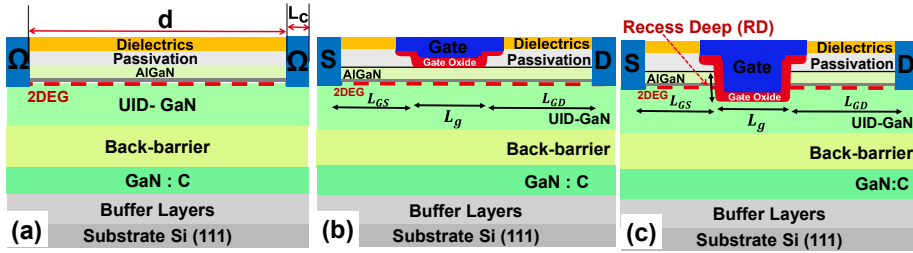


Fig. 1: Schematic cross section of AlGaIn/GaN HEMT stack (a) non-gated test structure, (b) normally-on without recess depth (RD=0 a. u.) and (c) normally-off with recess depth (RD≠0 a. u.).

Wafer	#0	#1	#2	#3	#4	#5	#6
Process flow	Recipe 1			Recipe 2			
Device	Normally-On			Normally-Off			
Recess depth	RD0	RD1	RD2	RD3	RD4	RD5	RD6

Table 1: Process flow of AlGaIn/GaN HEMT devices

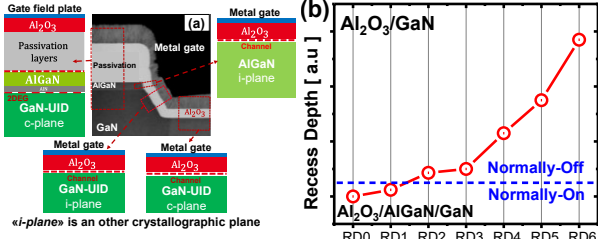


Fig. 2: (a) Cross-sectional TEM image of the recessed MIS gate with different typical interfaces and (b) recess depth for different tested wafers.

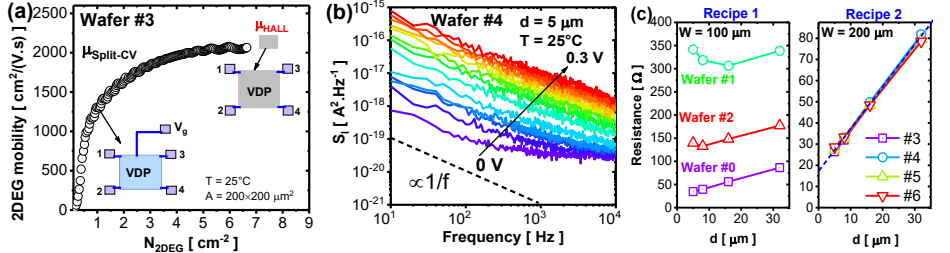


Fig. 3: (a) Comparison between 2D gas mobility versus N_{2DEG} on AlGaIn/GaN-based Van Der Pauw structure obtained by Effect-Hall and split-CV methods, (b) Typical drain current noise versus frequency S_1 on non-gated structure for different voltages and (c) Resistance versus contact length d on different wafers.

Non-gated structure

Carrier number fluctuations (CNF) ΔN

$$S_{N_{trap}}(f) = \frac{4 \langle \Delta N_{trap}^2 \rangle \tau}{1 + (2\pi f \tau)^2} \quad (1.a)$$

$$\langle \Delta N_{trap}^2 \rangle = \int_0^\infty S_{N_{trap}}(f) df = \langle N_{trap} \rangle = k_B T N_{st} W d \quad (1.b)$$

Condition of global charge neutrality: $\Delta N = -\Delta N_{trap}$

$$\frac{S_I}{I^2} = \frac{S_R}{R^2} = \frac{S_{N_{st}}}{N^2} = \frac{k_B T N_{st} W d}{f \cdot N^2} \quad (1.c)$$

where $N = n_s \cdot W \cdot d$, the total carrier number and n_s the carrier concentration.

Eq. 1: Noise model for non-gated structure [11].

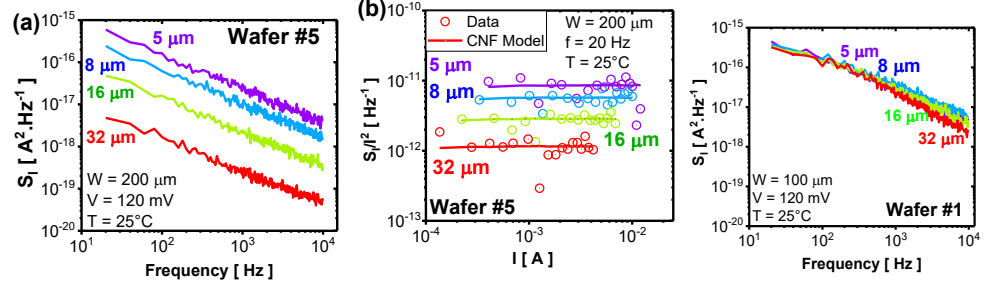


Fig. 4: (a) The drain current noise versus frequency and (b) normalized current power spectral density versus current for different non-gated structure lengths showing the scaling on optimized non-gated test structures.

Fig. 5: Same as Fig.4 (a) for wafer #1 with degraded contact resistance.

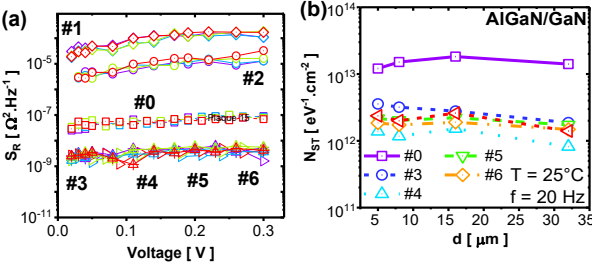


Fig. 6: (a) total resistance noise versus voltage and (b) surface trap density at AlGaIn/GaN interface versus test structure non-gated structure length for the different wafers.

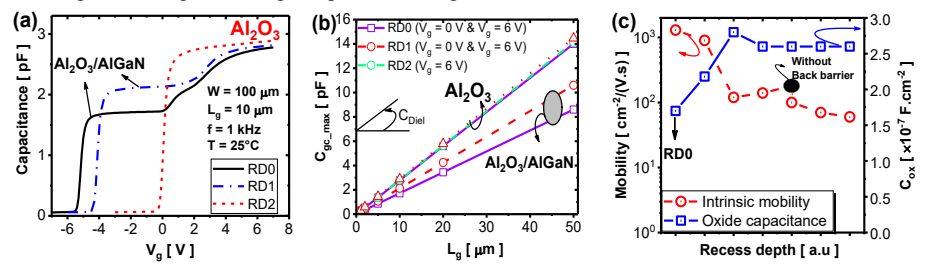


Fig. 7: (a) Capacitance versus gate voltage V_g and (b) maximum capacitance at $V_g = 0$ V (normally on devices) and $V=6$ V (normally off devices) versus L_g on GaN-HEMT for different recess depths and (c) intrinsic mobility and dielectric capacitance versus recess depth (RD).

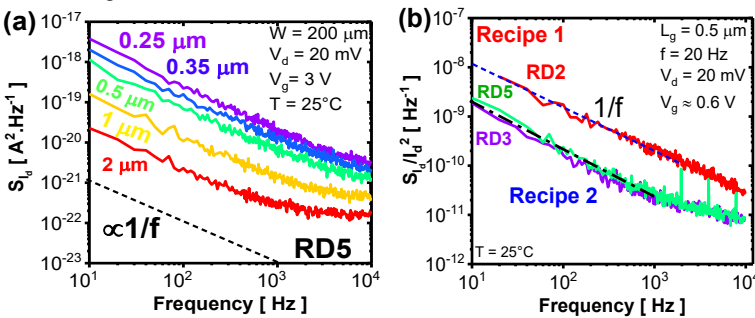


Fig. 8: (a) Drain current noise versus frequency on optimized normally off MIS-GaN HEMT (Wafer #5) and (b) comparison between normalized drain current PSD for different wafers.

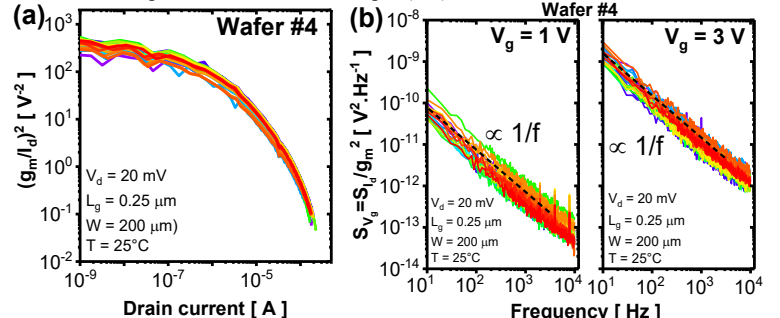


Fig. 9: (a) $(g_m/I_a)^2$ characteristics with logarithmic scale and (b) Input-referred gate voltage noise S_{id}/g_m^2 versus frequency for 25 devices with $L_g=0.25 \mu m$ at two different biases (1V and 3V)

MIS-HEMT
- Carrier number fluctuations (CNF) ΔN

$$\frac{S_{I_d}}{I_d^2} = \left(\frac{g_m}{I_d}\right)^2 \cdot S_{V_{fb}} \quad (2.a)$$

$$S_{V_{fb}} = \frac{q^2 \cdot \lambda \cdot k_B T}{f \cdot W \cdot C_{ox} \cdot L_{eff}} \left(\frac{N_{trap}}{L_{bot}}\right) \quad (2.b)$$

where λ is the tunneling attenuation coefficient:

$$\lambda = \left[\frac{q}{n} \cdot \sqrt{2q \cdot m^* \cdot Al_2O_3 \cdot \Phi_B}\right]^{-1} \quad (2.c)$$

- Correlated mobility fluctuations (CMF) $\Delta N/\Delta \mu$

$$\frac{S_{I_d}}{I_d^2} = \underbrace{\left(\frac{g_m}{I_d}\right)^2 \cdot S_{V_{fb}} \left(1 \pm \Omega \cdot \frac{I_d}{g_{m,0}}\right)^2}_{\text{Channel}} + \underbrace{\left(\frac{I_d}{V_d}\right)^2 S_{R_{SD}}}_{\text{Access}} \quad (2.d)$$

$$\frac{I_d}{g_{m,0}} = \frac{n k T}{q} + \frac{y}{\sqrt{\beta V_d}} \left[1 + \theta_{1,0} \frac{y}{\sqrt{\beta V_d}}\right] \quad (2.e)$$

$$\sqrt{S_{V_g}} = \sqrt{S_{V_{fb}} \left(1 \pm \Omega \cdot \frac{I_d}{g_{m,0}}\right)} \quad (2.f)$$

Fig. 2: CNF (3.a) and CNF/CMF (3.d) models for gated structure [5], [6].

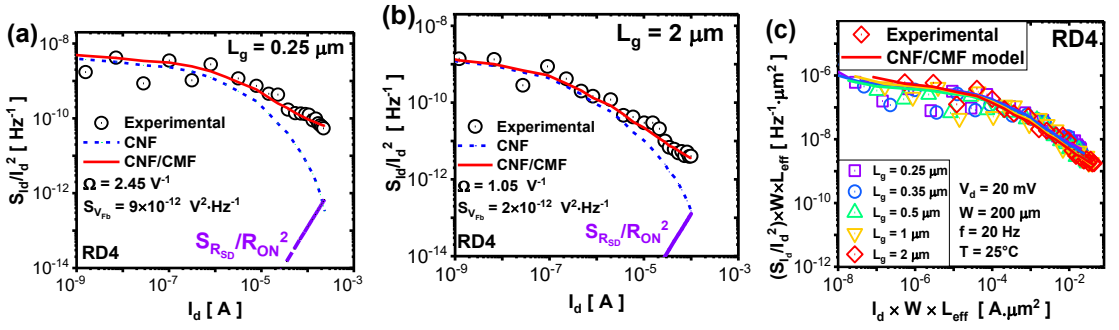


Fig. 10: Comparison between experimental of normalized drain current noise S_{I_d}/I_d^2 versus I_d with logarithmic scale, compared with CNF and CNF/CMF models for two gate lengths (a) $0.25 \mu\text{m}$ length ($S_{V_{fb}}=9 \times 10^{-12} \text{ V}^2 \cdot \text{Hz}^{-1}$ and $\Omega=2.45 \text{ V}^{-1}$) and (b) $2 \mu\text{m}$ length ($S_{V_{fb}}=2 \times 10^{-12} \text{ V}^2 \cdot \text{Hz}^{-1}$ and $\Omega=1.05 \text{ V}^{-1}$) and (c) normalized drain current noise level with device area for the different gate lengths on GaN-HEMT with recessed MIS gate.

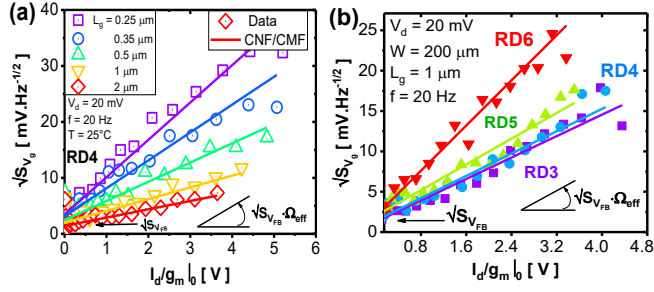


Fig. 11: Experimental and CNF/CMF model of square root of input-referred noise $\sqrt{S_{V_g}}$ versus intrinsic ratio of drain current and transconductance $I_d/g_{m,0}$ for (a) different gate lengths and (b) recess depths on optimized recipe.

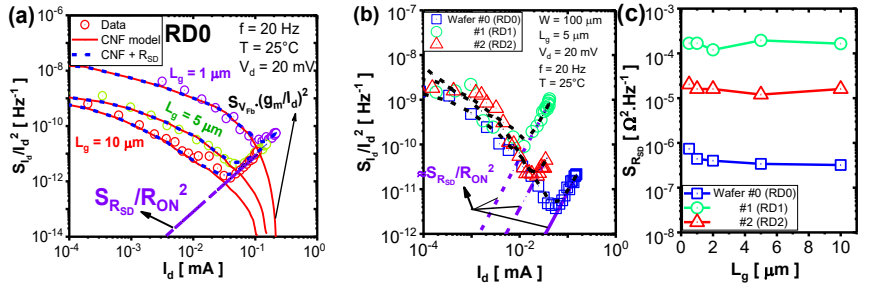


Fig. 12: (a) Comparison of experimental normalized drain current S_{I_d}/I_d^2 versus drain current I_d on RD0, compared with CNF-model and CNF model with access noise with different gate lengths, (b) comparison on different wafers with different RD showing the access noise issue and (c) the extracted access noise level $S_{R_{SD}}$ versus gate lengths for different wafers.

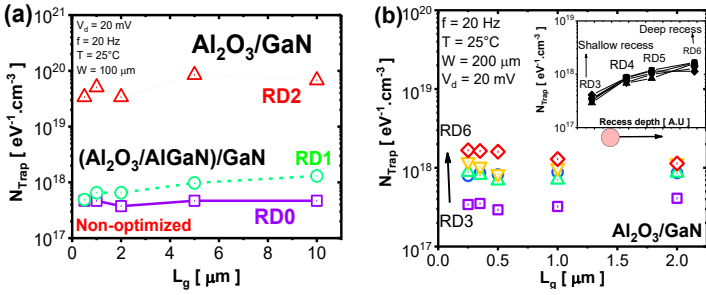


Fig. 13: Effective spatial trap density N_{Trap} versus gate length for various recess depths on (a) non-optimized technologies and (b) reference process GaN-HEMT and (c) N_{Trap} versus $1000/T$.

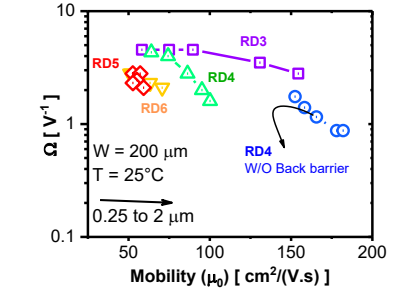


Fig. 15: Correlated mobility coefficient versus low field mobility μ_0 for different RD on GaN-HEMTs with recessed MIS gate.

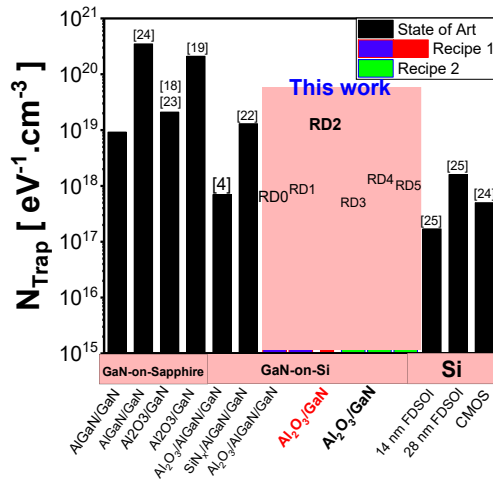
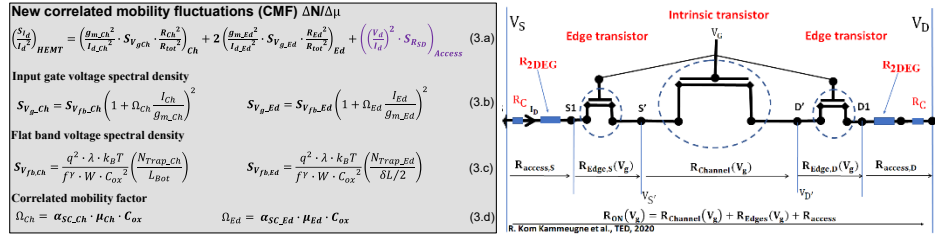


Fig. 14: Benchmarking of the mean trap density (N_{Trap}) for GaN-HEMT devices of this work with state of art GaN-based, FDSOI and CMOS technologies.



Eq. 3: New CNF/CMF and corresponding electrical model for GaN HEMT devices with recessed MIS-gate structure.

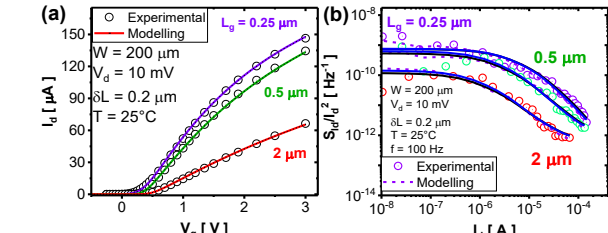


Fig. 16: Comparison between data and new model of (a) I_d - V_g characteristics and (b) normalized drain current S_{I_d}/I_d^2 versus I_d for different gate length. This model enables us to discriminate between intrinsic

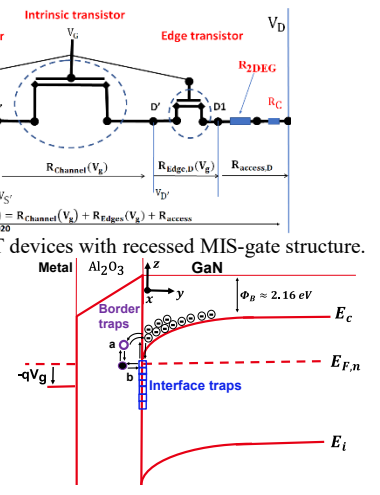


Fig. 17: Energy band diagram showing the tunnelling mechanism of electrons between the conduction band