

Foreground Static Error Calibration for Current Sources Using Backgate Body Biasing

Clément Beauquier^{§*1}, David Duperray[#], Chadi Jabbour[§], Patricia Desgreys[§], Antoine Frappé*, Andreas Kaiser*

[#]STMicroelectronics, Grenoble, France

[§]LTCI - Laboratoire de Traitement et Communication de l'Information, Telecom Paris,

Institut Polytechnique de Paris, Palaiseau, France

*Univ. Lille, CNRS, Centrale Lille, Junia, Univ. Polytechnique Hauts-de-France, UMR 8520 - IEMN -

Institut d'Electronique de Microélectronique et de Nanotechnologie, F-59000 Lille

¹clement.beauquier@ext.junia.com

Abstract—This work presents a detection and calibration circuit for current sources static mismatch introduced by the process of fabrication. The current is corrected through backgate body bias voltage control, which has the benefit of reduced additional parasitic elements, compared to more classic amplitude calibration or sort-and-map solutions. The main application are high speed and high resolution current steering Digital to Analog Converters (DAC). The calibration circuit is applied on a 2 time-interleaved (TI) DAC, with 12 bits of resolution and sampled at a frequency of 16 GHz. Its main requirement is to be able to generate signals up to the Nyquist Band (8 GHz) with Spurious Free Dynamic Range (SFDR) of at least 70 dBFS. We validate the method with a schematic 28 nm FDSOI CMOS transistor level testbench, Montecarlo simulations and temperature variations from 27 °C to 125 °C.

Index Terms—CMOS, 28 nm FDSOI, Current Source, Current Steering, Foreground Calibration, Body Biasing, Digital to Analog Converter, Amplitude Calibration

I. INTRODUCTION

With the expansion of global data traffic, new telecommunication standards are aiming to increase the data transmission rates, alongside with other key important factors such as latency, reliability and power consumption. Data converters are fundamental parts of modern telecommunication systems, they need to have high resolution, and high sampling rate to be able to generate and process complex wideband modulated signals. The transistor maximum operating frequency is highly dependent of its Width (W) and Length (L) ratio, as well as its area, which is directly linked to its parasitic capacitances. However, small area of transistor leads to higher mismatch between two transistors. In the case of a time interleaved current steering DAC, the matching between each subDACs is critical to meet linearity specifications. For high resolution DACs (≥ 12 bits) mismatch between elementary current sources can be a limiting factor of performance. All these facts highlight the need for calibration when designing high speed and high resolution DACs.

There are a lot of different techniques to compensate both static and dynamic errors in DACs, however this work focus

specifically on the calibration of static errors, which consist of amplitude and gain error in the DAC output. To characterize the validity of the calibration, we observe the following metrics : Derivative Non Linearity (DNL), Integral Non Linearity (INL), and Spurious Free Dynamic Range (SFDR).

Digital processing is an alternative method to calibration, for example, in 1976 [1] introduce the Dynamic Element Matching (DEM) method, which rely on digital signal processing to randomize DAC cell mismatch errors. In modern designs, DEM is achieved by swapping connections between thermometer code and unary cell, according to a predetermined control sequence. One advantage of the DEM is that it averages timing related errors. The downside of DEM is that it requires additional circuitry to shuffle the data at the sampling clock rate, leading to increased power consumption in high performance DAC design [2].

Digital predistortion modify the original input data to compensate a system distortion by applying an inverse correction algorithm to the digital code. More recently, a pulsed DPD technique uses sub-DACs to superpose sub-ps pulses to the data driving signal, managing to correct both amplitude and timing errors [3]. The timing constraint on the sub-DAC can be mitigated by generating wider pulse, at the expense of more amplitude precision.

Amplitude calibration reduces the output mismatch errors by compensating them with an auxiliary circuit. [4] shows that amplitude calibration significantly reduces the current source area in comparison to the intrinsic accuracy size required to match fixed DNL/INL and SFDR specifications. Fig. 1 shows an example of an amplitude calibration implementation. The weighted current cell output current is combined with the output of an auxiliary DAC. During the calibration phase, the digital input value of the auxiliary DACs are set to compensate the weighted current cells mismatch errors. Note that the precision of the auxiliary DAC and its dynamic range will determine the precision and range of the correction. This method still introduce more circuitry in the DAC current cell matrix, and, for the design of low power and high resolution DAC, creating the auxiliary current source for the Least

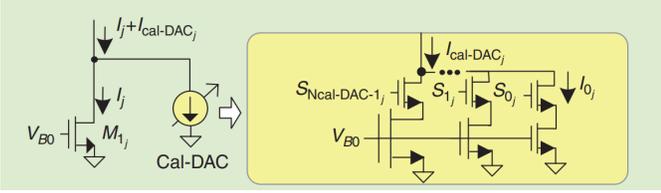


Fig. 1: Amplitude calibration using an auxiliary DAC for each cell [2]

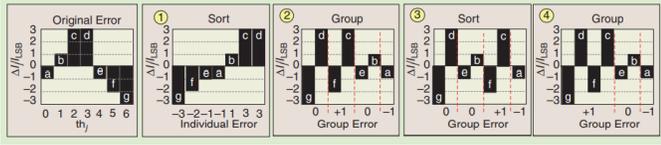


Fig. 2: Sort and group method applied to 7-unary cell errors [2].

Significant Bit (LSB) can be difficult especially if the LSB current is very small.

Mapping techniques rely on a reordering of the unary cell to create the DAC binary current cells. It requires a measurement of the unary cell errors, but it does not introduce dynamic swapping of interconnection as in the case of DEM. The mapping can be used to minimize amplitude errors, but it can also be used to optimize timing related errors. In Fig. 2 the *Sort-and-group* method is applied to 7 unary cell errors, and shows the steps to define the new switching sequence : at first the errors are sorted in increasing order, secondly, the largest negative and positive errors are grouped together repeatedly in order to minimize the summed group error. Thirdly, the groups of two unary cell are again sorted in the same manner as the first step. Lastly, the binary grouping is performed on the summed error of the second step.

In section II, we present an analytical model for mismatch applied to the 28 nm FDSOI technology and we detail how the body biasing effect can be used for calibration purposes. In section III we present the calibration algorithm and its implementation, In section IV, we describe the validation testbench, using a 16 GHz $2 \times$ time-interleaved DAC, with very small size current sources, and our calibration circuit. Section IV shows montecarlo simulation results, temperature robustness, and section V summarize the performance of our work.

II. 28 NM FDSOI TRANSISTOR TECHNOLOGY IMPLEMENTATION

A. Current sources Process Mismatch

The experimental data show that threshold voltage differences (ΔV_T) and current factor differences $\Delta\beta$, with $\beta = \mu C_{ox} \frac{W}{L}$, are the dominant sources underlying the drain-source current or gate-source voltage mismatch for a matched pair of MOS transistors [5]. Fig. 3 presents the mathematical description of these mismatch when considering a pair of NMOS transistors acting as current sources. The two constant

parameters ΔV_T and A_β are technology dependant, it is worth noting that for 28nm FDSOI technology, and LVT flavor transistors, $\Delta V_T = 1.2mV.um$ and $A_\beta = 2.8\%.um$. The standard deviation of the current mismatch ($\sigma(\Delta I/I)$) can be expressed as the quadratic sum of the two contributors, with g_m the transconductance gain, and I_d the drain current, as following:

$$\sigma(\Delta I/I) = \sqrt{\left(\frac{g_m}{I_d}\right) \times \Delta V_T \frac{A_\beta}{\sqrt{W * L}}\right)^2 + \left(\frac{A_\beta}{\sqrt{W * L}}\right)^2} \quad (1)$$

From 1, it can be seen that device mismatch is inversely proportional to the area of the current source, and proportional to the g_m value. When designing DACs, However, the total area of the current steering matrix scales with the resolution and the unitary element area. The use of segmentation can reduce the area ratio between the LSB and the MSB [6], but require a more complex organisation of the data latches. Ultimately, parasitic capacitances limit the operating speed, and they increase with the DAC area. These tradeoffs highlight the challenge associated with the design of high speed and high resolution DACs.

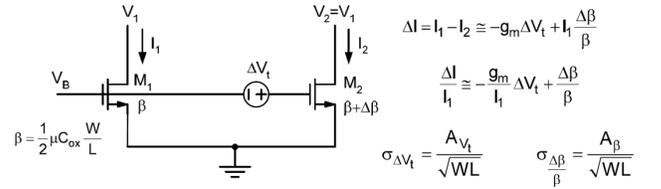


Fig. 3: Relative current mismatch expressed in function ΔV_T and $\Delta\beta$ [6]

B. Backgate Body Bias in FDSOI

The transistor implementation relies on the 28 nm FDSOI Body bias effect to compensate mismatch introduced by fabrication process. Fig. 4 presents a cross cut view of a 28 nm FDSOI transistors. Low Voltage Threshold (LVT) type of transistor are used for the current sources, as they have an increased maximum operating frequency in comparison to other flavor (Regular V_T or High V_T). Since the LVT requires a flip well, raising the body bias voltage will actually reduces its V_T . As shown in Fig. 5, the V_T variation is linearly dependent to the body bias voltage with a coefficient of $-80mV/V$. It is worth noting that the V_T variation is not affected by temperature, which impact can be interpreted as a threshold voltage offset, inversely proportional to the temperature value. These results reach the same conclusions developed in [7].

The main advantage of body bias voltage control in current steering DAC calibration techniques is that it only requires to bring one biasing voltage per weighed current cell, while the rest of the calibration circuit do not require to be close to the core current matrix. This approach limits the introduction of unwanted parasitic elements and therefore is suited for high

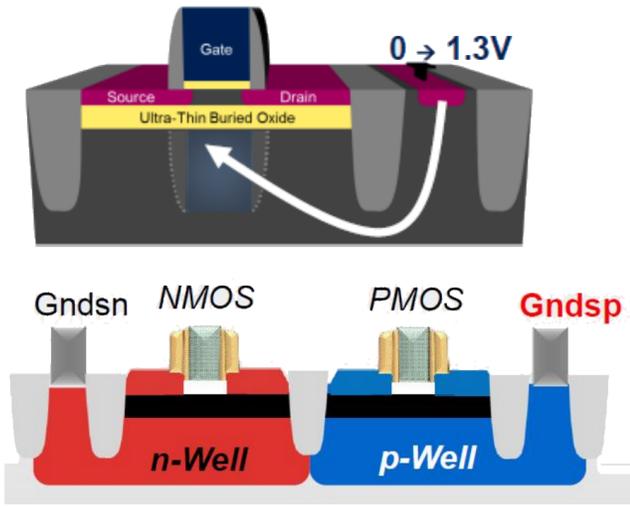


Fig. 4: Top : cross-cut view of a FDSOI transistor. Bottom : LVT flip-well transistors

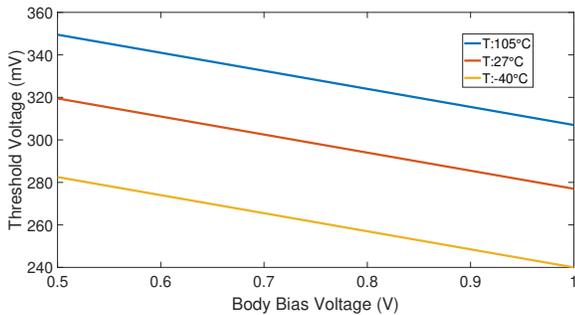


Fig. 5: Variation of the threshold voltage in function of the backgate body bias voltage.

speed optimization. The correction range and precision of this approach is directly linked to the system generating the body bias control voltage and to the intrinsic input voltage range limitation of the transistors.

III. DETECTION AND CALIBRATION ALGORITHM

A. Algorithm

This work is based on the amplitude calibration principle and the algorithm is inspired by [8]. In our case, the output current of the binary weighted cells is tuned through backgate body bias control. We illustrate the algorithm by applying it to a 3 bits DAC (see Fig. 6a). The unit current steering cell is composed of a current source (M1), and two current steering transistors (M2 and M3). This unit cell generate our LSB current. The LSB+1 current is generated by grouping 2 of these unit cells and the LSB+2 is obtained by grouping 4 of these unit cells. All the current cells can be activated or not, through the switches S0, S1, S2 and S3. The calibration current source generates a current equal to the LSB current, however, as it is only active during the calibration process, speed constraint are relaxed, so the reference current can

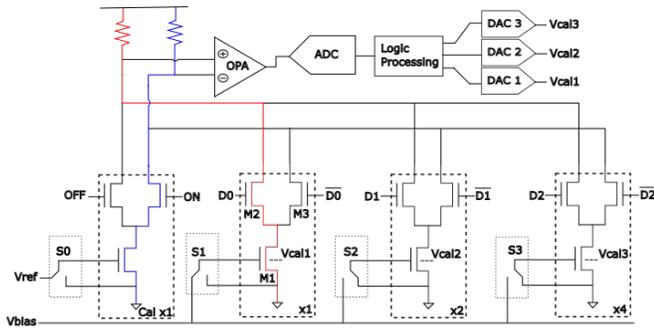
be designed to achieve a greater accuracy. The comparison between the calibrated cell and the reference current is made by an operational amplifier (OPA). After the quantization of the cell current error, the logic processing block will adjust the corresponding DAC input code to modify the body bias voltage of the calibrated cell, and effectively tune its output current, completing the negative feedback loop. An interesting feature of this calibration is that since we calibrate the weighed cells one by one, we need only one code per weighed cell to fully calibrate the static errors of the DAC. This lead to a very simple state machine to generate the calibration data input for the main DAC, and activate the specific current cells needed. Fig. 6 shows the different phase of the calibration algorithm applied on the 3 bits binary DAC. First we set all the current cells OFF, except the LSB and the reference. We calibrate the LSB cell (see Fig. 6a by comparing it with the reference. Then we activate the LSB+1 cell and calibrate it by comparing it against the LSB + the reference (see Fig. 6b). In the final calibration step, we activate the LSB+2 cell and we compare its output current to the reference plus the LSB plus the LSB+1 currents. In this work the state machine implementation is achieved through a walking bit, and the required calibration driving signals are generated using pass transistor logic.

B. Time interleaved DAC

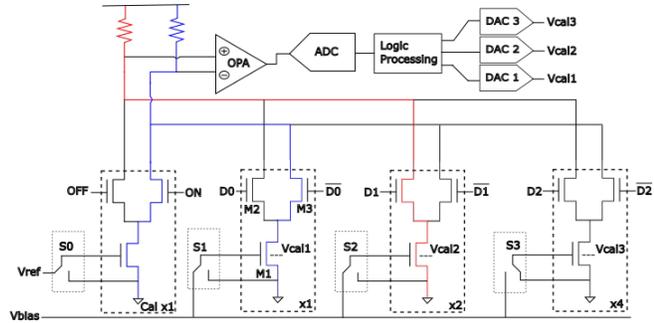
In order to validate our calibration method and since the current mismatches are directly linked to the area of the unit cells, we use a full transistor level implementation of a 2 x time interleaved current steering DAC with of the current source matrix, cascodes, steering transistors, and analog Multiplexer (MUX). Its effective sample rate is 16 GHz and it has a 12 bits resolution, implemented with a segmentation order of 4, resulting in 8 binary weighted bits and 15 MSB thermometric bits. The two subDACs are operating in phase opposition with a sample rate of 8 GHz, and their current output is routed by the analog MUX successively to the main and to the dummy loads. Fig. 7 shows the implementation of a unit current cell, we choose a cascode implementation to limit the capacitive coupling between the current source gate biasing voltage and the switching activity produced by both code related digital input, and the analog MUX. The transistor sizing is summarized in Table I, We set the unit current source area to a small value of $W = L = 350nm$ for a LSB current of $2 \mu A$. The relative current mismatch per current source is estimated to $\sigma I/I = 15\%$. As the calibration circuit will compensate these mismatch, the total area of the current steering matrix is under $50 * 50 \mu m^2$ for 12 bits of resolution and potentially very high speed operation.

C. Current source mismatch compensation through body bias

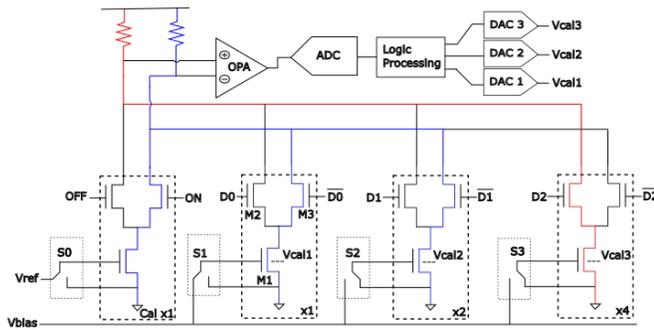
By varying the body bias voltage of the DAC MSB current cell (256 unit cells, with a current of $2 \mu A$) from $\frac{V_{DD}}{2} + / - 250mV$ the range of correction is $+/- 80$ LSBs, at $27^\circ C$. We verified by simulation that the relative current modification due to body bias is constant for a given sizing of current sources. Therefore for an elementary current source



(a) The LSB current is compared with the calibration current



(b) The LSB+1 current is compared with the LSB plus the calibration current



(c) The LSB+2 current is compared with the LSB, the LSB+1 and the calibration current

Fig. 6: Illustration of the calibration algorithm on a 3 bits DAC

with $W = L = 350nm$, A variation of ± 250 mV in the body bias voltage can compensate relative current mismatch up to $\pm 30\%$, which is twice more than the estimated $\sigma I/I$ in function of the current source sizing.

IV. VALIDATION TESTBENCH

A. Overview

To validate the functionality of the presented algorithm, we implement a simplified version using ideal elements, and we connect it at the output of the time interleaved DAC (see Fig. 8). The two subDACs are calibrated one after the other. During the calibration phase the error between the reference current and the cell to correct is sensed by an Operational

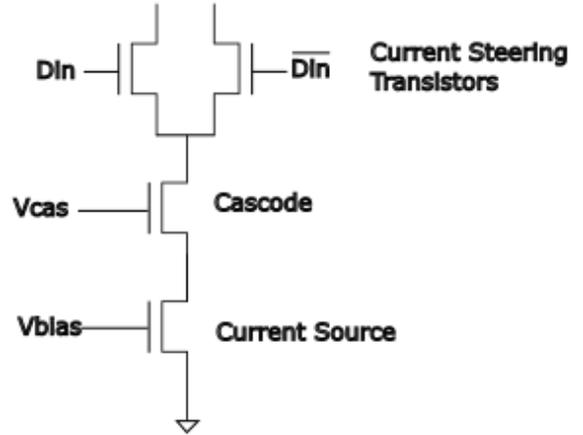


Fig. 7: Transistor level implementation of the unit current steering cell

		W	L	M
Analog Multiplexer (8 LVT N_FET)		1 μ m	30 nm	40
Reference I = 256 μ A	Cascode	120 nm	30 nm	128
	Current source	350 nm	350 nm	128
Bit 1 (LSB) I = 2 μ A	Current steering	320 nm	30 nm	1
	Cascode	120 nm	30 nm	1
Bit 2 I = 4 μ A	Current steering	320 nm	30 nm	1
	Cascode	120 nm	30 nm	2
Bit 3 I = 8 μ A	Current steering	320 nm	30 nm	1
	Cascode	120 nm	30 nm	4
Bit 4 I = 16 μ A	Current steering	320 nm	30 nm	1
	Cascode	120 nm	30 nm	8
Bit 5 I = 32 μ A	Current steering	320 nm	30 nm	1
	Cascode	120 nm	30 nm	16
Bit 6 I = 64 μ A	Current steering	640 nm	30 nm	1
	Cascode	120 nm	30 nm	32
Bit 7 I = 128 μ A	Current steering	1,28 μ m	30 nm	1
	Cascode	120 nm	30 nm	64
Bit 8 I = 256 μ A	Current steering	1,28 μ m	30 nm	2
	Cascode	120 nm	30 nm	128
MSB (x15) I = 512 μ A	Current steering	1,28 μ m	30 nm	4
	Cascode	120 nm	30 nm	256
	Current source	350 nm	350 nm	256

TABLE I: Transistor circuit sizing

Transconductance Amplifier (OTA). The output of the OTA is connected to one of the capacitors through one path of the switch array. Each capacitor is directly connected to the backgate body bias voltage of a weighed current cell. The control unit go through a finite state machine to decide the state of every switches in the circuit at each calibration steps. Because we are using ideal switches and ideal capacitors that have no leakage, the voltage stored on the capacitor will stay constant overtime. In reality, it is necessary to have a method to refresh the body bias voltage value. This can be achieved using DC DACs as presented in Fig. 6. The testbench simulation start by generating a one tone 100 MHz test to measure the performance before calibration. After this it starts calibrating the 23 current cells of DAC A, then it changes the path of the analog MUX to calibrate DAC B in the same way. INL and DNL are measured through simulation at the end of the calibration phase. After, we run again a 100 MHz one tone test, allowing us to measure the calibration improvement in SFDR and SNR.

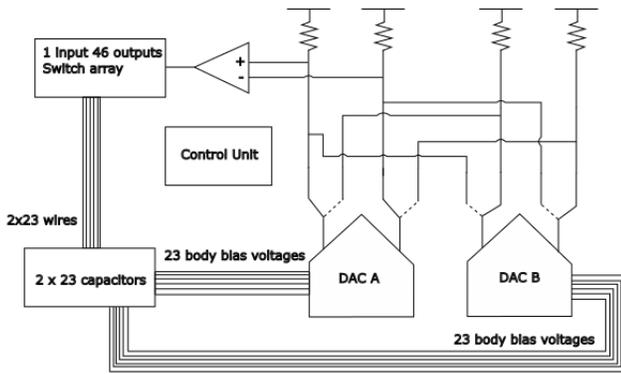


Fig. 8: Testbench validation: the calibration circuit with ideal elements is connected to the time interleaved DAC outputs

B. Temperature variation

In the first place we test the temperature robustness of the calibration from 27 °C to 125 °C, with a set of manually selected mismatch on the current sources represented in Fig.9. We choose to place more errors in the early LSB section, as statistically the MSB section is going to be less impacted due to their larger area. From the result plotted in Fig. 10 the calibration method is robust to a wide range of temperature, providing an amelioration of 15 dB on the SNR and SFDR at 125 °C. We can also observe that the calibration performance decrease with an increase in temperature. An explication to this phenomenon is that an increase in temperature reduces the intrinsic threshold voltage of a transistor, and therefore reduces the range of current compensation through the body bias voltage.

C. Montecarlo simulations

The Montecarlo simulation is set with a maximum standard deviation of 4σ and include local and global mismatch, We

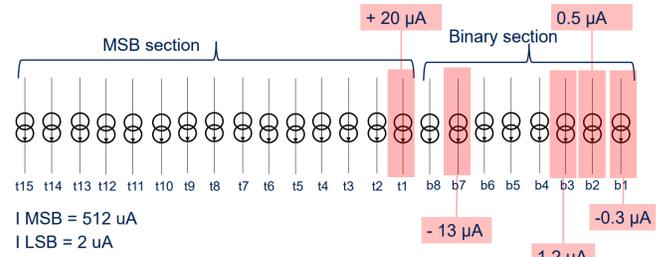


Fig. 9: Set of mismatch injected manually in the current sources

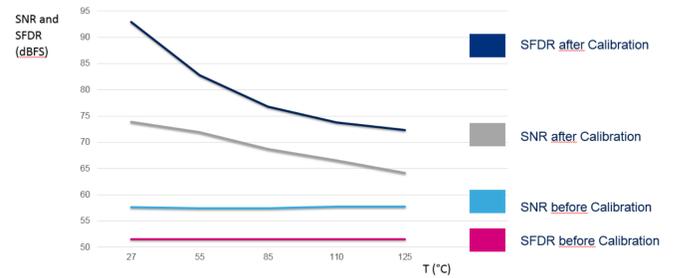


Figure 42: SFDR and SNR after calibration in function of temperature

Fig. 10: Impact of the calibration on SNR and SFDR through a temperature range of 27 - 125 °C

run a total of 500 runs and selected the case with the worst INL. Fig 11 plot the INL of the two subDAC, before and after the calibration. In this case we started from an INL value of +17 LSB, and after calibration dropping to 0.03 LSB. This value is very low because the analog feedback calibration loop is not limited by the digital resolution and therefore can converge very precisely. This calibration performance is also impacted by the current steering transistors mismatch, as only one path is calibrated with the algorithm. Fig. 12 shows the the output of the time interleaved DAC in the frequency domain, the fourier transform is calculated with one point per sample in order to characterize only the impact of static mismatch. Before calibration calibration we can spot INL and DNL related spurs, located at the higher order harmonics of the 100 MHz generated tone. We can also notice a gain error between the two subDACs, generating at half the sampling frequency (8 GHz) minus the input signal frequency. The time interleaving error mechanism and frequency signature spurs are well documented in [9]. We observe that our calibration technique removes the INL and DNL related spurs,as well as the spurs near Nyquist frequency, meaning that both the subDAC are well calibrated, but also well matched together. The calibration circuit ameliorates the SFDR from 70 dB to 87 dB, which is a very good improvement.

V. CONCLUSION

In conclusion we presented a novel method for current steering DAC amplitude calibration using body bias voltage control

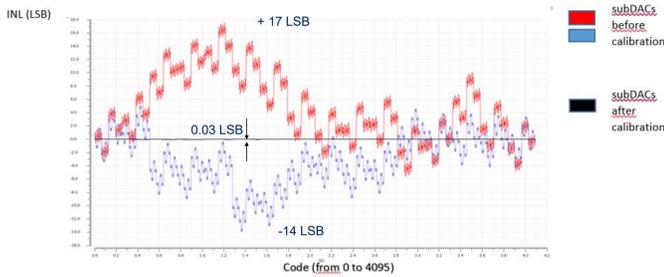


Fig. 11: INL of the two subDAC from a montecarlo run, before and after calibration

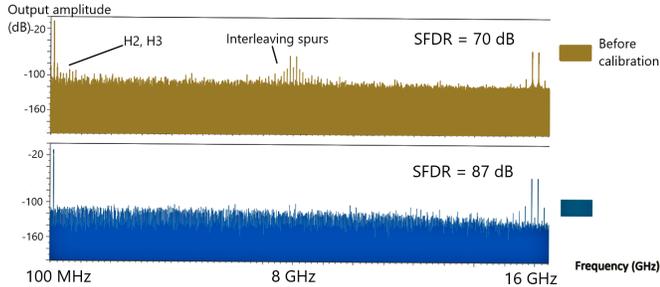


Fig. 12: Frequency domain spectrum of the 100 MHz tone output before and after calibration

to effectively compensate current due to fabrication process mismatch. We proved the validity of the algorithm using an implementation of the algorithm with ideal electrical elements, and calibrating a transistor level implemented 12 bits, 16 GS/s 2 x time interleaved DAC. The calibration circuit shows satisfying results from montecarlo runs, maintaining the output SFDR above 70 dB, and compensating INL up to 0.03 LSB. This technique requires a transistor technology with backgate biasing possibilities. However, most of the existing calibration techniques introduces extra parasitic element near the core current matrix of the DAC. Classic amplitude calibration requires per-cells auxiliary DACs with sufficient resolution to compensate the mismatch. Mapping techniques also require to plan interconnection between the current sources to be able to sort and map them. These interconnexions have to be near the core current matrix and therefore will also be a source of parasitic capacitance. Using the body bias control voltage allows for a significant area reduction, both from the DAC current source matrix, which matching constraints have been relaxed by the calibration, but also by the absence of extra elements near the core current matrix, beside one metal connexion per cell. Being able to design very small area DACs is a critical step in the design of very high speed wideband DACs.

VI. AKNOWLEDGEMENTS

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