



**HAL**  
open science

## Feature selection techniques for indirect test and statistical calibration of mm-wave integrated circuits

Manuel Barragan, Gildas Leger, Florent Cilici, Estelle Lauga-Larroze, Salvador Mir, Sylvain Bourdel

### ► To cite this version:

Manuel Barragan, Gildas Leger, Florent Cilici, Estelle Lauga-Larroze, Salvador Mir, et al.. Feature selection techniques for indirect test and statistical calibration of mm-wave integrated circuits. 27th European Test Symposium (ETS 2022), May 2022, Barcelona, Spain. hal-03759492

**HAL Id: hal-03759492**

**<https://hal.science/hal-03759492>**

Submitted on 24 Aug 2022

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



Distributed under a Creative Commons Attribution - NonCommercial 4.0 International License

# Feature selection techniques for indirect test and statistical calibration of mm-wave integrated circuits

Manuel J. Barragan<sup>1</sup>, Gildas Leger<sup>2</sup>, Florent Cilici<sup>3</sup>, Estelle Lauga-Larroze<sup>1</sup>, Salvador Mir<sup>1</sup>, Sylvain Bourdel<sup>1</sup>

<sup>1</sup> Univ. Grenoble Alpes, CNRS, Grenoble INP, TIMA, 38000 Grenoble, France

<sup>2</sup> IMSE-CNM, CSIC, Universidad de Sevilla, Av. Americo Vespucio, 41092 Sevilla, Spain

<sup>3</sup>NXP, Toulouse, France

## I. INTRODUCTION

Nowadays, the constant evolution of CMOS technologies towards smaller design nodes and higher transitions frequencies, together with the development of optimized back-end-of-line (BEOL) options, make possible the co-integration of complex RF and mm-wave circuits in a single silicon substrate. However, these advanced integration nodes are prone to large process variations and manufacturing defects that may result in a significant –sometimes catastrophic– performance degradation and low fabrication yield. Extensive production test and calibration procedures are required to guarantee the performance of integrated RF and mm-wave circuitry, which, due to the complex nature of at-speed functional test, results in expensive and long test and calibration cycles that may stall the production line.

Leveraging the power of machine learning techniques has been proposed as a promising solution to alleviate these issues. These techniques are aimed at replacing the direct measurement of complex functional specifications by simpler observables, usually called signatures, that are strongly correlated to the target specifications. Machine learning regression algorithms are then employed to map the signatures to the target specifications. Since signatures are designed to be simpler and cheaper to extract –in many cases even using some sort of simple on-chip test instruments– the overall test complexity and cost are greatly reduced. This is the basis of the so-called alternate test [1]-[2], where supervised machine learning models are used to replace the classical functional test. Supervised machine learning models are applied in two phases: a training phase, where the model is inferred from a set of training data containing both the input signatures and the target specifications; and a testing phase, where only the signatures are measured and the target performance is predicted using the previously inferred machine learning regressor.

Indirect test based on machine learning regression is an elegant solution to simplify the complexity of analog functional testing while still addressing the issue of characterizing the circuit performance and comparing it against classical performance acceptance windows. Moreover, this technique can be easily extended to performance calibration applications. Indeed, provided that the circuit has some tuning knobs, the machine learning regressor can be trained to predict the optimum positions of the tuning knob, rather than the nominal performance [3]-[5].

However, machine learning-based test and calibration are not free of shortcomings and potential pitfalls that should be addressed for a successful implementation. In this special session we will focus on one of the main issues for the adoption of these techniques: the choice of a meaningful set of input signatures. It is clear that finding appropriate signatures that are strongly correlated to the target

performances is a key point of this test strategy. Actually, early works on this topic explored an automated signature generation technique based on optimizing a piecewise-linear test stimulus to recover meaningful output signatures [6]. While this is a sound strategy, the nature of the test stimulus is fixed which may limit the information that can be recovered from the output signatures. In this special session we will explore a more general solution to the definition of appropriate signature sets based on advanced feature selection algorithms. Firstly, we will introduce the concept of feature selection, describing the potential advantages and disadvantages of different techniques. Then we will present some case studies to illustrate the application of feature selection techniques to different scenarios in the context of mm-wave ICs.

## II. FEATURE SELECTION TECHNIQUES

Given a set of input features and a set of target specifications, the goal of a feature selection algorithm is to find the minimum subset of input features that can be used to regress the target specifications within a predefined prediction error. In practice, signature sets are either proposed *ad hoc* based on expert design knowledge or generated by following an *ad hoc* procedure such as [6]. As a result, the initial signature set is usually suboptimal: it may contain redundant information, noise, or even information that is uncorrelated to the target specifications. A variety of feature selection techniques have been proposed in the literature for cleaning up the input signature space in indirect test applications [7]-[14]. Generally speaking, we can classify these proposals in three main feature selection families: a) Wrappers, b) Filters, and c) Hybrid feature selection.

### A. Feature selection using wrappers

The wrapper approach to feature selection considers the selection as an optimization problem. Wrapper feature selection algorithms employ the machine learning regressor as a black box within an optimization loop. An optimizer is used to explore the input feature space and find the optimum set that minimizes the prediction error. The main advantage of the wrapper approach is the direct estimation of the prediction error, while the main disadvantage is the computational cost, as training and evaluation have to be repeated in each step of the optimization loop. For large data sets, a full search in the input feature space becomes impossible, and smart search strategies must be used [7].

### B. Feature selection using filters

Filters are aimed at selecting or removing signatures from the initial feature set based on a statistical observation, without the need of training a machine learning model. In general, we can distinguish two families of filters: unsupervised and supervised filters.

Supervised filters rank the candidate features in the input feature space according to their correlation to the target performance. Complex multidimensional and/or nonlinear

correlation metrics that go beyond Pearson’s classic correlation have been explored in recent literature, including Kendall’s tau [11], Brownian distance correlation [10], minimal-redundancy-maximal-relevance criterion [8], etc. Unsupervised filters, on the other hand, do not consider the information in the target space. Instead, they analyze the information structure in the feature space. The most common example of unsupervised filter is the Principal Component Analysis (PCA), that tries to identify the directions in the feature space that best explain the variation observed in the data, supposing that the underlying structure in the data is linear [12]. The main advantage of filtering techniques is the low computational cost. However, they do not offer any estimations of the prediction error that can be expected in the regression.

### C. Hybrid feature selection techniques

Hybrid techniques were proposed in [8] as a way of combining the advantages of wrappers and filters. The main idea is to use a correlation metric, such as the Brownian distance correlation, to guide the selection of new features in a classical wrapper loop. In this scheme, a feature is selected if it can explain the prediction error in the previous iteration of the wrapper loop. This way, only one training stage is required per iteration and the selection is naturally biased to add features that are meaningful for improving the predictions.

## III. CASE STUDIES

### A. Nonintrusive indirect test of mm-wave circuits [15]

Our first case study is aimed at the systematic design of an indirect test program for a mm-wave DUT based on nonintrusive process monitors. Nonintrusive process monitors are stand-alone circuits that are integrated in the close proximity of the DUT, but that are not electrically connected to it. These monitors provide a low-frequency or DC signature that is strongly correlated to the variation of a given process parameter. It should be clear that by carefully choosing relevant process monitors, we could be able to train a machine learning regressor that would be able to predict the performance of the DUT by measuring only the signatures provided by the process monitors. Early works on nonintrusive test proposed process monitor circuits that mimic DUT circuit structures [16]-[18], however this may result in suboptimum performance prediction as only first-order performance degradation mechanisms may be covered based just on a visual inspection of the design architecture [18].

Feature selection techniques can be used to systematize the design of process monitors, as demonstrated in [7], [15]. In this regard, we can use a feature selection algorithm to explore, in a simulation environment, the space of process parameters defined in the Monte Carlo and corner models in the PDK of the technology, in order to find the parameters that are actually relevant for the DUT performance. Once identified, we can target the design of process monitors that provide signatures of these parameters. The interested reader is referred to [15] for a detailed description of the proposed feature search technique.

The proposed technique has been successfully applied to a 65 GHz PA case study fabricated in STMicroelectronics 55nm CMOS technology. A feature selection algorithm based on a hybrid selection technique was employed to explore the space of process parameters of the technology, containing more than 500 independent parameters. Hybrid selection allowed the

identification of only 11 relevant parameters, which guided the design of appropriate process monitors. The feasibility of the resulting indirect test was validated in a set of 21 fabricated samples. Table I shows the relative RMS prediction error obtained in the prediction of the main PA specifications from the nonintrusive signatures. As it can be seen, a significant precision is achieved for all the considered specifications.

TABLE I. RELATIVE RMS PREDICTION ERROR

Specification	Relative RMS prediction error (%)
$S_{21}@65\text{GHz}$	1.4
$S_{11}@65\text{GHz}$	1.6
$S_{22}@65\text{GHz}$	2.0
$P_{sat}$	0.7
$CP_{1\text{dB}}$	1.3
$PAE$	2.0
$IDC$	0.65

### B. One-shot statistical calibration of mm-wave circuits using nonintrusive performance monitoring [19]

Our second case study is aimed at designing a one-shot calibration strategy for yield enhancement of a mm-wave DUT, based again on nonintrusive process monitors. Since process monitors track process variations, assuming that appropriate tuning knobs are included in the DUT, it would be possible to correlate the output of the monitors to the optimum calibration code, i.e., the positions of the tuning knobs that minimizes performance degradation due to process variation. This strategy has the advantage of avoiding costly and lengthy test-and-tune calibration loops.

Again, feature selection algorithms are a key element for defining this calibration strategy. Feature selection can be used to explore the multidimensional space of process parameters in search of the relevant process parameters for predicting the calibration code, while at the same time can guide the design of appropriate tuning knobs by unveiling the main root causes of performance variation in the DUT. The interested reader is referred to [19] for a detailed description.

The proposed technique has been applied to a 69 GHz PA case study fabricated in STMicroelectronics 55nm CMOS technology. The feasibility and performance of the proposed calibration is demonstrated on a set of 39 fabricated samples. Table II shows the yield before and after calibration for each of the considered PA specifications. It is clear to see a dramatic yield improvement due to the proposed one-shot calibration solution.

TABLE II. YIELD ENHANCEMENT

Specification	Yield before calibration (%)	Yield after calibration (%)
$S_{21}@69\text{GHz}$	51	100
$S_{11}@69\text{GHz}$	90	100
$S_{12}@69\text{GHz}$	100	100
$P_{sat}$	74	95
$CP_{1\text{dB}}$	77	100
$PAE$	31	100
$IDC$	72	97
Overall yield	5	92

## REFERENCES

- [1] P. N. Variyam and A. Chatterjee, "Enhancing test effectiveness for analog circuits using synthesized measurements," in *VLSI Test Symposium*, 1998, pp. 132–137.
- [2] G. Leger and M. J. Barragan, "Mixed-signal test automation: Are we there yet?," 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 2018, pp. 1–5.
- [3] N. Kupp, H. Huang, Y. Makris, and P. Drineas, "Improving Analog and RF Device Yield through Performance Calibration," *IEEE Design & Test of Computers*, vol. 28, no. 3, pp. 64–75, May 2011.
- [4] M. Andraud, H. Stratigopoulos, and E. Simeu, "One-Shot Non-Intrusive Calibration Against Process Variations for Analog/RF Circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 11, pp. 2022–2035, Nov 2016.
- [5] A. Zjajo, M. J. Barragan, and J. P. d. Gyvez, "Low-Power Die-Level Process Variation and Temperature Monitors for Yield Analysis and Optimization in Deep-Submicron CMOS," *IEEE Trans. on Inst. and Meas.*, vol. 61, no. 8, pp. 2212–2221, Aug. 2012.
- [6] P.N.Variyametal., "Prediction of analog performance parameters using fast transient testing," *Trans. on Computer-Aided Design of Int. Circ. and Syst.*, vol. 21, no. 3, pp. 349–361, 2002.
- [7] M. Barragan and G. Leger, "A Procedure for Alternate Test Feature Design and Selection," *IEEE Design & Test*, vol. 32, no. 1, pp. 18–25, Feb. 2015.
- [8] G. Leger and M. J. Barragan, "Brownian distance correlation-directed search: A fast feature selection technique for alternate test," *Integration, the VLSI Journal*, vol. 55, pp. 401–414, Sep. 2016.
- [9] H.-G. Stratigopoulos *et al.*, "RF Specification Test Compaction Using Learning Machines," *Trans. on VLSI Systems*, 2009.
- [10] M. J. Barragan and G. Leger, "Efficient selection of signatures for analog/RF alternate test," in *European Test Symposium*, 2013.
- [11] A. Gomez-Pau, L. Balado, and J. Figueras, "Efficient Production Binning Using Octree Tessellation in the Alternate Measurements Space," *Trans. on Computer-Aided Design of Int. Circ. and Syst.*, vol. 35, no. 8, pp. 1386–1395, 2016.
- [12] H. Ayari *et al.*, "Smart selection of indirect parameters for DC-based alternate RF IC testing," in *VLSI Test Symposium*, 2012, pp. 19–24.
- [13] S. Larguech *et al.*, "Efficiency evaluation of analog/RF alternate test: Comparative study of indirect measurement selection strategies," *Microelectronics Journal*, vol. 46, no. 11, pp. 1091–1102, Nov. 2015.
- [14] M. J. Barragan, G. Leger, F. Cilici, E. Lauga-Larroze, S. Bourdel and S. Mir, "On the use of causal feature selection in the context of machine-learning indirect test," 2019 Design, Automation & Test in Europe Conference & Exhibition (DATE), Florence, Italy, 2019, pp. 276–279.
- [15] F. Cilici *et al.*, "A Nonintrusive Machine Learning-Based Test Methodology for Millimeter-Wave Integrated Circuits," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 8, pp. 3565–3579, Aug. 2020.
- [16] A. Zjajo, M. J. Barragan and J. P. de Gyvez, "BIST Method for Die-Level Process Parameter Variation Monitoring in Analog/Mixed-Signal Integrated Circuits," 2007 Design, Automation & Test in Europe Conference & Exhibition, Nice, France, 2007, pp. 1–6.
- [17] L. Abdallah, H. Stratigopoulos and S. Mir, "True non-intrusive sensors for RF built-in test," 2013 IEEE International Test Conference (ITC), Anaheim, CA, USA, 2013, pp. 1–10.
- [18] A. Dimakos, H. -G. Stratigopoulos, A. Siligaris, S. Mir and E. De Foucauld, "Built-in test of millimeter-Wave circuits based on non-intrusive sensors," 2016 Design, Automation & Test in Europe Conference & Exhibition (DATE), Dresden, Germany, 2016, pp. 505–510.
- [19] F. Cilici, M. J. Barragan, S. Mir, E. Lauga-Larroze, S. Bourdel and G. Leger, "Yield Recovery of mm-Wave Power Amplifiers using Variable Decoupling Cells and One-Shot Statistical Calibration," 2019 IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, 2019, pp. 1–5.