Integration of power flow controllers in HVDC grids

Florent Morel, Joan Sau-Bassols, Selle Toure, Serge Poullain, Frank Jacquier

Paper ID: 896 Session 2022
Study Committee B4
Preferential Subject: HVDC Systems and their applications

Integration of power flow controllers in HVDC grids

Florent MOREL*[1], Joan SAU BASSOLS[1], Sellé TOURE, Serge POULLAIN[1], Frank JACQUIER[1]
Supergrid Institute[1]
France
florent.morel@supergrid-institute.com, joan.saubassols@supergrid-institute.com,
selle.toure@gmail.com, serge.poullain@supergrid-institute.com,
frank.jacquier@supergrid-institute.com

SUMMARY

High voltage direct current (HVDC) grids are seen as a key technology to integrate renewable power sources across long distances. They provide flexibility and redundancy to the system, but they also bring many challenges. Among them, the power flow control becomes a concern since the converter stations at each terminal can control the current at node level but not the currents circulating inside the mesh. The current distribution through the different DC conductors depends on the resistance relation between conductors. The installation of new converter stations, modifications of the grid configuration, N-1 contingencies, etc. can modify the current distribution leading to overloads in some conductors, while others are underused. Consequently, power curtailments or the installation of new conductors may be necessary. An alternative solution is to install medium voltage converters inserting voltages in series with the DC conductors, known as power flow controllers (PFC) or current flow controllers (CFC). Those devices allow to control the current distribution in the HVDC grid and they can be understood as the equivalent of flexible AC transmission systems (FACTS) for HVDC grids. In the literature, several converter topologies are suggested, which are validated via simulations or experimental testing of scaled-down prototypes. However, less attention is being put on how to integrate such a device into the HVDC grid: the type of busbar arrangement, the type of required switches, such as disconnectors, bypass switches, DC breakers, etc. Additionally, the busbar arrangement must allow the insertion, bypass and grounding of the PFC converter without interrupting the HVDC grid power transmission and ensuring minimal disturbances.
This work discusses different DC busbar arrangements with PFC and selects a circuit providing good availability, moderate cost and allowing insertion, bypass and grounding of the PFC. Then, the sequence of switches to insert, bypass and ground the PFC is presented and validated using simulations. The simulation results show that the proposed circuit and sequences allow to smoothly insert, bypass and ground the PFC while the HVDC grid is in operation. The device does not cause any major disturbance to the HVDC grid and can smoothly control the current distribution between the different conductors. Finally, the requirements of the external switches of the PFC are also assessed by means of the simulations, identifying the opening voltage, current and time. This work outlines that the bypass switches of the PFC have requirements in between busbar transfer switches and line transfer switches, but much lower than DC breakers and also lower than other already implemented switches, such as the metallic return transfer breaker (MRTB). The other switches of the PFC busbar arrangement are expected to be in the range of DC disconnectors (excluding the necessary DC breakers according to the protection strategy of the HVDC grid). Thus, the realization of the busbar arrangement becomes technically feasible.

KEYWORDS

Power Flow Controller – Current Flow Controller – High Voltage - Direct Current – Integration – Busbar – Bypass Switches – Multi-terminal – Mesh - DC Grid.

1. INTRODUCTION

High voltage direct current (HVDC) grids can facilitate the integration of distant renewable power sources. They can increase the flexibility and redundancy of the electrical system, but they also bring challenges regarding their operation and control [1]. Since the founding works on HVDC grid feasibility, presented in Cigré technical brochure 533, much progress has been done. The first multi-terminal HVDC systems are in operation in China and other such systems are likely to be developed in Europe, probably in the North Sea to integrate the offshore wind power [2]. Also, the first meshed HVDC system has already been commissioned in China, the Zhangbei grid with initially 4-terminals, but to be upgraded with 3 more terminal stations in the following phases of the project [3].

Several evolutions for those HVDC projects are possible during their lifetime: new terminals can be added; new conductors (overhead lines or cables) can be also added (potentially changing the system configuration from radial to meshed); the system can also operate in N-1 configuration after a contingency, etc. In those cases, congestions can occur since the initial design and sizing of the system elements may not account for the evolutions and the corresponding increase in power transmission. In meshed HVDC systems, there is more than one path to transmit power from one terminal to another. The converter stations at the nodes can regulate the power flow at node level but they are not able to control independently the DC currents circulating inside the mesh, through the different DC conductors. The current distribution through those conductors depends on the conductor resistance relation [4]. Then, a conductor between two terminals can become overloaded while other paths between the same terminals exist and are underused. Since this cannot be solved by the converter stations, power curtailments or the upgrade of the conductors with larger cross-sections may be required.

As an alternative approach, several papers in the literature proposed to use power electronic converters to manage the current distribution in HVDC meshed systems. These converters are named power flow controllers (PFC) or current flow controllers (CFC) and they can be seen as the equivalent of flexible AC transmission systems (FACTS) for DC grids [5]. By inserting voltages in series with the conductors, the PFCs modify the current circulating through the conductors where they are connected. This way, additional degrees of freedom are provided to the transmission system operator (TSO) of the HVDC system. Among the proposed solutions, the most promising family of PFCs consists in DC/DC converters connected at a node of the grid, inserting voltages in series with two or more conductors. In the literature, several topologies have been presented with different levels of complexity and performance. Those PFCs are normally introduced with electric diagrams illustrating their control and operation, which are sometimes validated through simulations or in scaled-down prototypes tested in laboratory [6]. No full-power prototype has been built to the knowledge of the authors. However, some works have provided a preliminary sizing of a PFC, based on the converter specifications for certain case study [7]. The work in [7] shows that the required PFC for a HVDC grid of ±500 kV and currents up to 3 kA is a medium voltage converter that must insert voltages in the order of just several kV, although being insulated from ground for the high voltage. Complementary works have also analyzed the technical feasibility of such a converter, taking into account points such as the protection of the device, the cooling management, powering of the semiconductors at high voltage, among others [8]. Nevertheless, less attention is put into how to integrate those PFCs in the DC switchyard of the converter station. Usually, the works deal with the power electronics circuit but do not consider the required busbar arrangement, DC breakers, bypass switches, disconnectors, etc. to properly integrate the PFC.

On the one hand, a fault at a node of the HVDC grid can have major consequences, thus, the design of the switchyard at the node needs particular attention. Several solutions are possible [9]: using different types of switches, such as disconnectors, transfer switches, breakers, etc.; different busbar arrangements, such as single busbars, double busbars, one and a half breaker arrangement, etc. Fig. 1 and Fig. 2 illustrate two typical busbar arrangements, a single busbar single breaker and a double busbar single breaker, respectively. In case a fault in a busbar, considering a single busbar (see Fig. 1), the power exchange between the 3 terminals is totally stopped with the corresponding consequences that this can have for the system. Considering a double busbar (see Fig. 2), after a fault in one of the busbars, it is still possible to reconfigure the switches and resume the service between the different terminals using the other busbar. In the end, the choice between busbar arrangements is done according to availability and cost objectives bearing in mind the protection strategy of the HVDC grid. As the PFC is connected to a node, it is necessary to think of those aspects when integrating the device into the system. A fault in the PFC should not compromise the operation of the rest of the HVDC grid.

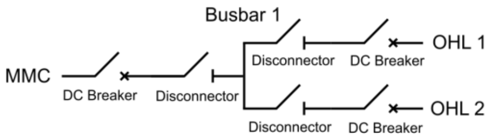

Fig. 1. Single busbar single breaker arrangement to connect a modular multilevel converter (MMC) with two overhead lines (OHL).

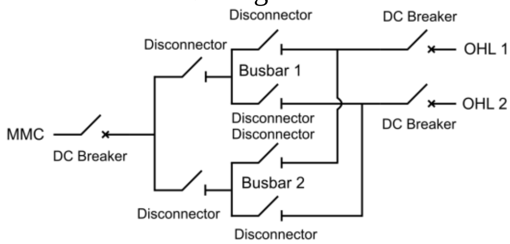

Fig. 2. Double busbar single breaker arrangement to connect an MMC with two OHL.

On the other hand, during the HVDC grid operation, it is likely that the PFC will not be permanently needed. Switches are then required to bypass and insert the power converter into the system without any grid shutdown. Besides, the PFC insertion and bypass, while the HVDC system is in operation, must be smoothly conducted, without disturbances in the HVDC grid. During PFC maintenance operations, the integration circuit must allow the grounding of the device without disturbing the network operation.

The purpose of this paper is to propose a busbar arrangement circuit providing good availability, moderate cost and allowing insertion, bypass and grounding of the PFC, while the rest of the system is in operation. Different busbar arrangements with a PFC are first analyzed, and two options are then selected, one of them inspired in a single busbar and another one in a double busbar. Then, the circuit inspired in a single busbar with the PFC is analyzed in detail. Its sequence of operation is defined, illustrating the switching pattern to insert, bypass and ground the PFC ensuring minimum disturbances in the HVDC network. The previous sequences are validated using simulations in EMTP and they also allow to assess the voltage, current and time requirements for the needed switches considering a certain case study. Depending on the configuration and the sequence of operations, there are cases where some switches should be able to open the circuit when the current flowing through them is null. In other cases, there is a low-impedance path in parallel with a switch which is opened when its current is at the rated value. The previous analysis provides the requirements for the switches of the selected busbar arrangement with PFC.

2. BUSBAR ARRANGEMENT WITH PFC

2.1. Overview of busbar arrangements with PFC

Several publications deal with possible busbars for HVDC grids, trying to minimize the requirement of HVDC breakers due to their high cost [9]. Those busbars are inspired in the arrangements used in AC, with many options being possible: single busbar single breaker, double busbar single breaker, one and a half breaker, double busbar double breaker, etc. When integrating the PFC into the HVDC grid, the choice of the busbar arrangement is not straightforward, and the number and type of switches depends on the expected availability in case of faults, cost objectives and the general protection strategy of the HVDC grid.
This work considers the single busbar and the double busbar scheme as a base to propose busbar arrangements with PFC. In those arrangements, the PFC replaces one of the busbars or is added as an additional PFC-busbar, with different configurations of switches. Busbar arrangements having 3 terminals are considered (for example, an MMC and 2 OHLs). To simplify the analysis, the number and disposition of HVDC circuit breakers is defined by establishing a minimum availability of the circuit when having faults in different points: For single busbar arrangements, it is defined that a fault in the busbar may stop the power transmission between the different terminals. For double busbar arrangements, it is defined that a fault in one of the busbars may temporally stop the power transmission between the different terminals, but after a switch reconfiguration, the power transmission can be

resumed. And for both types of busbars, it is defined that a fault in one of the terminals must be isolated without stopping the power transmission between the other terminals.
Based on the previous points, a DC circuit breaker in each terminal (3 in total) is considered for the following busbar arrangements with PFC. The rest of the switches in the different busbar arrangement options are expected to go from disconnectors to line transfer switches, in terms of requirements, but without current breaking capability. The analysed options are illustrated in Fig. 3.

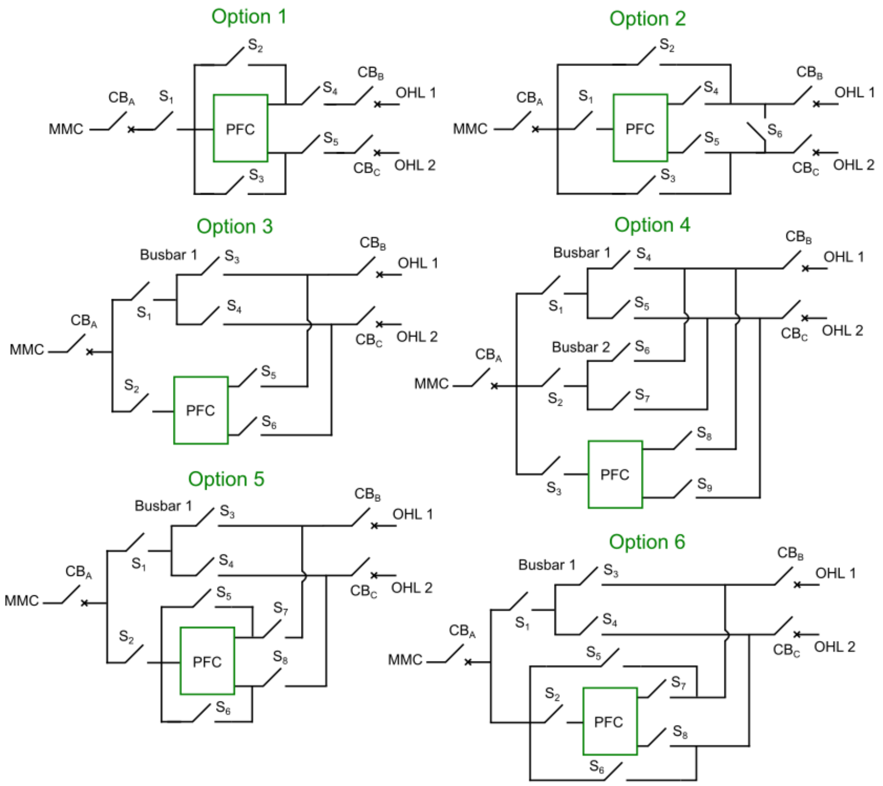

Fig. 3. Busbar arrangement options with PFC.

For each of the previous options, it is assessed if it is possible to resume the power transmission after a fault in the MMC, OHL 1, OHL 2, PFC and busbars, by rearranging the internal switches (assuming the switches in contact with the CB that opens the fault will open as well). Also, for each type of fault, the number of paths that the circuit provides is identified. Table I shows the previous analysis for the busbar arrangement in Option 2 as an example. A summary of the results of all the options is given in Table II.

Option 1 and 2 are inspired in single busbars, with option 2 having one more switch than option 1. They both provide a path for the power transmission when there is a fault in the MMC, OHL 1 or OHL 2. However, if a fault happens in the PFC in option 1, there is no possibility to resume the power transfer. While for option 2, the circuit provides 3 paths for that situation. Even considering a single busbar philosophy, since the PFC is a new element (with a robustness to be proven) to be introduced into the system, it seems reasonable in terms of a risk/reliability assessment to choose option 2 before option 1. This way, a fault in the PFC still allows to transmit power. Option 2 is the busbar arrangement that is used in the following sections to introduce the sequence of insertion, bypass and grounding. Regarding the other options, inspired from double busbars, option 3 is discarded since it provides low redundancy for a double busbar. A fault in busbar 1 implies to compulsorily use the PFC path to transmit power, even if the device is not necessary (increasing the losses of the system). Option 4 is also discarded, despite providing a lot of redundancy (many paths), since it is also the option with more switches and busbars. Finally, option 5 and 6 offer similar performances and the same number of switches. Option 5 has more redundancy when a fault happens in the MMC, while option 6 has more redundancy for PFCs faults. Following the previous argument, option 6 is chosen because it provides more redundancy for PFC faults (considering the lack of return of experience regarding the robustness of this device), but the consideration of other aspects could lead to also select option 5.

Table I. Fault analysis and possible paths to resume the power transmission for Option 2.

Faults	Switches	Comments
MMC	S_1 S_2 S_3 S_4 S_5 open / S_6 closed	1 path
OHL 1	S_1 S_2 S_4 S_5 S_6 open / S_3 closed	1 path
OHL 2	S_1 S_3 S_4 S_5 S_6 open / S_2 closed	1 path
PFC	S_1 S_4 S_5 open / S_2 S_6 closed / S_3 DM S_1 S_4 S_5 open / S_3 S_6 closed / S_2 DM S_1 S_4 S_5 open / S_2 S_3 closed / S_6 DM	3 paths PPC

PPC: Possible power curtailment since the PFC cannot be used. DM: Does not matter.

Table II. Summary of the fault analysis and possible paths to resume power transmission for the different options.

Faults/switches	**Op. 1**	**Op. 2**	**Op. 3**	**Op. 4**	**Op. 5**	**Op. 6**
MMC	1 path	1 path	1 path	2 paths	2 paths	1 path
OHL 1	1 path	1 path	1 path	2 paths	2 paths	2 paths
OHL 2	1 path	1 path	1 path	2 paths	2 paths	2 paths
PFC	No path	3 paths PPC	1 path PPC	4 paths PPC	1 path PPC	4 paths PPC
Busbar 1	-	-	1 path with PFC	2 paths (w/o PFC)	2 paths (w/o PFC)	2 paths (w/o PFC)
Busbar 2	-	-	-	2 paths	-	-
N° switches	5	6	6	9	8	8

2.2. Selected busbar arrangement

Option 2 has been selected in the previous section as a trade-off between simplicity and performance. Fig. 4 depicts the selected busbar arrangement including the grounding switches and the power electronic circuit of the PFC.

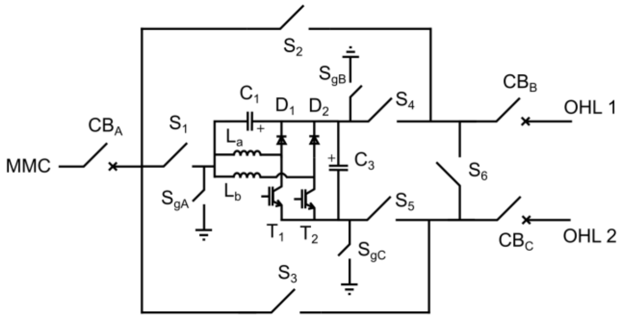

Fig. 4. Selected busbar arrangement with the chosen PFC converter.

The PFC topology considered in this study is the circuit proposed in [10], whose sizing was done in [7]. It is a unidirectional PFC converter with two interleaved branches. The current enters through S_1 and goes out through S_4 and S_5. By acting on the duty cycle to the transistors T_1 and T_2 (shifted a half of the period), the capacitor voltages are controlled, and the device can increase the current going to OHL 1 and reduce the current going to OHL 2 (with respect to the current values without PFC).

3. SEQUENCE OF OPERATION

In this section, the procedure to insert, bypass and ground the PFC is illustrated. The following subsections detail the sequence of switches that must be opened and closed. As mentioned before, the busbar arrangement to consider is the one depicted in Fig. 4. It must be noted that the sequences introduced in this section represent a possibility among several to achieve a smooth insertion, bypass and grounding, thus, other approaches could be also considered. In the following figures, the blue ellipses represent closed switches; the red ellipses, open switches; the green ellipses, that the switch can be open or closed; and the yellow ellipses, the semiconductors switching.

3.1. Insertion sequence

Fig. 5 to Fig. 10 present the steps to smoothly insert the PFC into the HVDC grid.

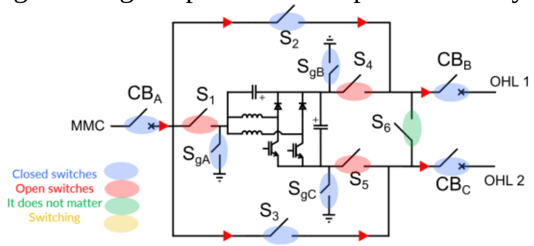

Fig. 5. Insertion sequence: step 1. PFC bypassed and grounded.

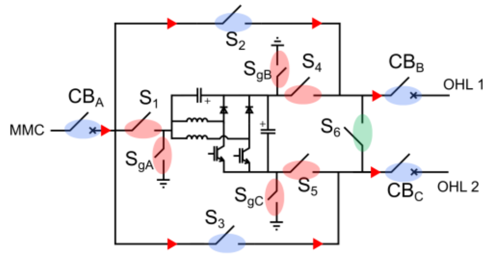

Fig. 6. Insertion sequence: step 2. PFC ungrounded.

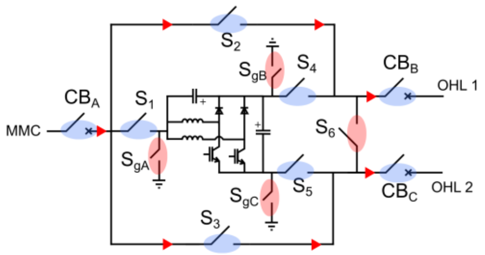

Fig. 7. Insertion sequence: step 3. S_1, S_4 and S_5 closed, S_6 open.

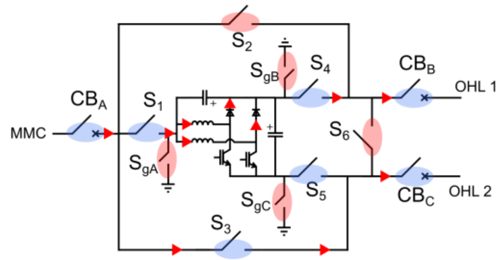

Fig. 8. Insertion sequence: step 4. S_2 open.

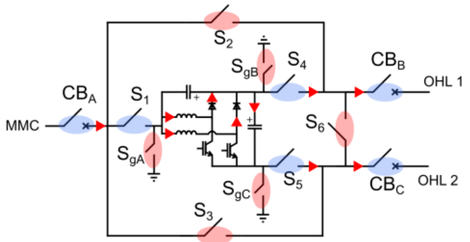

Fig. 9. Insertion sequence: step 5. S_3 open.

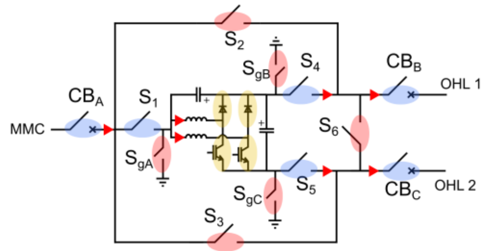

Fig. 10. Insertion sequence: step 6. PFC in operation.

It is considered that the HVDC grid is exchanging power at the moment of the PFC insertion (current direction given by the red arrows). Initially, at step 1, the PFC is grounded and the bypass switches, S_2 and S_3, are closed, allowing the power transmission through the circuit. In step 2, the grounding switches open and then, in step 3, S_1, S_4, S_5 close, connecting the PFC to the high potential. At this moment, the current through the PFC is almost 0 since it represents a higher impedance path compared to the bypass switches. At step 4, S_2 opens, switching the current into the PFC. Since S_2 has to switch the nominal current to a parallel path, the requirements are checked in the next section. The current at this point circulates through two paths: S_3 and through the LC circuit and the PFC diodes, resulting in an oscillatory behaviour. Then, in step 5, the S_3 opens, switching the current into the PFC. It is important to ensure a path for the current of OHL 2 after opening S_3, otherwise, the current will charge the capacitor C_3 until it stops the current going to OHL 2. To avoid that, in step 6, the IGBTs start to switch (this could be done at the same time than opening S_3). In order to smoothly start the operation of the PFC, a duty cycle that corresponds to the initial current relation between the currents of OHL 1 and OHL 2 is used. By doing this, the PFC does not modify the HVDC grid currents and the capacitors maintain a low voltage. Once in operation, the PFC can be controlled by changing the duty cycle or changing the setpoint of the corresponding current loop [7].

3.2. Bypass and grounding sequence

Fig. 11 to Fig. 16 show the steps to bypass, isolate and ground the PFC.

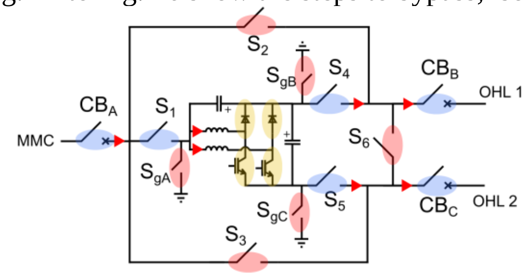

Fig. 11. Insertion sequence: step 1. PFC in operation.

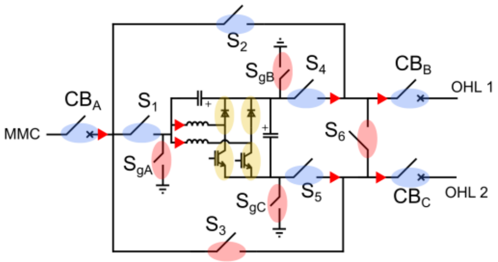

Fig. 12. Bypass sequence: step 2. S_2 closed.

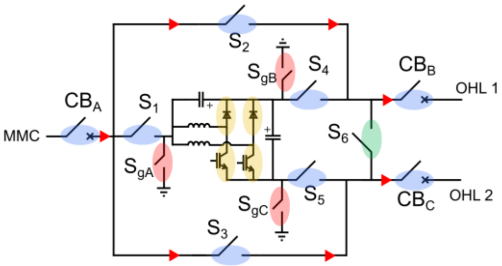

Fig. 13. Bypass sequence: step 3. S_3 close, PFC bypassed

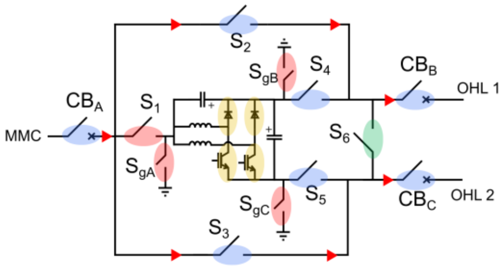

Fig. 14. Bypass sequence: step 4. S_1 open

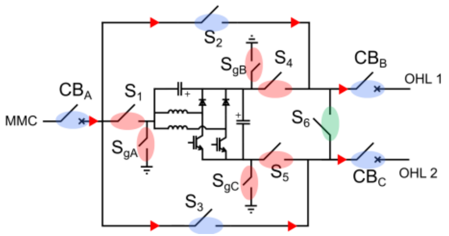

Fig. 15. Bypass sequence: step 5. S_4 and S_5 open, PFC isolated

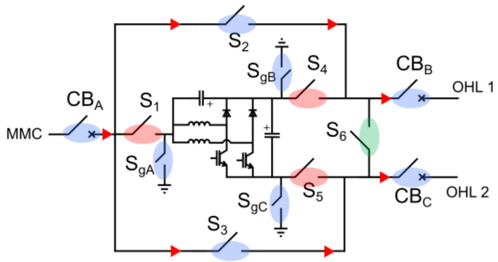

Fig. 16. Bypass sequence: step 6. PFC grounded.

At the starting of the sequence, the PFC is controlling the current with a certain duty cycle as in the scheme shown in Fig. 11 (step 1). The first step consists in applying the duty cycle equivalent to the relation between currents OHL 1 and OHL 2 when the PFC is bypassed, to discharge the PFC capacitors. By doing this, the PFC is switching, but it is not modifying the natural current distribution. Then, S_2 closes while the voltage across capacitor C_1 is very low. At step 3, S_3 also closes and now the current is redirected from the PFC to the bypass switches S_2 and S_3, with a much lower impedance. Then, with most of the current circulating through the bypass switches, S_1 opens with a current close to 0. Consequently, at step 4, S_4 and S_5 can open with null current and the PFC gets isolated from the high voltage potential. Finally, the grounding switches close and bring the PFC at ground potential in step 6.

4. CASE STUDY

The case study considers the Zhangbei HVDC grid in China [11] to test the insertion and bypass sequence introduced in the previous section. The power electronic circuit of the PFC is the result of the sizing process explained in [7]. Fig. 17 presents the HVDC grid and the location of the PFC with the power values being exchanged in each station. The model of the PFC and the HVDC grid that is used for the insertion sequence is depicted in Fig. 18. Notice that for the bypass switches S_2 and S_3, a switch model implementing the effect of the arc behaviour when opening the switch is considered. For the bypass sequence, S_2 and S_3 are replaced by ideal switches and S_1 is implemented with the previous switch arc model. The model also considers contact resistances (R=0.001 Ω) and stray inductances (L=1 μH) between the switches and the PFC circuit to assess the effect on the switches' requirements.

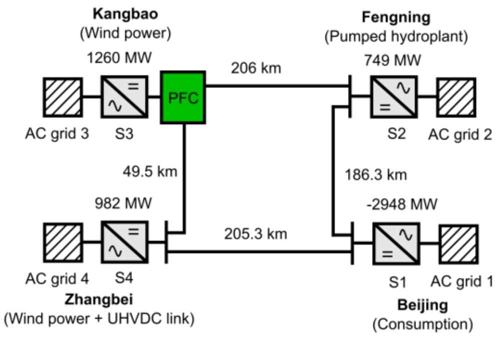

Fig. 17. Zhangbei HVDC grid with the PFC installed in station 3.

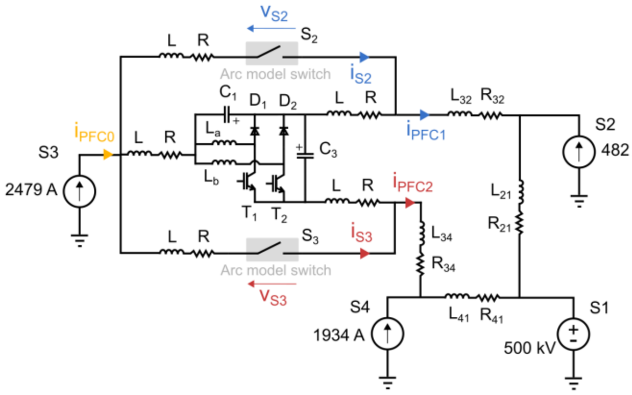

Fig. 18. Model of the PFC and HVDC during the insertion sequence in EMTP.

4.1. Insertion sequence results

The simulation results of the insertion sequence are shown in Fig. 19 and Fig. 20.

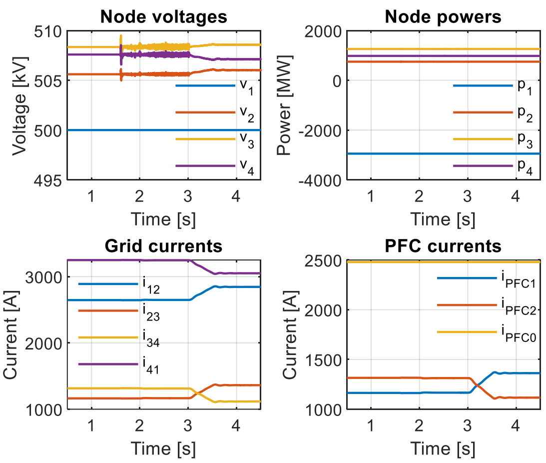

Fig. 19. Insertion sequence simulation results.

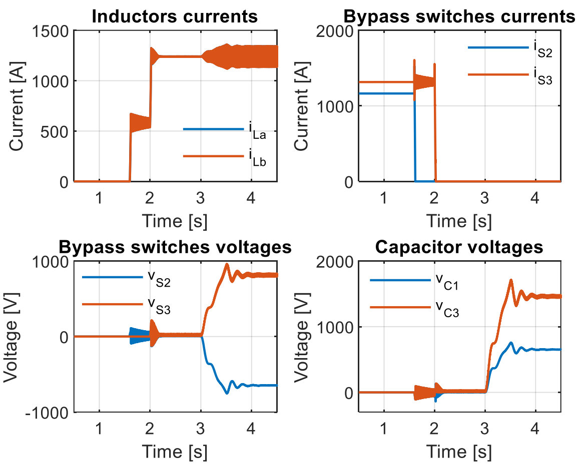

Fig. 20. Insertion sequence simulation results.

The simulations start at step 3 (see Fig. 7) with the PFC bypassed. At t=1.6 s, S_2 opens, switching the current into the LC circuit of the PFC. After, at t=2 s, S_3 opens and at the same time a duty cycle corresponding to the current relation is sent to the IGBTs. It can be seen that the voltages of the capacitors are kept at a low value after a short transient and the grid currents are not modified. Then, at t=3 s, the duty cycle is ramped down from 0.5305 to 0.45, modifying accordingly the grid currents. It is possible to notice that the capacitors charge to apply this change. During the insertion process the node powers are kept constant and the node voltages suffer only small oscillations in the order of some kV.

4.2. Bypass sequence results

The simulation results of the bypass sequence are shown in Fig. 21 and Fig. 22. The simulations start at step 1 (see Fig. 11) with the PFC applying a duty cycle equal to 0.45 with the capacitors charged and modifying the grid current distribution. At t=3.5 s, the duty cycle is ramped up until 0.5305 (corresponding to the natural current distribution). It is possible to see that by doing this, the capacitors discharge and the current distribution is modified. S_2 and S_3 are closed at t=4.6 s and t=5 s, respectively. After t=5 s, the current is switched from the PFC to the bypass switches (S_2 and S_3) since it provides a very low impedance path. With almost 0 current, S_1 opens at t=5.7 s, bypassing completely the PFC (notice that the opening of S_4 and S_5 will be done at 0 current after opening S_1 and they are not included in the simulation). Then the current flows entirely through the bypass switches and the PFC can now be grounded after opening S_4 and S_5.

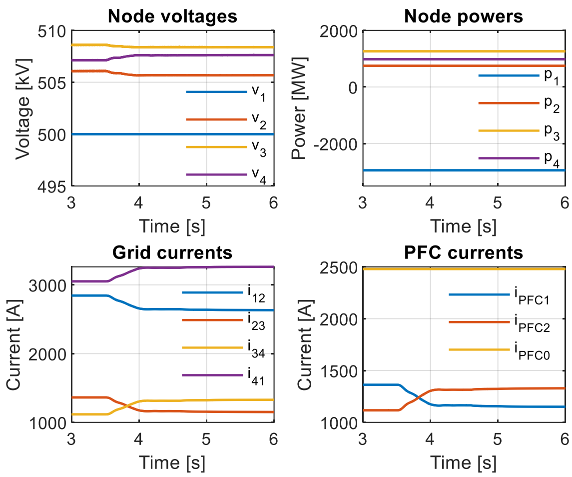

Fig. 21 Bypass sequence simulation results.

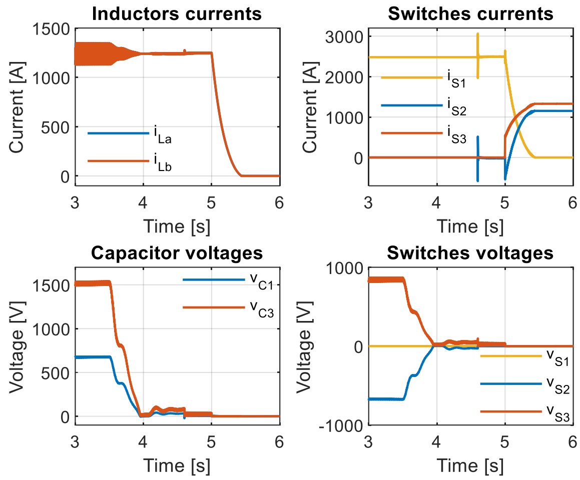

Fig. 22. Bypass sequence simulation results.

4.3. Requirements of switches

This section shows in detail the current and voltage values when opening the external switches of the PFC, to assess what type of switches are required. Fig. 23 presents the current and voltage at the instant of the opening for switches S_2 (first column), S_3 (second column) and S_1 (third column). The first two columns of graphics correspond to the insertion sequence, while the third one corresponds to the bypass sequence.

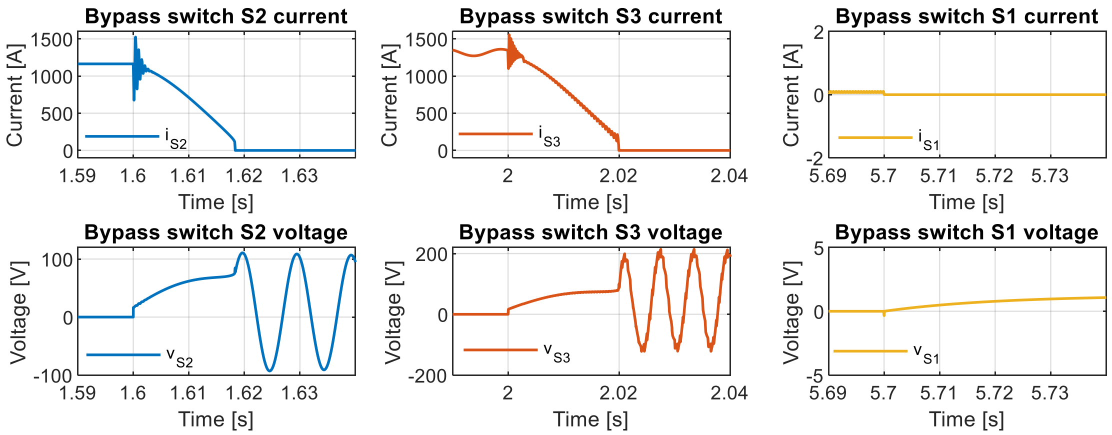

Fig. 23. Voltage and current values across the switches S_2, S_3 and S_1 during their opening.

On the one hand, for both S_2 and S_3, in the instant of opening during the insertion sequence, the current to be switched is in the order of 1.2-1.3 kA. The opening takes around 20 ms and during this time the voltage across the switch is in the order of 80 V. On the other hand, S_1 opens a current lower than 0.1 A, with a very small voltage applied on it, less than 1 V.

Based on this, S_2 and S_3 have requirements in between transfer line switches and transfer busbar switches. Consequently, their constraints are much lower than DC breakers. There exist switches in already built HVDC projects, such as the metallic return transfer breaker (MRTB), that have higher specifications, meaning that the technical feasibility of these bypass switches is not questionable [12].

Regarding S_1, the low requirements allow to implement the previous switch as a disconnector since the current and voltage are very low. The rest of the switches of the busbar arrangements do not seem to imply higher requirements, since S_4 and S_5 will open when the current is already 0. S_6 is not used in the previous sequences, it is required when a fault on the MMC happens and the system needs to be reconfigured to provide a new path between OHL 1 and 2. Since it is not used during normal operation, the constraints and sizing of this switch should come from protection studies [13], in which the S_6 operation is included in the corresponding sequence.

5. CONCLUSIONS

This work has introduced the concept of integrating a PFC into the DC switchyard of a converter station. Different busbar arrangements with their corresponding switches have been discussed and a circuit providing good availability, moderate number of switches and the capability to insert, bypass and ground the PFC has been selected. The paper has outlined the sequence of switches to be opened and closed to insert, bypass and ground the PFC. The simulation results show that the proposed sequence provides a smooth insertion and bypass of the PFC without disturbing the power exchanges within the HVDC grid. Additionally, the simulation results also provide the requirements for the external switches of the PFC. It has been seen that the bypass switches have significant constraints, but they are below the requirements of already used switches in the HVDC projects, meaning that their feasibility is not questionable. The requirements of the other switches in the busbar arrangement are expected to be much lower. Then, this work confirms that the PFC can be inserted, bypassed and grounded without disturbing the power transmission in the HVDC grid, using switches technically feasible during normal operation. Further work should analyze the system under abnormal conditions, such as faults, to obtain the PFC constraints in terms of protection.

ACKNOWLEDGMENTS

This work was supported by a grant overseen by the French National Research Agency (ANR) as part of the “Investissements d’Avenir” Program ANE-ITE-002-01.

BIBLIOGRAPHY

[1] D. Van Hertem, O. Gomis-Bellmunt and J. Liang, “HVDC Grids: For Offshore and Supergrid of the Future” (IEEE Press Series on Power Engineering, Ed. John Wiley & Sons, 2016).

[2] Amprion, 2020, "Amprion connects climate protection by innovation”, 20-09-2021 [online] https://www.amprion.net/Bilder/Netzjournal/2020/Eurobar/Eurobar_Handout_final_EN.pdf

[3] G. Buigues, V. Valverde, A. Etxegarai, P. Eguía, E. Torres, “Present and future multiterminal HVDC systems: current status and forthcoming” (Int. Conf. on Renewable Energies and Power Quality (ICREPQ’17) Malaga, April 2017, pp. 1-6).

[4] E. Veilleux and B. Ooi, “Power flow analysis in multi-terminal HVDC grid,” (Power Systems Conf. and Expo. (PSCE), 2011, pp. 1-7).

[5] O. Gomis-Bellmunt, J. Sau-Bassols, E. Prieto-Araujo and M. Cheah-Mané, “Flexible Converters for Meshed HVDC Grids: From Flexible AC Transmission Systems (FACTS) to Flexible DC Grids” (IEEE Trans. on Power Del., vol. 35, no. 1, Feb. 2020, pp. 2-15).

[6] C. Barker and R. Whitehouse, “A current flow controller for use in HVDC grids,” (IET Int. Conf. on AC and DC Power Trans. (ACDC), 2012, pp. 1-5).

[7] J. Sau-Bassols, F. Morel, T. Sellé, S. Poullain and F. Jacquier, "Methodology to obtain the specifications and perform the sizing of a power flow controller for meshed HVDC grids," (23rd European Conf. on Power Electr. and Appl. (EPE'21 ECCE Europe), 2021, pp. 1-10).

[8] J. Sau-Bassols, F. Morel, T. Sellé, S. Poullain and F. Jacquier, “Technical feasibility of Power Flow Controllers for HVDC grids” (AEIT HVDC virtual conference, 2021, pp. 1-6).

[9] E. Torres, *et al* “Busbar Configurations for HVDC Grids” (Int. Conf. on Renewable Energies and Power Quality (ICREPQ’16) Madrid, May 2016, pp. 1-5).

[10] S. Touré, F. Morel and S. Poullain, “Power flow control device for controlling the distribution of currents in a mesh network”, (EP3656030 B1, 2020).

[11] G. Tang, H. Pang, Z. He, X. Wei, “Research on Key Technology and Equipment for Zhangbei 500 kV DC Grid” (Int. Power Electr. Conf. (IPEC), Niigata 2018, pp. 1-9).

[12] Working Group A3/B4.34 CIGRE. “Technical requirements and specifications of state-of-the-art HVDC switching equipment” (number 683 April 2017 pp. 1-240).

[13] S. Poullain, F. Morel and S. Touré, “System comprising a power flow control device used to control the distribution of currents in a grid network and means for protecting said device”, (EP3799671 A1, 2021).