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Selective sublimation of GaN and regrowth of AlGa_N to co-integrate enhancement mode and depletion mode high electron mobility transistors

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ABSTRACT.

In the present study, the selective sublimation of the p-GaN cap layer of Al(Ga)_N/GaN HEMTs is developed to replace the commonly used dry etching with no risk of damage in the barrier layer in order to fabricate enhanced mode transistors. Thanks to this approach, enhancement-mode transistors are fabricated with a threshold voltage between 0V and +1.5V depending on the barrier layer aluminum molar fraction and thickness. Furthermore, we show the benefit of the combination of selective sublimation with the regrowth of AlGa_N to reduce access resistance in these transistors which can be co-integrated with depletion-mode devices fabricated in the same process in areas where p-GaN has been totally evaporated.

Keywords: *A1. Selective sublimation, A3. Local area epitaxy, B1. Group III-Nitrides, B3. High electron mobility transistors*

Introduction

High electron mobility transistors (HEMTs) based on the AlGa_N/GaN heterostructure have shown interests in many power applications that benefit from outstanding properties of GaN material such as high breakdown voltage, high electron velocity and good thermal conductivity [1]. To date, the main successes in GaN electronics have been obtained with depletion-mode (D-mode) devices [2-4]. Implementation of enhancement-mode (E-mode) transistors, which is much more difficult to achieve, is one of the biggest challenges to fulfilling the functionality of GaN HEMTs. After many intensive efforts, E-mode GaN

transistors have been attained through multiple approaches [5-11]. For example, fluorine implantation and gate recess are proposed to shift the threshold voltage V_{th} of AlGaIn/GaN HEMTs from a naturally negative value towards a positive one, and then to produce an E-mode device [5-8]. However, the thermal stability of fluorine implantation remains questionable and the recess etching of the barrier layer is difficult without any electrical degradation impacting the device performance.

Using a thin AlN barrier, less than 2 nm, can prevent two-dimensional electron gas (2DEG) formation, and hence can shift the threshold voltage V_{th} to a positive value [10], however it also can induce a dramatic reduction of the device current because of large access resistances. The use of a p-type doped GaN cap layer to raise the conduction band is another efficient method to shift the threshold voltage towards positive values [11], but in that case the p-GaN should be present only just under the metal gate to allow the electrons to flow through the source and drain access regions of the transistors. This can be obtained by local area growth of the p-GaN gate with difficulties associated with regrowth interface contamination with n-type dopants like silicon [12]. For this reason, most of the developments are based on dry etching of the p-GaN cap layer grown planar on Al(Ga)N/GaN HEMT heterostructures. Again, dry etching of p-GaN necessitates a very careful process to limit electrical damages possibly induced at the surface or inside the Al(Ga)N barrier with an additional difficulty concerning the selectivity of etching with respect to Al(Ga)N. To circumvent those drawbacks, we propose to use an innovative technology consisting of selective evaporation [13,14] of p-GaN and the regrowth of AlGaIn material. It will significantly reduce the electrical resistance in the E-mode transistor access regions [15,16] and provide elsewhere the negative threshold voltage desired for D-mode co-integrated devices.

Process description

The main steps of the process are depicted in Fig.1. The Al(Ga)N/GaN HEMT epi-layers are first grown by molecular beam epitaxy (MBE) on a Si(111) substrate. After nucleation of an AlN layer and growth of an AlGaIn/AlN stress mitigation stack, a 1.5 μm thick GaN buffer layer is grown followed by the Al(Ga)N barrier. In the present study, two kinds of barriers are grown: either a 15 nm thick $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ barrier, or a thin 2 nm AlN barrier. These HEMTs structures are grown in a Riber Compact 21 reactor equipped with an ammonia source [17]. A 50 nm thick p-type doped GaN cap layer is regrown on these structures in another reactor, a Riber 32 equipped with a solid Magnesium source [18]. The epilayer is covered by a 100 nm thick SiO_2 mask layer deposited by plasma enhanced chemical vapour deposition (PECVD) at 350°C. Large patterns of 4x4 mm² squares are formed by using photolithography and reactive ion etching (RIE) to define the areas for fabrication of E-mode and D-mode operation HEMTs (Fig. 1a). To form the E-mode device, the SiO_2 mask is kept on areas where the p-GaN has to be protected from any evaporation, i.e. gate patterns (Fig.1b). Then the sample is transferred into the MBE reactor for GaN sublimation

(Fig.1c). The selective evaporation is performed under ultra-high vacuum after heating the sample under ammonia and stopping the gas supply once the desired temperature between 850 and 900°C is reached. Evaporation proceeds at pressure below 10^{-7} Torr via the formation of islands [13]. Reflection high energy electron diffraction (RHEED) is employed to detect when the evaporation reaches the Al(Ga)N layer and the spotty pattern recovers to streaky (Fig.2a-d). The evaporation is stopped due to the high thermal stability of AlN. Even when Ga and N could leave the surface of AlGa_{0.8}N, the latter could become Al-rich AlGa_{0.8}N or pure AlN which don't decompose. Then, a nominal ammonia flow of 200 sccm is restored and the sample is either cooled-down for E-mode (Fig.1d) and D-mode (Fig.1e) transistor fabrication or a 20 nm thick of Al_{0.2}Ga_{0.8}N barrier layer is regrown to form D-mode devices as well as source/drain access regions of the E-mode HEMTs (Fig.1f). As shown in Fig.2e, the streaky RHEED pattern is preserved attesting to a 2D growth of AlGa_{0.8}N with metal polarity evidenced by the surface reconstruction [19] shown in Fig.2f. The device process steps start with the SiO₂ mask removal with a buffered oxide etchant (BOE) followed by mesa isolation using Cl₂/Ar/CH₄ RIE. Ohmic contacts of Ti/Al/Ni/Au are deposited, followed by a rapid thermal annealing at 750°C in a nitrogen atmosphere in 30s, consistently obtaining a contact resistance of 0.2-0.3 Ω.mm. For the aim of fabricating the D-mode and E-mode devices at the same time, gate contacts of Ni/Au sequences are evaporated simultaneously on the p-GaN layer of the E-mode devices and on the Al(Ga)N layer of the D-mode ones. Other metal stacks of Ni/Au are then deposited to form the pads of gate and Ohmic contacts for electrical measurements with the needle probes. The last step consists of the on-wafer electrical characterizations including Hall effect and DC I-V.

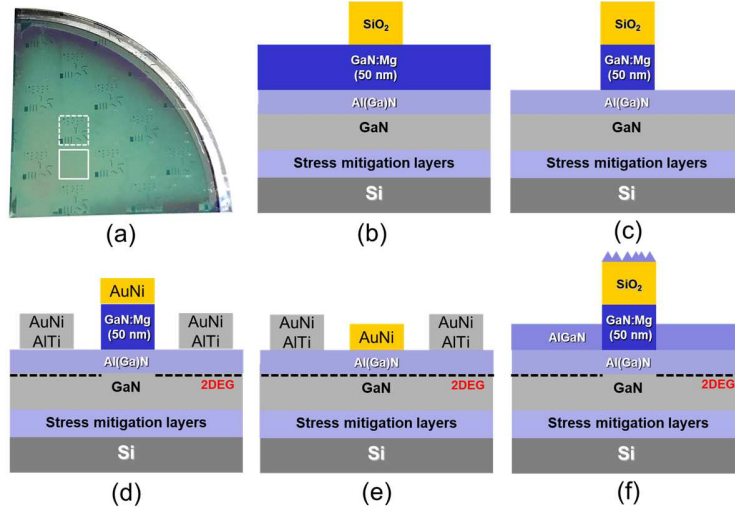


Figure 1. Schematic of the fabrication process enabling the co-integration: (a) photograph of the quarter wafer with SiO₂ patterned for E-mode transistors (area defined by a dashed line) and D-mode devices (area defined by a continuous line); (b) Definition of the E-mode gate pattern on the initial epi-layers covered with SiO₂; (c) sublimation of the p-GaN cap; (d) fabrication of an E-mode transistor; (e) fabrication of a D-mode transistor; (f) alternative process with regrowth of AlGa_{0.8}N after p-GaN sublimation.

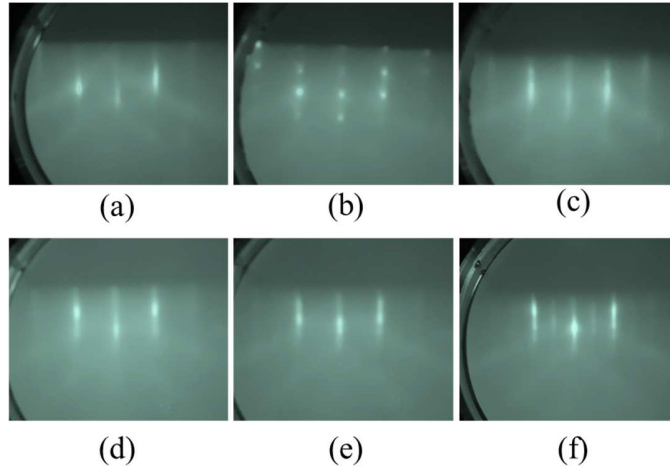


Figure 2. RHEED patterns of (a) the GaN surface at 900°C under NH₃; b) 1 min and c) 50 min after closing the NH₃ supply; (d) at 800°C under NH₃; (e) after AlGaN regrowth and (f) at 500°C under NH₃.

Structural analysis

The crystalline quality of the epilayers was assessed by X-ray diffraction with a Panalytical X'PERT Pro MRD system. 2 theta-omega scans around (002) or (004) reflexions corresponding to planes perpendicular to the growth axis are reported in Fig.3. Spectra recorded on the HEMT structure with a 15 nm thick Al_{0.26}Ga_{0.74}N barrier and a 2 nm thick AlN barrier are reported in Fig.3a and Fig.3b respectively. In Fig.3b, the large difference of form factor and lattice parameter between AlN and GaN exacerbates the Pendellösung fringes generated by the presence of the 50 nm p-GaN cap (spectrum 1). The fringes totally disappear in spectrum 2 owing to the fact that the remaining p-GaN occupies a very limited fraction of the surface corresponding to the gate patterns of E-mode transistors. However, such process revealed a totally depleted structure not compatible with the fabrication of transistors, so that the regrowth of AlGaN has been achieved after sublimation of p-GaN on another piece of the original sample. Fig.3b clearly shows the rise of a new peak due to the regrown Al_{0.2}Ga_{0.8}N layer (spectrum 3) that covers almost the totality of the sample. Also, the AlGaN barrier peak present in spectrum 1 of Fig.3a almost disappeared since spectrum 2 has been recorded after the device process in which a large part was etched for device isolation. On the other hand, for both kinds of structures, negligible change is noticed for other features like peaks due to the thick GaN buffer, the AlGaN in the stress mitigating stack and the AlN nucleation layer.

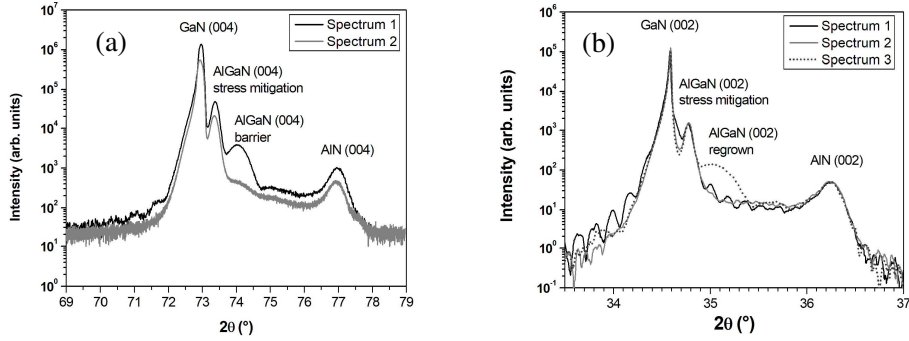


Figure 3. X-ray diffraction 2 theta-omega scans (a) around the (004) reflexion for the initial HEMT with 15 nm thick $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ barrier covered with p-GaN (spectrum 1) and after p-GaN selective sublimation (spectrum 2); (b) around the (002) reflexion for the initial HEMT with 2 nm AlN barrier covered with p-GaN (spectrum 1), after p-GaN selective sublimation (spectrum 2) and after AlGaN regrowth (spectrum 3).

The selectivity of GaN sublimation against Al(Ga)N barrier was demonstrated with RHEED (Fig.2) and confirmed by scanning electron microscopy (SEM), atomic force microscopy (AFM) and cross-section transmission electron microscopy (TEM) as shown in the next section. Furthermore, the AFM analysis confirms that the gate pattern defined with SiO_2 is replicated into the p-GaN after sublimation (Fig.4a-c). The morphology of the p-GaN surface as well as that of the AlGaN revealed after GaN evaporation is similar and typical for ammonia-MBE grown materials. The mounds with a typical diameter of 1 μm generate a moderate roughness with a root mean square value (RMS) less than 5 nm [20]. We recall that the RHEED patterns of the corresponding samples are streaky and this morphology doesn't affect the electron mobility of the two-dimensional electron gas (2DEG) as shown in our previous studies [12-17]. Fig.4d-f show the gate region after the regrowth of AlGaN. Again, similar surface morphologies are obtained. As the AlGaN regrowth is not totally selective with respect to SiO_2 , the latter has to be sufficiently thick to allow the lift-off of crystallites eventually nucleated on it (Fig.1f). The few spots present on Fig.4d are due to an incomplete cleaning after the removal of SiO_2 into a BOE 7:1 solution. The RMS roughness of the regrown AlGaN is 3 nm and unchanged compared to the one measured before and after p-GaN sublimation (Fig.4a). The pits seem at the surface of AlGaN with a density estimated to a few $10^9/\text{cm}^2$ are due to threading dislocations. Such a defect density is typical for the epilayer stack grown for this study [17].

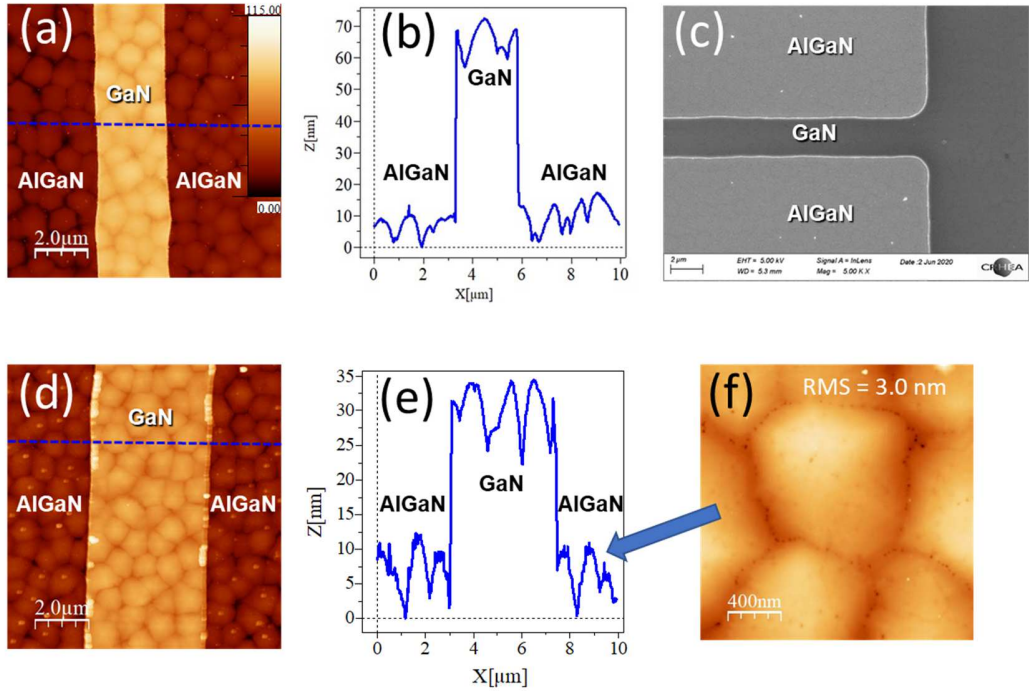


Figure 4. a) AFM view of a gate pattern after sublimation of the 50 nm GaN cap on the 15 nm AlGaIn layer covered with SiO₂ mask; b) height profile of the gate pattern; c) SEM view of gate pattern; d) AFM view of a gate pattern after evaporation of the 50 nm GaN cap on the 2 nm AlN layer and regrowth of 20 nm AlGaIn layer; (e) height profile of the gate pattern; (f) AFM view of the surface of the regrown AlGaIn.

Cross-section TEM observations performed after device fabrication and electrical characterizations complement this analysis of the p-GaN gate pattern definition. The cross-section views at different magnifications of the gate edge region of a transistor with p-GaN on Al_{0.26}Ga_{0.74}N barrier are shown in Fig. 5a-b. The observations are performed along the (11-20) zone axis. The darker pattern located on the p-GaN layer corresponds to the metal Schottky gate contact. In Fig.5a, the image shows threading dislocations of *a+c* type as well as *a* type ones. The picture demonstrates the filtering of dislocations in the bottom region of the GaN buffer grown on the AlGaIn/AlN stress mitigation stack. The location of threading dislocations is random and despite the large density estimated in the mid 10⁹/cm², their presence doesn't affect the evaporation selectivity nor the definition of the p-GaN gate edge with a rather steep slope. Similar behaviour is noticed for the 2 nm AlN barrier HEMT as shown in Fig.5c where dislocations and gate metal appear bright due to the dark-field imaging conditions. Furthermore, a perfect crystal continuity is noticed between the p-GaN at gate edge and the regrown Al_{0.2}Ga_{0.8}N layer as shown in Fig.5d.

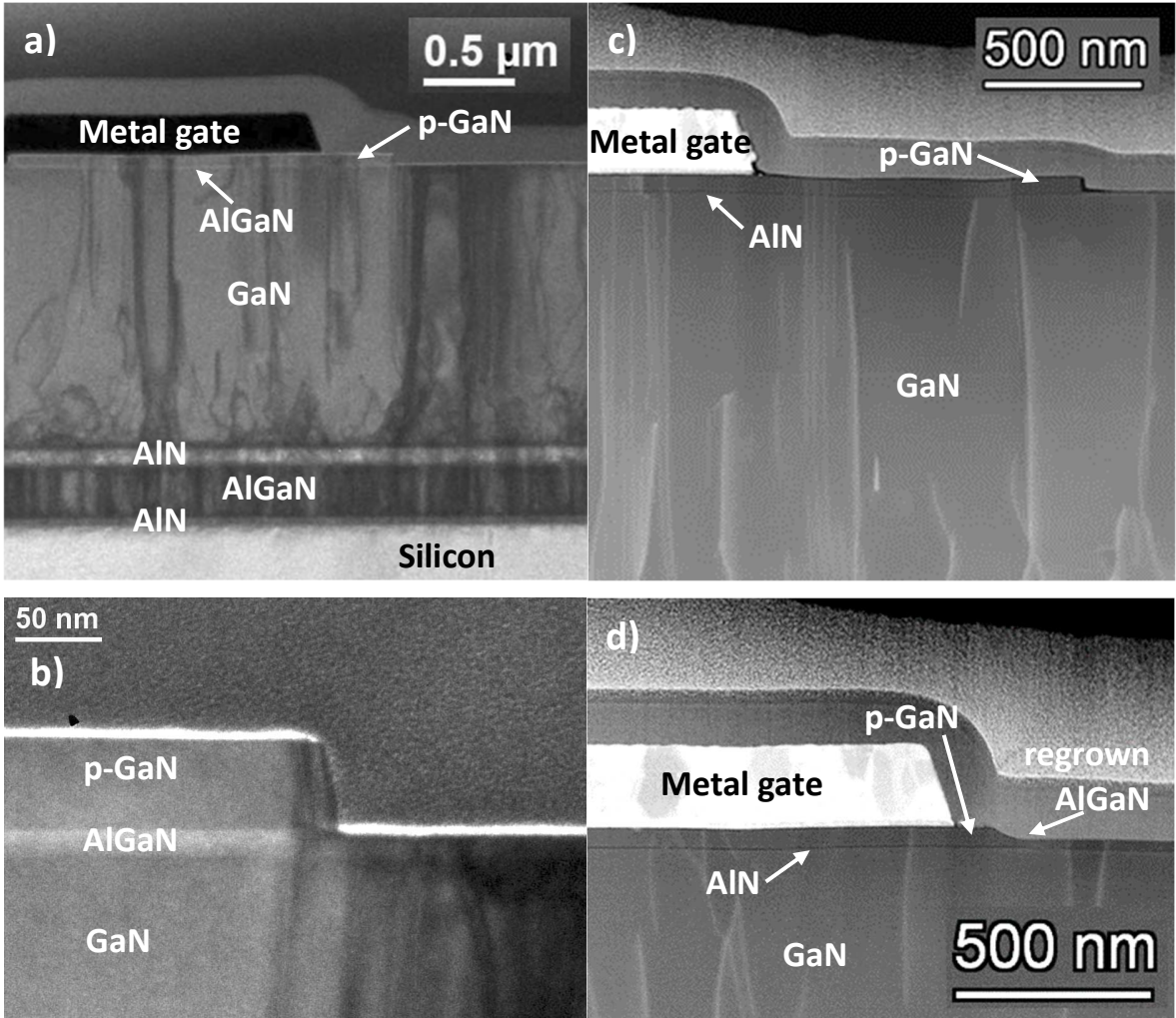


Figure 5. Cross-section electron microscope views of p-GaN gate edge (a-b) on the 15 nm thick $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ barrier, (c) on the 2 nm AlN barrier and (d) after regrowth of a 20 nm $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ layer.

Electrical characterizations

The electrical properties of the 2DEG extracted from the Van der Pauw patterns fabricated on wafer areas where p-GaN was evaporated are summarized in Table I. It is clear from this table that a HEMT with a 2 nm AlN barrier can already produce an almost normally-off transistor as a sheet resistance around 1 M Ω /sq is measured. On the contrary, a 2.5 nm AlN barrier is enough to generate a 2DEG with a density of $5 \times 10^{12}/\text{cm}^2$ and a sheet resistance greater than 1 k Ω /sq. On the other hand, the HEMT with a 15 nm $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ contains a 2DEG with a density between 4.3 and $5 \times 10^{12}/\text{cm}^2$ and a slightly lower resistance owing to a higher electron mobility. Such a mobility of 1500 $\text{cm}^2/\text{V}\cdot\text{s}$ attests to the quality of the $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}/\text{GaN}$ interface. Finally, after regrowth of $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ the initially depleted HEMT with a 2 nm AlN barrier exhibits a 2DEG with a density of more than $1.1 \times 10^{13}/\text{cm}^2$ and a mobility greater than 1100 $\text{cm}^2/\text{V}\cdot\text{s}$ resulting in a sheet resistance around 400 Ω /sq.

Table I. Comparison of sheet resistances, 2DEG carrier densities N_s and electron mobility μ deduced from Hall effect measurements performed on HEMT heterostructures grown with different barrier layers.

| Barrier layer | Rsh (ohm/sq) | N_s (/cm ²) | μ (cm ² /V.s) |
|--|--------------|-------------------------------|------------------------------|
| 2 nm AlN | 1 000 000 | n.a | n.a |
| 2.5 nm AlN | >1000 | 5×10^{12} | ~1000 |
| 15 nm Al _{0.26} Ga _{0.74} N | 800-900 | $4.3\text{-}5 \times 10^{12}$ | >1500 |
| 20 nm Al _{0.2} Ga _{0.8} N + 2 nm AlN | 400-414 | $>1.1 \times 10^{13}$ | >1100 |

Figure 6 shows the output and transfer characteristics of co-integrated 2.5 μm gate E-mode and D-mode transistors fabricated on the 15 nm Al_{0.26}Ga_{0.74}N barrier HEMT. The drain to source distance is 9.5 μm . The sheet resistance deduced from the measurements on transmission line method (TLM) devices is in the same range as the one measured on Van der Pauw patterns and extrapolation of the resistances indicates contact resistances around 0.5 Ohm mm. At $V_{gs} = 0$ V the maximum drain current of the D-mode transistor is $I_{ds}=116$ mA/mm and it reaches 360 mA/mm at $V_{gs} = +2$ V. The threshold voltage V_{th} defined at 1 mA/mm is around -1.5 V. A total resistance R_{on} of 7 Ohm.mm is deduced from the slope of the linear region of output characteristics $I_{ds}\text{-}V_{ds}$. On the other hand, the total resistance R_{on} of the E-mode transistor is 10 Ohm.mm. The threshold voltage V_{th} is between 0 V and +0,7 V and for a gate bias V_{gs} of +2 V a drain current of 175 mA/mm is measured. Further increase of V_{gs} to +3 V allows to reach 245 mA/mm.

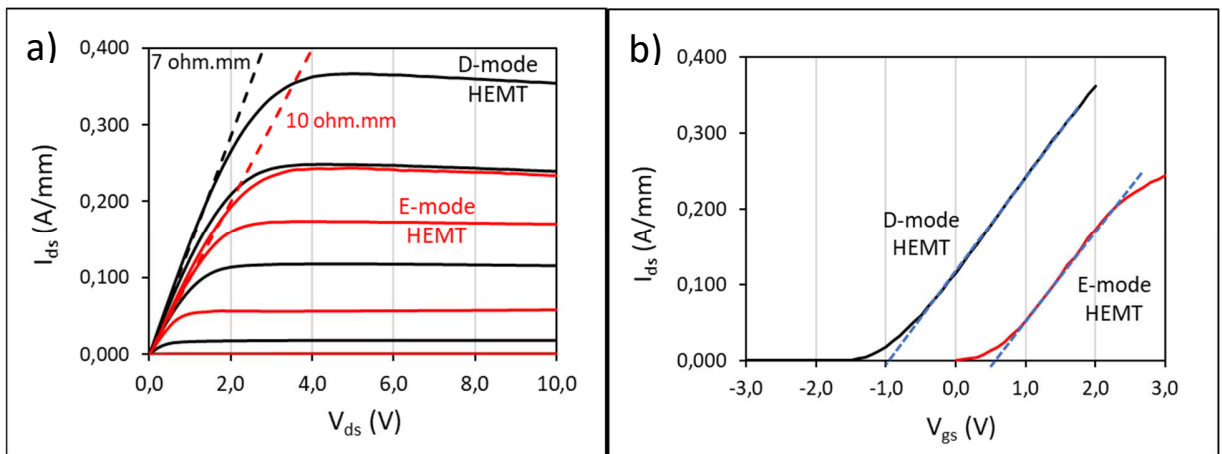


Figure 6. (a) Output and (b) transfer characteristics at $V_{DS} = 6$ V for the 2.5 μm gate E-mode and D-mode HEMTs with a 15 nm AlGa_N barrier.

We failed to fabricate transistors on a 2 nm AlN barrier HEMT due to the high sheet resistance around 1 MOhm/sq. Only the regrowth of AlGa_N allowed us to obtain contacts with an ohmic behaviour. Figure 7 shows the output and transfer characteristics of co-integrated E-mode and D-mode transistors fabricated on the 2 nm AlN barrier HEMT after the p-GaN sublimation and the 20 nm Al_{0.2}Ga_{0.8}N layer regrowth. The contact resistance extracted from TLM is 0.3 ohm.mm. The E-mode transistor exhibits a positive threshold voltage V_{th} slightly above 1.5 V and the drain current I_{ds} reaches 212 mA/mm at $V_{gs} = +5$ V. The regrowth of the Al_{0.26}Ga_{0.74}N layer onto the 2 nm AlN barrier allows a large number of electrons to populate the 2DEG at the AlN/GaN interface. It significantly reduces the electrical resistance in transistor access regions, hence results in the drain current I_{ds} of more than 200 mA/mm flowing between source and drain in the E-mode device. The total resistance R_{on} is around 8 Ohm.mm. Thanks to the regrown Al_{0.26}Ga_{0.74}N layer, the threshold voltage V_{th} of the D-mode co-integrated devices is shifted to a large negative value of -5.6 V. The total resistance R_{on} is 6 Ohm.mm and the drain current I_{ds} greater than 500 mA/mm at $V_{gs} = 0$ V, is beyond 700 mA/mm at $V_{gs} = +2$ V, which is almost twice the one previously achieved without AlGa_N regrowth in the D-mode transistor fabricated on a 15 nm Al_{0.26}Ga_{0.74}N barrier.

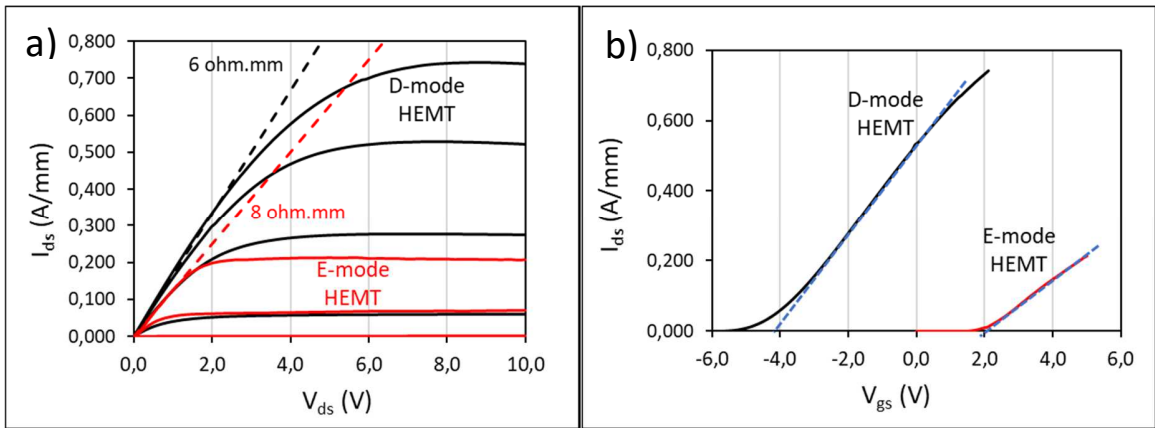


Figure 7. (a) Output and (b) transfer characteristics at $V_{DS} = 7$ V for the 2 μ m gate E-mode and D-mode HEMTs with a 15 nm AlGa_N layer regrown on the 2 nm AlN barrier.

Conclusions

In this work, integration of E/D-mode GaN HEMTs has been demonstrated. Starting from an initial p-GaN/Al(Ga)N/GaN HEMT structure grown on Silicon substrate, the selective sublimation method is first used to pattern the p-GaN gate for the E-mode transistors. The process based on the evaporation of GaN under high vacuum in an MBE reactor makes it possible to co-integrate E-mode with D-mode transistors with balanced maximum drain currents for a structure with a 15 nm Al_{0.26}Ga_{0.74}N barrier layer. However, the threshold voltage V_{th} of the E-mode transistor remains limited below +0,7 V and the maximum drain currents are lower than 250 mA/mm, even for the D-mode transistor. For applications requiring both a more positive threshold voltage of the E-mode device and a higher maximum drain current of the D-mode one, we proposed to evaporate p-GaN grown on top of a 2 nm AlN barrier HEMT structure and to regrow a 20 nm Al_{0.2}Ga_{0.8}N barrier layer. The E-mode transistor exhibits a positive threshold voltage of more than 1.5 V and the drain current can exceed 200 mA/mm at $V_{gs} = +5$ V. On the other hand, the D-mode device

exhibits a more negative pinch-off voltage of -5.6 V and a maximum drain current above 500 mA/mm at $V_{gs}=0V$. Beyond the feasibility of p-GaN sublimation to replace dry etching, this study shows that the necessary trade-off between the threshold voltage and the maximum drain current in the E-mode and in D-mode transistors is easier to achieve when the barrier layer design is combined with the regrowth of an additional barrier layer. Not only the regrowth allows the fabrication of co-integrated D-mode transistors, but it can significantly reduce the access resistances with resulting larger drain current in the E-mode devices.

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