



HAL
open science

Design methodology of a 28 nm FD-SOI Capacitive Feedback RF LNA based on the ACM Model and Look-up Tables

Giovani Britton, Estelle Lauga-Larroze, Salvador Mir, Philippe Galy

► **To cite this version:**

Giovani Britton, Estelle Lauga-Larroze, Salvador Mir, Philippe Galy. Design methodology of a 28 nm FD-SOI Capacitive Feedback RF LNA based on the ACM Model and Look-up Tables. Solid-State Electronics, 2022, 194, pp.108340. 10.1016/j.sse.2022.108340 . hal-03740211

HAL Id: hal-03740211

<https://hal.science/hal-03740211>

Submitted on 1 Aug 2022

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



Distributed under a Creative Commons Attribution - NonCommercial 4.0 International License

Design methodology of a 28 nm FD-SOI Capacitive Feedback RF LNA based on the ACM Model and Look-up Tables

Giovani Britton^{1,2}, Estelle Lauga-Larroze², Salvador Mir² and Philippe Galy¹

¹STMicroelectronics, 850 rue Jean Monnet, 38920 Crolles, France

²Univ. Grenoble Alpes, CNRS, TIMA F-38000 Grenoble, France

1. Abstract

The race to reduce the size and improve power consumption in new transistor technologies has given rise to design trade-offs that are difficult to address with standard methodologies that require an iterative process. This paper proposes a design methodology based on the ACM model and look-up tables to quickly size a 28 nm FD-SOI RF LNA that is intended to work down to 233.15 K as demonstrated with post-layout simulations results. The design incorporates different tuning knobs that might be useful for allowing the circuit to work at cryogenic temperatures during experimental measurements.

2. Introduction

As the size of silicon transistors is scaled down, there is a notable increase in performance regarding the speed of operation and power consumption of the devices. Although there are important improvements seen with transistor length reduction, such improvements are accompanied by the amplification of intrinsic parasitics and physical phenomena not perceived in large-length transistors. Classical design techniques become inadequate to deploy an effective design environment, forcing the designer to follow an iterative design process that heavily depends on simulation software. This type of approach can prove to be time-consuming and lacks insight regarding the working of the transistor.

The above-stated limitations can be tackled by using an adequate model that covers the behavior of the transistor at different working regions and which can be efficiently integrated on existing numerical computing environments together with Spice-based simulation software. We use for this the Advanced Compact MOSFET (ACM) model together with a Look-Up Table (LUT) in a co-simulation environment with MATLAB and Spice models [1] [2]. In this paper, we will describe this approach for the design of a capacitive feedback (CF) radio-frequency (RF) Low Noise Amplifier (LNA) designed to minimize power consumption and noise figure with suitable S-parameters at a working frequency of 7 GHz.

Referring to the state-of-the-art of CMOS LNAs in a similar frequency range (6.85-7 GHz), our design presents an important reduction of power consumption. Since we are also interested in experimenting the behavior of this LNA at cryogenic temperatures, several voltage bias are considered as tuning knobs to adapt the circuit performances as temperature decreases.

3. Capacitive feedback RF LNA

The core stage of the LNA is shown in Figure 1. This architecture allows, in principle, the matching of the input impedance via the passive components L_g and C_F while the stage gain is defined by the sizing of the transistor as we have done in [3] for lower frequency designs.

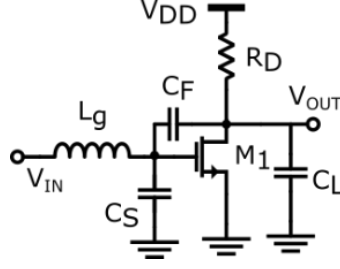


Figure 1: Capacitive feedback LNA

Since there will be an output stage, neglecting C_L with respect to C_F , the LNA gain is given by

$$G_{LNA} = \frac{sR_D C_F - g_m R_D}{s^3 R_D C_F C_S L_g + s^2 [C_F L_g (1 + g_m R_D) + C_S L_g] + s R_D C_F + 1} \quad (1)$$

with $A_{v0} = -g_m R_D$ is the DC gain. The zero in the numerator will typically occur well beyond the working frequency. A Zero-Value Time (ZVT) constants analysis allows a conservative estimation of the first cut frequency as

$$f_h \approx \frac{1}{2\pi} \frac{1}{R_D C_F + g_m L_g} \quad (2)$$

where the time constant $R_D C_F$ is dominant. Real and imaginary components of input impedance are given by

$$R_e \approx \frac{R_D C_F}{C_F (1 + g_m R_D) + C_S} \quad (3)$$

$$I_m \approx s L_g + \frac{1}{s [(1 + g_m R_D) C_F + C_S]} \quad (4)$$

This set of first order equations allows setting the gain, input impedance and working frequency as a function of the design parameters R_D , g_m , C_S , and L_g . Parasitic components of the inductance and amplifying transistor M1 play an important role.

4. Proposed LUT design methodology

The principal parameter to optimize is the noise figure of the system. This parameter will be taken to define the inversion region and a first bias point for the amplifier, which will be reconsidered later to address the other design objectives. An approximative relation for the minimum noise figure that can be obtained for a given transistor and inversion region is given by

$$F_{min} \cong 1 + \frac{\omega}{\omega_t} \quad (5)$$

where ω_t is the transit frequency [4]. First, with the aid of a MATLAB/Spice co-simulation, a sweep of the voltage in all terminals of a transistor is carried, and the obtained small signal parameters are stored in a LUT. With the use of this LUT, Figure 2 is obtained where g_m/I_d defines the inversion level. We can see that a high

V_{ds} and a strong inversion region in the transistor result in the smallest noise figure NF_{min} which also defines the value of the transistor length L . We consider this as the initial bias point. Next, with this bias point, we size the width W of transistor M1 by using the noise equations and the transistor ACM model [5].

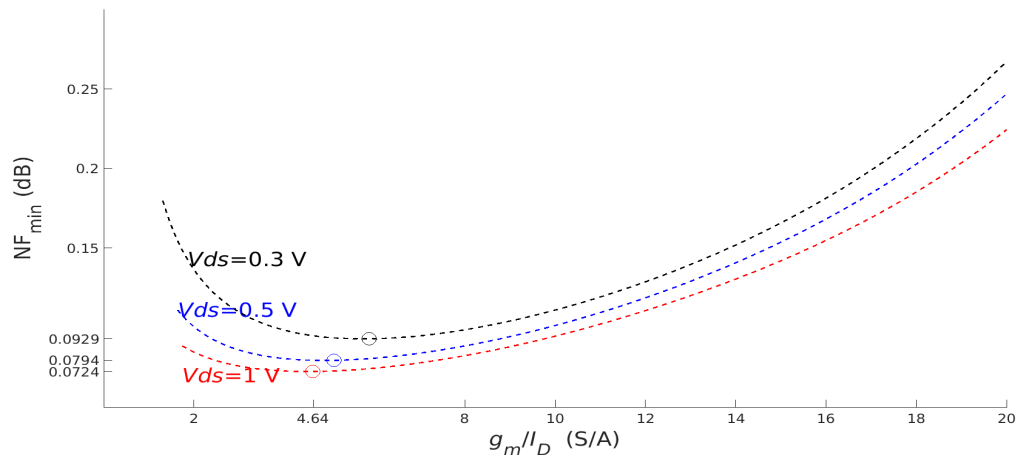


Figure 2: Minimum transistor noise figure vs inversion region (gm/ID).

Power consumption, working frequency, and noise figure can be simultaneously considered with the following Figure of Merit (FoM)

$$FoM = \frac{f_t g_m}{I_D} \tag{6}$$

where I_D is the bias current of the transistor. As shown in Figure 3, this FoM is optimized in a region of moderate inversion that we will consider since this addresses the design trade-offs.

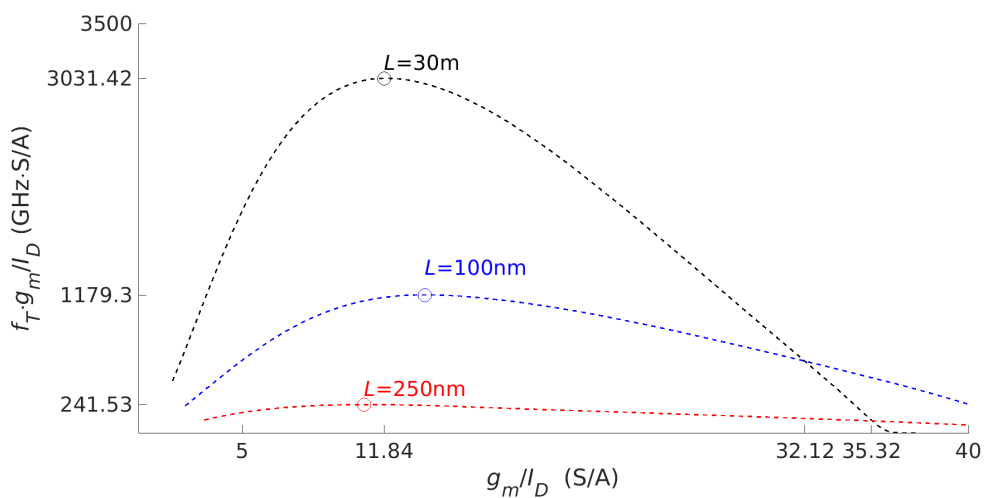


Figure 3: Power consumption, working frequency, and noise FoM vs inversion region.

For a common source resistive loaded amplifier, the DC gain, the load resistance, the bias current, and the transistor sizing are related by (7)

$$A_{v0} = -\frac{\frac{g_m}{I_D}}{\frac{1}{V_{EA}} + \frac{1}{I_D R_D}} \quad (7)$$

where V_{EA} is the Early voltage. Taking V_{DS} as the independent parameter, A_{v0} is plotted for a defined inversion level in Figure 4 [2]. A compromise is found between the length of the transistor, the gain as shown in Figure 4 and the FoM as shown in Figure 3.

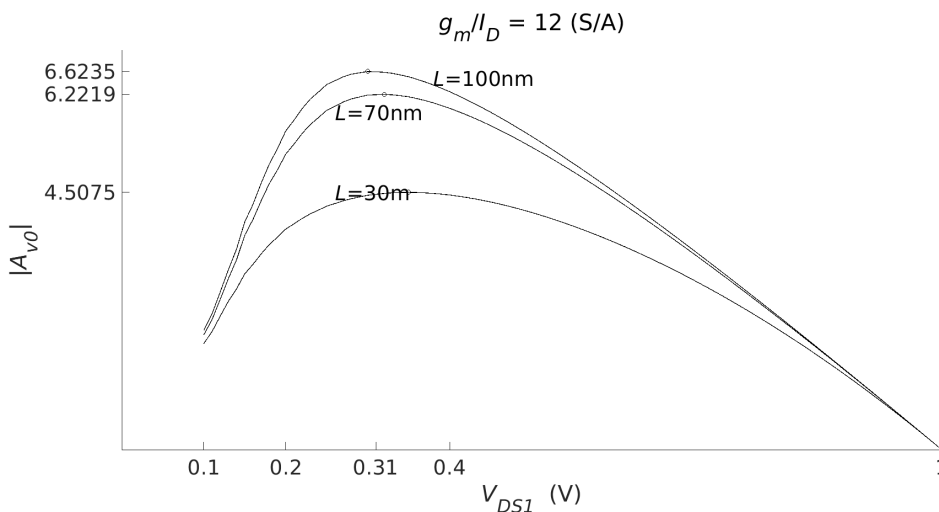


Figure 4: Low frequency voltage gain while varying L vs Vds.

The last step in the design procedure is to define the values of C_S, C_F and L_g to achieve the input matching for a given frequency response, while the output matching will be obtained by means of an additional output stage.

5. Simulation results

Our design in a 28 nm FD-SOI technology is shown in Figure 5. The targets for a working frequency of 7 GHz were noise figure lower than 2.5 dB at 233.15 K, gain above 10 dB, and power consumption lower than 1 mW. The schematic of the LNA in Figure 5(a) shows also the bias and output buffer blocks. In the layout of the test chip shown in Figure 5(b), the LNA is placed at the top. Additional single circuit elements (resistance, capacitance, inductance, transistor) are placed at the bottom of the test chip for characterizing them at low temperatures. This information will be helpful for understanding the LNA performances at low temperatures for experimental measurements, helping to tune the different bias voltages that are made independent. These include the power voltages of the input bias stage, LNA core and output stage, and the back-bias voltages of transistors M1/M2 and transistor M3, in total 5 tuning knobs. Figure 5(c) shows the post-layout simulation results at 233.15 K.

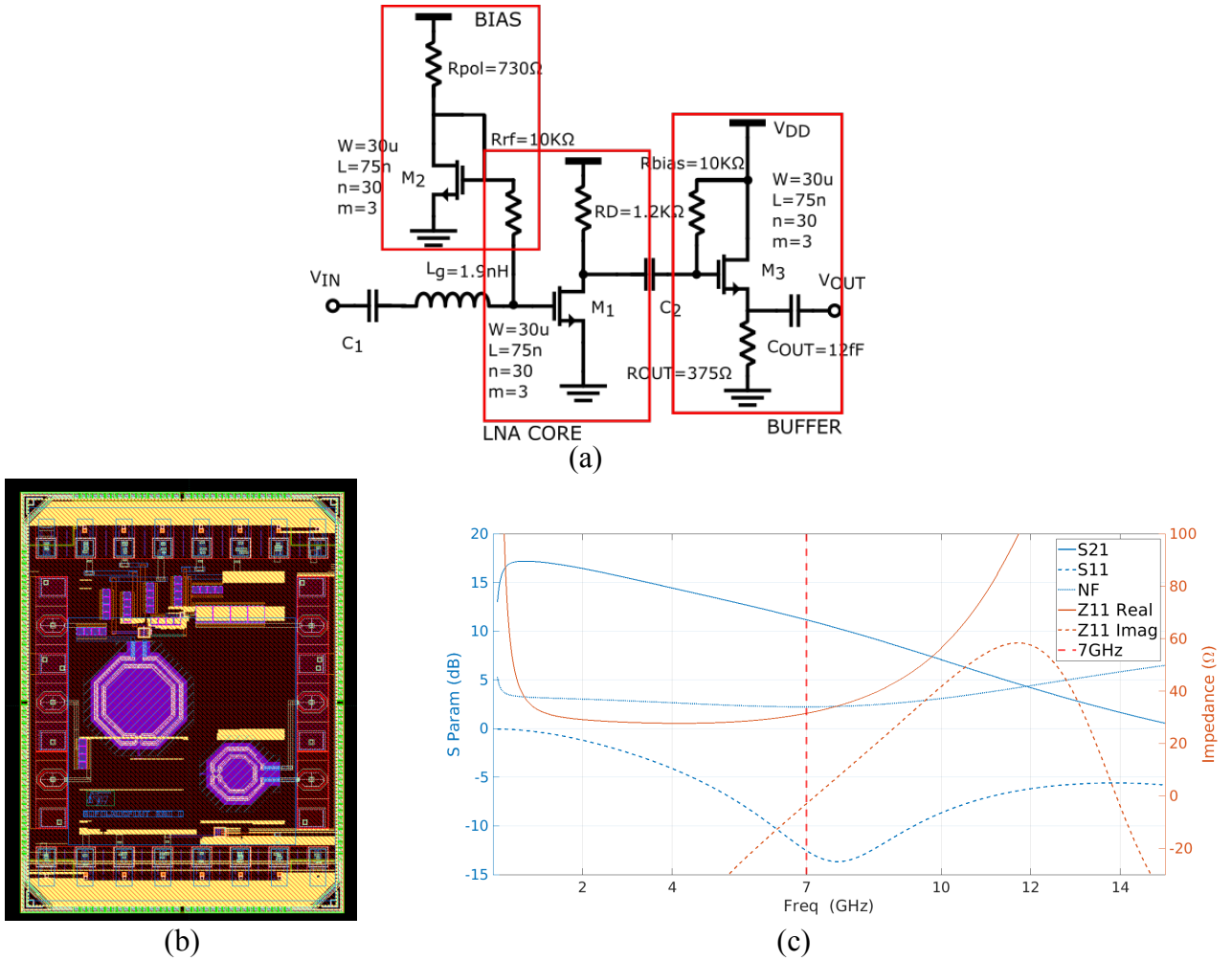


Figure 6: 28 nm FD-SOI LNA design: (a) schematics, (b) test chip, and (c) post-layout simulation results at 233.15 K.

Different FoMs have been used in the literature to compare the LNAs state of the art [6]. In our case, we consider the following figure of merit

$$FoM_0 = \frac{G[\text{lin}] f_0[\text{GHz}]}{(F-1)[\text{lin}] P_{DC}[\text{mW}]} \quad (8)$$

where G represents the gain, f_0 the working frequency, F the noise factor, and P_{DC} the power consumption. Table I summarizes the performances of the proposed LNA together with the state of the art at a similar working frequency and at room temperature. We obtain the highest FoM_0 thanks in particular to the very low power consumption, although these are post-layout simulation results, while the state of the art is for experimental data.

Table I. Comparison of performances at room temperature of LNA state of the art (experimental) and designed LNA (post-layout simulation)

	Technology (μm)	Bandwidth [Ghz]	Center Freq(Ghz)	S11 [dB]	Noise Figure [dB]	Gain [dB]	Pdc(mW)	FoMo
[7]	0.09	7.5	6.85	-14.1	2.92	10.7	21.6	3.9
[8]	0.13	6.8	6.7	-11.5	2.08	16.1	10.2	43.1
[9]	0.13	8	7	-7.5	2.9	10	2.4	30.7
[10]	0.13	10.8	6.7	-10	2.5	7.92	10.68	5
[11]	0.18	11.5	6.75	-10	2.2	14.7	18	16.8
This work*	0.028	2	7	-10.6	3.1	9.3	0.758	75.8

*Simulation results.

6. Temperature effects

Taking as reference the minimal temperature that we can simulate of 233.15 K (-40°C), Table II shows the effect of increasing temperatures in the transistor parameters and the LNA performances. As temperature increases, we see a decrease of the threshold voltage and a degradation of all LNA performances. In FD-SOI technology, the shift of the threshold voltage V_{th} can be compensated via the biasing of the back-gate and this may give a further improvement in LNA performances. Table III shows the result of adapting the back-gate bias voltage of transistors M1/M2 so that either the threshold voltage V_{th} at 233.15 K is obtained at room temperature (first line of the table), or the I_{ds} current at 233.15 K is obtained at room temperature (second line of the table). In both cases, there is no real improvement of the LNA performances. This can be attributed to the fact that g_m/I_D and g_m are also strongly dependent on temperature. We will see experimentally the interest of these tuning knobs at cryogenic temperatures.

Table II. Transistor and LNA parameters as a function of temperature with constant power supply obtained with circuit level simulation

Temperature (°C)	gmoverid	Ids (uA)	Vth (mV)	gm (mS)	S21 @7GHz (dB)	S11@7GHz (dB)	NF@7GHz (dB)	FoMo
-40	28.5	646.2	448.9	18.4	13.8	-13.1	2.0	444.3
-20	26.8	655.4	437.9	17.6	13.3	-12.6	2.3	327
-5	25.7	661.8	429.7	17.0	12.9	-12.2	2.4	279.5
5	24.9	665.7	424.1	16.6	12.7	-11.9	2.5	251.6
20	23.9	671.1	415.7	16.1	12.3	-11.5	2.7	205.5
27	23.5	673.4	411.8	15.8	12.2	-11.3	2.8	190.5

Table III. Transistor and LNA parameters with back-gate voltage adaptation at room temperature obtained with circuit level simulation

Vback-gate (mV)	gmoverid	Ids (uA)	Vth (mV)	gm (mS)	S21 @7GHz (dB)	S11@7GHz (dB)	NF@7GHz (dB)
-620	24.0	637.2	448.9	15.3	12.1	-11.7	2.8
-460	23.9	646.2	439.9	15.4	12.1	-11.7	2.8

7. Conclusions

The derivation of the transistor parameters of a given technology via a LUT and an ACM model help to relate the transistor behavior to its inversion level and facilitate the design without the need of numerous iterations, strongly reducing the time and resources needed to size a LNA amplifier. In this paper, this approach has been illustrated for the design of a CF LNA working at 7 GHz down to 233.15 K, having as key parameters the noise, gain, power consumption and frequency behavior. The design obtained shows a very low power consumption compared to the state of the art. The test chip under fabrication includes five tuning voltages that may help to adapt circuit performances during experimental measurements down to cryogenic temperatures.

Acknowledgements

We thank Raphael Paulin from STMicroelectronics and all colleagues in his team for their help and useful advice related to the technology, and the colleagues in the team at TIMA Laboratory for their help in LNA design.

References

- [1] M. C. Schneider and C. Galup-Montoro, *CMOS Analog Design Using All-Region MOSFET Modeling*, 1er édition. Cambridge University Press, 2010.
- [2] P. G. A. Jespers, *Systematic Design of Analog CMOS Circuits: Using Pre-Computed Lookup Tables*, 1st edition. Cambridge ; New York: Cambridge University Press, 2017.
- [3] J. Liu *et al.*, “A Methodology for the Design of Capacitive Feedback LNAs based on the gm/ID Characteristic,” in *2018 16th IEEE International New Circuits and Systems Conference (NEWCAS)*, Jun. 2018, pp. 178–181. doi: 10.1109/NEWCAS.2018.8585612.
- [4] C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design* | Wiley. Wiley & Sons, 2006.
- [5] Z. Y. Chang and W. Sansen, “Noise optimization of CMOS wideband amplifiers with capacitive sources,” in *IEEE International Symposium on Circuits and Systems*, May 1989, pp. 685–688 vol.1. doi: 10.1109/ISCAS.1989.100443.
- [6] L. Belostotski and S. Jagtap, “Down With Noise: An Introduction to a Low-Noise Amplifier Survey,” *IEEE Solid-State Circuits Mag.*, vol. 12, no. 2, pp. 23–29, 2020, doi: 10.1109/MSSC.2020.2987505.
- [7] H.-K. Chen, Y.-S. Lin, and S.-S. Lu, “Analysis and Design of a 1.6–28-GHz Compact Wideband LNA in 90-nm CMOS Using a π -Match Input Network,” *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 8, pp. 2092–2104, Aug. 2010, doi: 10.1109/TMTT.2010.2052406.
- [8] Y. Li *et al.*, “A Novel Low-Power Notch-Enhanced Active Filter for Ultrawideband Interferer Rejected LNA,” *IEEE Trans. Microw. Theory Tech.*, vol. 69, no. 3, pp. 1684–1697, Mar. 2021, doi: 10.1109/TMTT.2021.3053264.
- [9] H. Zhang, X. Fan, and E. Sá. Sinencio, “A Low-Power, Linearized, Ultra-Wideband LNA Design Technique,” *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 320–330, Feb. 2009, doi: 10.1109/JSSC.2008.2011033.
- [10] J.-H. Lee, C.-C. Chen, H.-Y. Yang, and Y.-S. Lin, “A 2.5-dB NF 3.1–10.6-GHz CMOS UWB LNA with small group-delay-variation,” in *2008 IEEE Radio Frequency Integrated Circuits Symposium*, Jun. 2008, pp. 501–504. doi: 10.1109/RFIC.2008.4561486.
- [11] Y.-S. Lin, C.-C. Wang, G.-L. Lee, and C.-C. Chen, “High-Performance Wideband Low-Noise Amplifier Using Enhanced π -Match Input Network,” *IEEE Microw. Wirel. Compon. Lett.*, vol. 24, no. 3, pp. 200–202, Mar. 2014, doi: 10.1109/LMWC.2013.2293666.