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## Automotive Optoelectronic Components Submitted to Thermal Shock: Impact of Component Architecture on Mechanical Reliability

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### Abstract

New LED technologies & modules allow glare-free automotive lighting. Valeo solutions include the first high-definition LED lighting system. These LEDs technology endure extreme tests conditions in form of thermal shocks or mechanical vibrations to insure reliability under the lifetime of automotive usage. Strict regulations require lead-free solders. Advanced optimization of LEDs for automotive lighting led to multilayered and miniaturized stack-ups. The first lead-free solders were revealed as a weak part of the electronic components and LED assembly. Enormous efforts have been spent on optimizing the lead-free solder material, design and reflow process. However, component miniaturization can also lead to high thermal gradients. Present work analyses the relation between component architectures and thermal shock induced fatigue damage. First, damage after  $N_1$  and  $N_2$  thermal shock cycles was characterized experimentally. Genuine sample preparations by a Cross polisher followed by high-resolution SEM observations reveal void growth in the solder material and cracking in the current circuit Layer. A two-scale finite element model reproduces both damage types. Simulation results can help to provide design improvements on the component architectures and modules to avoid (minimize) both damage types.

**Keywords:** LED, Solders, Damage, SEM Characterization, two scale mechanical model.

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## 1. Introduction

The optimization of Light Emitting Diodes (LEDs) for automotive lighting applications leads to multilayered, miniaturized stack-ups. From a single lighting module, the system features anti-glare technology and a wide beam of light, as well as a turning beam which can detect pedestrians and cyclists on the road and assist drivers with reading road markings.

In service, automotive lighting components undergo thermal cycles (due to changes in the environment) and electric power cycles (on/off) as well as mechanical vibrations on a wider range and longer time than most consumer electronic appliances [3]. The LED components are thus submitted to thermo-mechanical fatigue loading. LED components have to fulfill strict regulations before marketing.

A Light Emitting Diode (LED) is composed of a semiconductor for light emission, a current circuit layer (CCL) for electric current distribution and a substrate. These layers are composed of different materials exhibiting extremely different thermo-mechanical behaviors. Figure 1b illustrates an example of new lighting technologies for Multibeam LED lights [1]. The upper and lower parts of the component are assembled by soldering. This process is called reflow. During this process, the temperature decreases from about 20 °C above solder solidus to room temperature. The maximum reflow temperature is limited due to the possible formation of hard, brittle intermetallic phases [2].

The first product families assembled with lead free solders revealed significant fatigue damage in the solder material. Consequently, solders were considered the weakest components. However, solders are essential for electric current supply as well as thermal and mechanical reliability. Thus, over the last decade, enormous efforts have been spent on optimizing the lead-free solder material. Current lead-free solder dimensions range from several nanometers to several millimeters. Different product families [4] with the same architecture of small solders such as PBGA, WLCLSP, CABGA, achieved market reliability. Two soldering levels may be distinguished for these families. The first level (FLIs) connects LEDs and substrates. The second level (SLIs) interconnects the package and motherboard [5]. In present work, attention will be focused on the first level interconnects. The most used lead-free solder is SnAgCu (SAC). Unfortunately, SnAgCu solders effectively accumulate significant damage during thermal loading. These lead-free materials are more complex than Tin-Lead solder (SnPb). Pradeep et al [3], [6] analyzed different SnAgCu alloys (SAC 105, SAC 305) combined with different surface finishes. To characterize reliability, their boards were subjected to 5000 thermal cycles between -40°C and 125°C. Adding Bismuth (Bi) to SnAgCu solder joint improves the fatigue resistance.

Cavallaro [7] and Borgesen [8] analyzed damage caused by thermal cycles, thermal shock cycles and power cycles. The most damaging sequence starts with thermal cycles [8]. Thermomechanical fatigue damage initiation in common lead-free solders SnAgCu was analyzed extensively in the literature [5],[2],[9-11]. Voids nucleation and growth in the bulk of SnAgCu solders has been reported [12-13]. This explains the recent interest in SnAg-, CuSn- or AuSn-based solders for SnAgCu-replacement [14]. These latter play an outstanding role in heat dissipation thanks to its low thermal resistance [9]. Several solder joints need flux additions during reflow. These additions have been identified to cause void formation [5]. Therefore, solders analysis is required to assure a reliable and robust assembly for future integration in headlamps [15], [12].

Previous analyses focused essentially on the solder material without considering a possible influence of LED architecture. Studies classified AuSn or nanoporous gold NPG, solders as the most reliable ones [1]. Component miniaturization may effectively lead to severe damage in the solders. However, miniaturization causes also unseen problems in the other materials, particularly in the current circuit layer (CCL). The literature overview identified thermal shock cycling as the loading causing the severest damage. Present work focuses on damage due to thermal shock cycles in pixelated LEDs. First, experimental observations based

on advanced sample preparation techniques are presented in sections 2 and 3. Section 4 presents a two scale (complete LED and single pixel) mechanical model. The mechanical model aims at representing damage induced by a single thermal shock cycle. Cooling and heating are modelled independently. Based on this model a new failure criterion for the solder material and the CCL are given. These results allow a new design of the component.

## 2. Materials and Methods

### 2.1. LED Architecture and Materials

The different LED architectures, analyzed in this work, contain several dies (light emitting components) represented in yellow in figure 1a. The latter are connected to the substrate to allow electric current flow and system cooling through interconnect joints. Each pixel contains two pads (PN Junctions) of different geometries. One of them is illustrated in figure 1b. On each pad (N&P), the solder is deposited via a reflow process. Figure 1b shows a schematic representation of a single pixel. Different materials with different thicknesses and temperature dependences are in the stack-up (figure 1b). Table 1 gives the corresponding room temperature properties.

Namazu et al ([16]) determined experimentally Young's modulus at different temperatures. They considered steady-state creep during long time periods (20 hours). In present paper, thermal shock cycles (1 hour) are considered (figure 3). At first order, creep strain is small compared with plastic strain. Hence, the yield stress has been determined from Namazu et al ([16]) as shown in the appendix. In the mechanical models, only one single cycle will be considered. Cooling and heating are modelled independently without creep. This simple approach allows analyzing void growth in the solder material and crack propagation in the current circuit layer (CCL). Figure 2 summarizes the stress strain curves of the solder material and the CCL. The huge differences in Thermal Expansion Coefficients (CTE) of the different materials may lead to significant residual (thermal) stresses during shock cycling and eventually damage the component. Thermal loadings are detailed in the next section. Wong et al [11], [17] analyzed the thermal stresses in a stack-up of materials with different expansion coefficients by an analytical model. A similar approach was presented in [13].

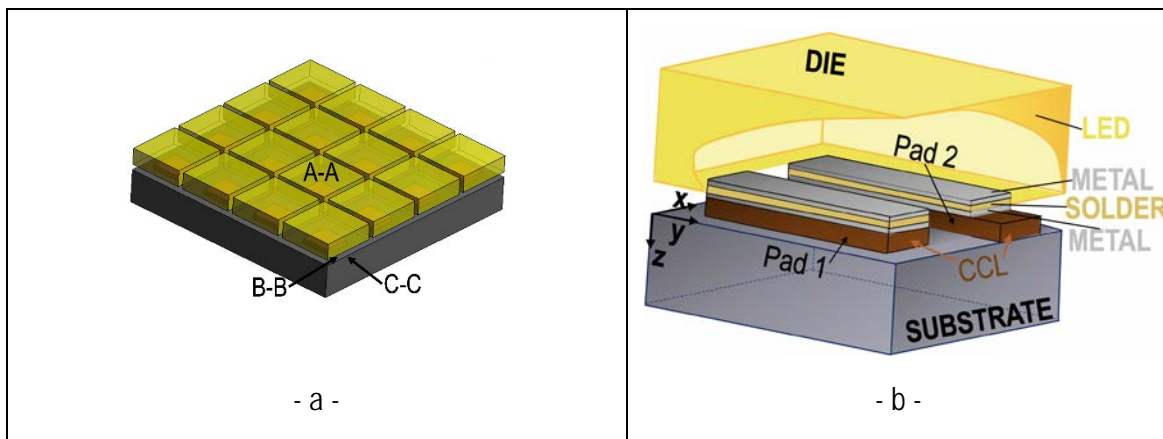


Figure 1: (a) Typical high definition LED (b) detailed view of a single pixel with an example of pad geometry and the different materials.

Part	Material	E(GPa)	$\nu$	CTE (C <sup>-1</sup> )	Behavior
LED		430	0.17	4.4 10 <sup>-6</sup>	Hyperelastic
Solder Joint	M2	E(T°)	0.31	CTE(T°)	Elasto-plastic Multilinear Hardening
	Solder	E(T°)	0.288	16 10 <sup>-6</sup>	Bilinear Hardening
CCL	M1	E(T°)	0.34	CTE(T°)	Multilinear Hardening
Substrate		168	0.28	CTE(T°)	Hyperelastic

Table 1: Materials properties at room temperature. Young's modulus (E), Poisson coefficient ( $\nu$ ), thermal expansion coefficient (CTE).

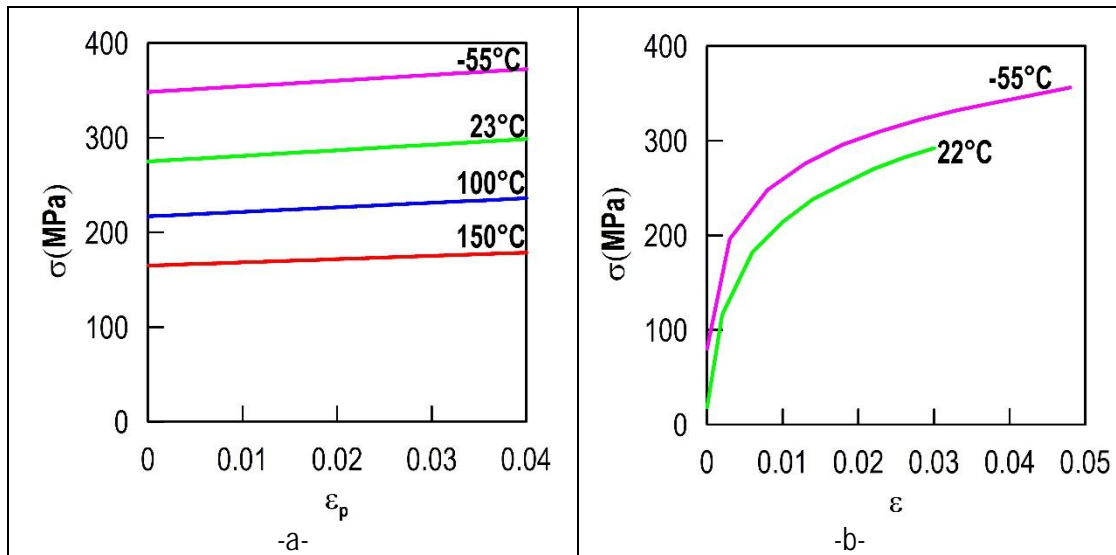


Figure 2: (a) Stress vs. plastic strain of solder material, (b) stress vs. total strain of CCL material [18], with temperature dependence.

## 2.2. Thermal Loadings

In the automotive field, for a product life of 10-15 years, a maximum failure risk smaller than 0.1% is mandatory [4]. Each component has to undergo a series of validation tests (QEC, JEDEC, USCAR, etc.). Present work focuses on thermal shock loadings identified as the most damaging single loading. Following the USCARR33 Standard, the product has to be validated after 1000 Cycles. Shock cycling corresponds to a very sharp temperature increase from  $T_{min}$  to  $T_{max}$  followed by a small holding time (figure 3). Samples were

submitted to  $N_1$  and  $N_2$  thermal shock cycles ( $N_1 < N_2$ ). SEM observations were made after reflow,  $N_1$  and  $N_2$  cycles.

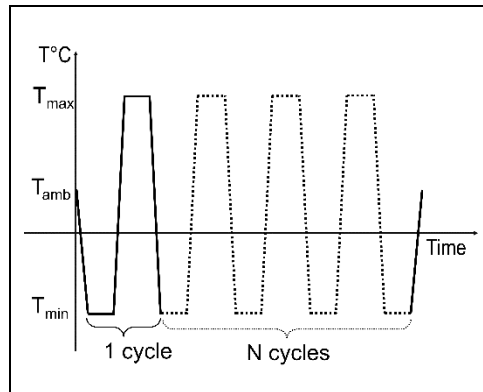


Figure 3: Thermal loadings:  $N$  thermal shock cycles ( $T_{max} > 100^\circ\text{C}$   $T_{min} < -40^\circ\text{C}$ ). Each cycle lasts one hour (30min at  $T_{min}$  and 30min at  $T_{max}$ ).

### 2.3 Sample preparation and SEM observations

Damage was characterized by SEM observations after reflow,  $N_1$  and  $N_2$  thermal shock cycles. For different specimens, damage was observed at the 6 locations depicted in figure 4: (1, 2 & 3) and (1', 2' & 3') on different dies.

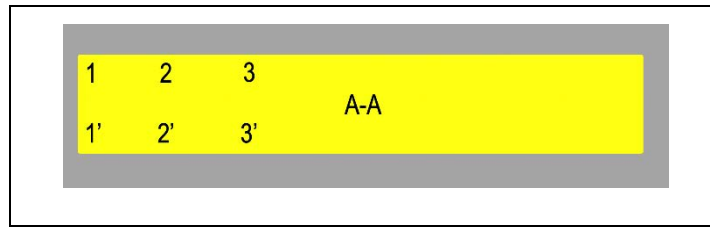


Figure 4: Zones observed in the SEM

In present work, cross sections were prepared by milling with a Jeol Cross Polisher IB-19530CP using an Argon Ion beam. A mask, on top of the sample, reveals only the part to be removed by the Argon beam. All details and parameters used for cross polishing are given in table 2. After polishing with this new facility, samples were ready for SEM observations.

Parameters	Modes	Voltage (kV)	Time (Hours)
Values	Normal (Basic)	6	4-11
	Fine	4	1-2

Table 2: Cross Polisher parameters

Cross polishing led to sections ( $\alpha$ ,  $\beta$ ,  $\gamma$ ,  $\delta$ ) perpendicular to the  $y$  axis. But, no orientation control was done after cross polishing. Figure 5a depicts a single pixel prior to cross-polishing and figure 5c shows the

final result. Both pads were characterized by SEM. A ZEISS SUPRA 55 VP Scanning Electron Microscope, with a large chamber, allowed to set the entire LED with a tilt angle close to  $70^\circ$  (figure 5b) under a voltage of 20kV and with a working distance (WD)", of 17 mm. These conditions (voltage, tilt angle and WD) allowed optimal resolution with both detectors (SE2 for topology and AsB for chemical contrast). Figure 5c shows a single pixel in the tilted position, used for damage characterizations.

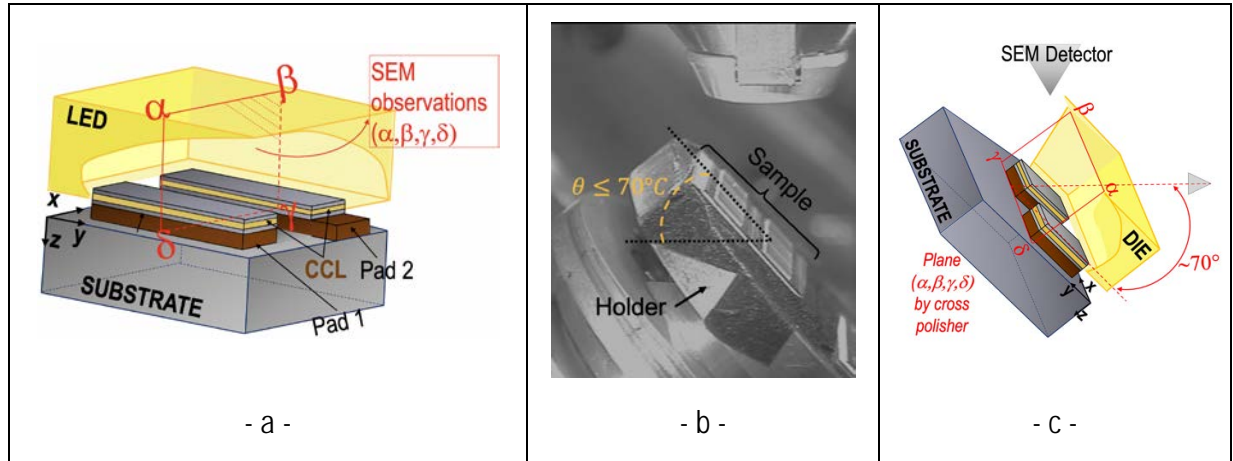


Figure 5: SEM observations of samples. (a) Schematic representation of one pixel with indication of the observed plane ( $\alpha, \beta, \gamma, \delta$ ), (b) Sample position in the SEM-chamber with tilt angle, (c) Single pixel depicted in tilted position with SEM-detector and observed plane

### 3. Experimental results

#### *General damage observation at medium magnification*

Figure 6 shows damage characterizations in zones 1', 2' and 3' respectively at medium magnification after reflow and after  $N_2$  thermal shock cycles. After reflow, (figure 6 left side), the CCL heights differ significantly from one solder to another. The interconnect joint in the middle, in the zone 2', is shorter than in zones 1' and 3'. These observations highlight warpage induced during the reflow. The existence of reflow-induced warpage was checked by optical measurements on the outer Die surfaces [13].

The right-hand side of figure 6 depicts damage after  $N_2$  shock cycles. Significant void formation in the solders may be observed. The CCL exhibits significant cracks "inside" geometric singularities (corners) zones and close to these corners ( $d < w$ ). At this magnification, all regions (1, 2, and 3) seem to exhibit similar damage.

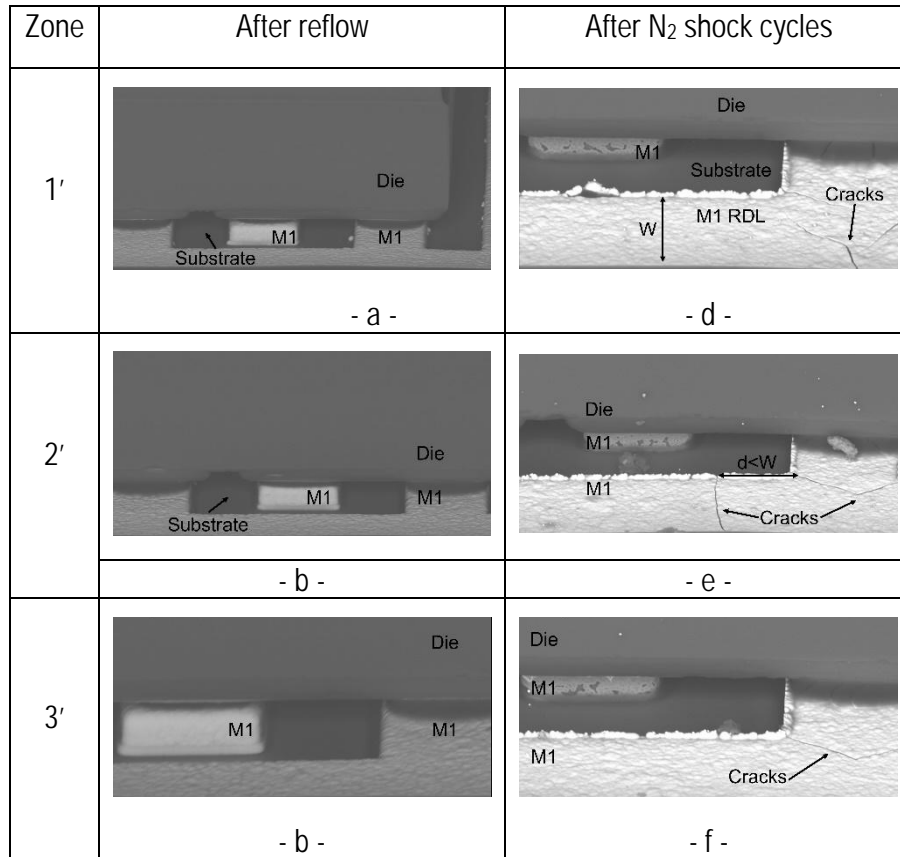


Figure 6: SEM characterizations in zones (1', 2', 3') after reflow (a, b, c) and N<sub>2</sub> thermal shock cycles (d, e, f).

### ***High magnification (resolution) observation of damage***

The two main damage types, void growth and coalescence in the solders and cracking in the CCL were characterized at higher magnification. Figure 7 highlights initial voids (after reflow) and void growth (after N<sub>2</sub> shock cycles) in the solder material. These particular observations correspond to section A-A (figure 4). Similar damage occurred in other locations.

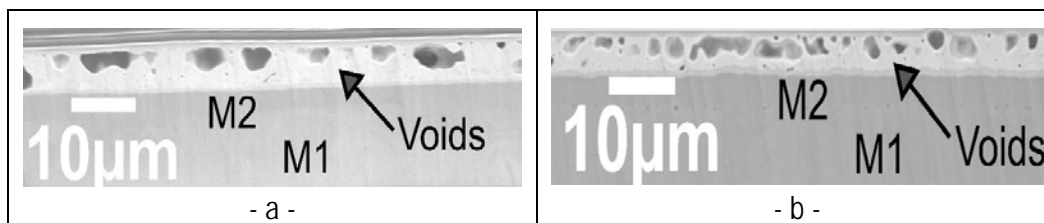


Figure 7: Damage observations in solders at section A-A of the center of the die after reflow (a) and after N<sub>2</sub> thermal shock cycles (b).



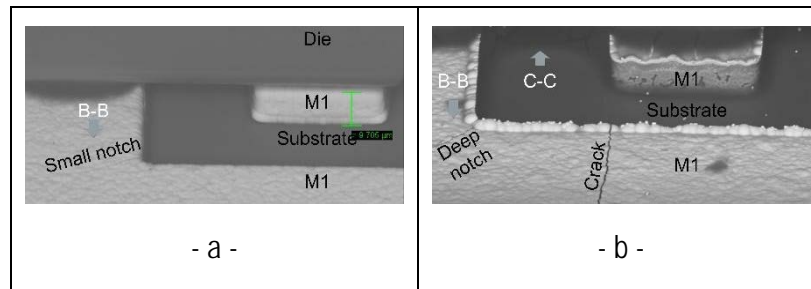


Figure 8: Damage observations in zone 1' after reflow (a) and after N<sub>2</sub> shock cycles (b).

After reflow, no significant damage is observed. After N<sub>2</sub> shock cycles, cracks appear at geometrical discontinuities, i.e. corners (B-B) and at the Substrate/M1 interface (C-C). Figure 8 offers high-resolution observations of the CCL after reflow and after N<sub>2</sub> thermal shock cycles. After reflow, small notch-like lines (B-B) could be observed in inner corner locations of the CCL. The length and depth of these notches were always very small compared to the CCL dimensions.

After N<sub>2</sub> shock cycles, cracks exhibiting a small opening were observed at the same locations. However, through thickness, cracks appeared systematically at a small distance from the CCL corner. The CCL is electrodeposited in present architecture. In present work, the wetting metal did not exhibit severe damage after thermal shock cycles. However, in the CCL material crack nucleation and propagation were observed experimentally. The apparent “brittleness” due to decohesion of electrodeposited layers is known for more than a century. However, to our knowledge, the tendency of crack formation in these layers was not revealed experimentally in microelectronic components. The significant opening of these cracks reveals substantial tensile loading in the CCL. Hence, at first order, crack formation in the CCL material should be controlled by the maximum principal stress. No noteworthy defects were found at the substrate/M1 interface after reflow. However, after thermal shock cycling, interface cracks appear (location C-C in figure 8).

## 4. FEM (Finite Element Method)

### 4.1. Mechanical models

The mechanical model should describe accurately void growth in the solder material and crack formation in the CCL. Two models are used. The global model is represented in figure 9a. This model has to predict the load distribution between the different layers with the smallest possible number of elements. The local (sub-) model (figure 11) simulates one typical solder. The loadings applied to the local model are obtained by the global simulation. Based on the comparison between local model prediction with the experimental data, new damage criteria will be given.

The outer parts of the stack-up, i.e. LED and substrate, constitute a huge thermal mass. All materials of the considered components exhibit high thermal conductivity. The temperature of the latter will always be close to the substrate and LED temperature. Therefore, in both models, homogenous temperature distributions were assumed. Moreover, the plateau of temperature is modelled through a static simulation for both models. Static simulation corresponds to a strong assumption. But, the main damage mechanisms in the solder material (void growth) and CCL (Crack propagation) may be well represented with elasto-plastic solids. Cooling between room temperature and  $T_{\min}$  (<-40°C) and heating between room temperature and  $T_{\max}$  (>100°C) were modelled independently. The substrate and die are modelled as elasto-plastic solids. The

wetting metal (M2), the CCL and solders are modelled as elastoplastic solids with temperature dependent properties.

### Global model

The new architecture is characterized by component miniaturization with a high pad density. A model reproducing the whole component was used to determine the effect of this high pad density. The following major simplifications are applied. First, symmetry with respect to A-A' and B-B' (figure 9a) was used to represent only  $\frac{1}{4}$  of the component. To fix the six DOFs, the displacement in the z-direction was blocked at the intersection of both symmetry planes (figure 9b). With topology sharing, the mesh was a lot easier to apply for a homogenous interface between layers. The component is meshed with SOLID 185 elements. The thickness (z-direction) of each interconnect layer (wetting metal, solder, CCL) was modelled with one single element (figure 10). The pads have 3 elements in the x- and 5 in the y- direction.

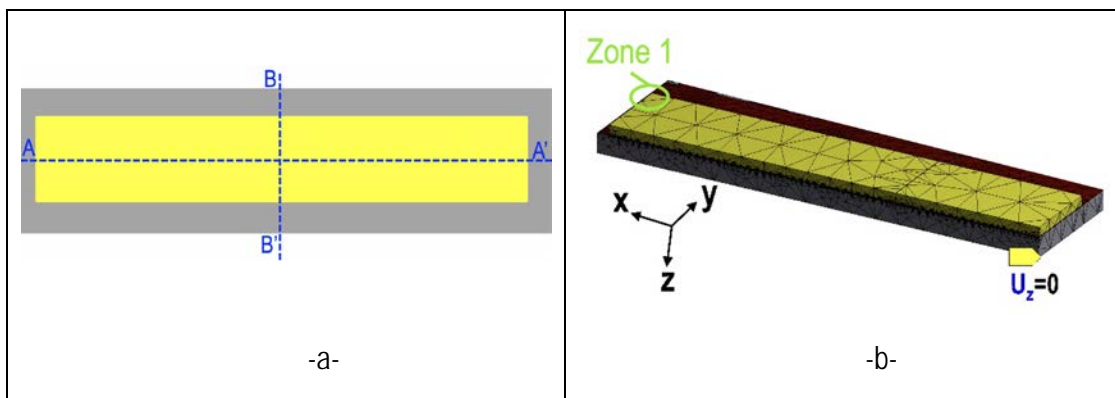


Figure 9: a) Global model before simplifications, b) Mesh of  $\frac{1}{4}$  of the product and boundary conditions.

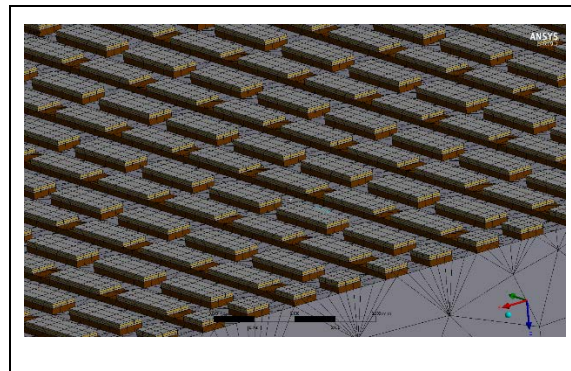


Figure 10: Mesh in interconnect layers in global model

### Local model

Solders identified as critical by the global model are further analyzed in the sub-model, with a refined mesh compared to the global model. First, the global model determines the displacement field around the critical solder. This displacement field constitutes the loading applied in the local model. The local model covers one pixel including a small proportion of the surrounding die and substrate (figure 11a). Only the displacement field imported from the global model (figure 11b) has to be changed when switching from one critical solder to another. Figure 11c details the FE-mesh of the local model.

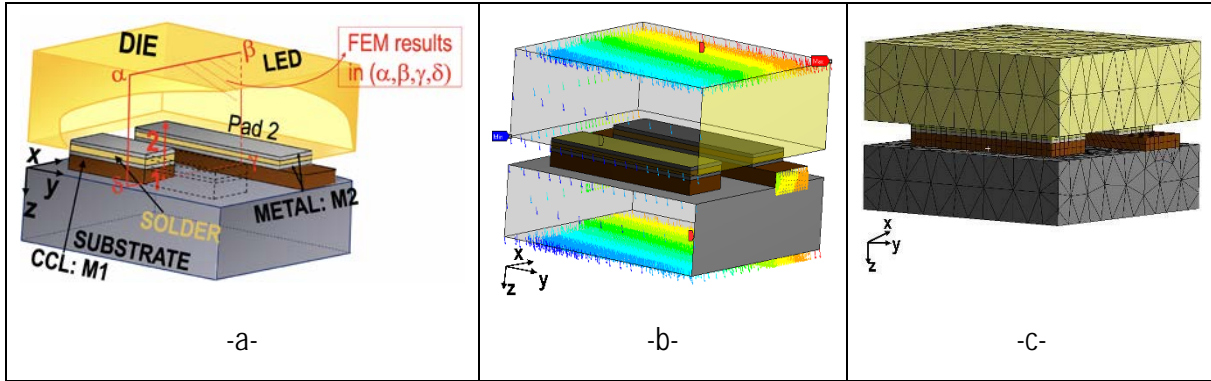


Figure 11: (a) Schematic representation of a single pixel used for the local model (b) Transferring displacements from the global to the local model (c) meshed local model

### Finite element mesh for local and global models

Details on finite element models (mesh type, number of elements and nodes) are given below in table 3 for both models (global, local). Three mesh types (hexahedron, tetrahedron and pyramid) and three element orders (Tet10, Hex20 and Pyr13) were used. The total number of elements in the global and local models correspond respectively to 640158 and 11638.

Model	Mesh type	Element order	Number of elements	Number of nodes	Number of elements
Global	Hexahedron	Hex20	87287	1370390	640158
	Tetrahedron	Tet 10	502920		
	Pyramid	Pyr13	45661		
Local	Hexahedron	Hex20	2828	26946	11638
	Tetrahedron	Tet 10	7854		
	Pyramid	Pyr13	956		

Table 3: Mesh element types and nodes number of global and local models

A structured mesh was used for the interconnect layers. The substrate and die were discretized with an unstructured mesh respecting the topology sharing properties. The latter consists of joining mesh interfaces of different materials. This property is activated when layers have bonded contacts.

For the global model, the number of elements along the width, of the interconnect layers (M2, Solder, CCL) was fixed to 3. The combined condition of an aspect ratio close to unity and a reasonable number of total elements, led to one element along the z-direction (interconnect layer thickness) and five elements along the x-direction (pad length). To insure accuracy of the stress and strain field, a 20 nodes hexahedron element was chosen.

The dies and substrate, modelled with an unstructured mesh, respect interface homogeneity mesh (shared topology). They contain two element types, i.e. tetrahedrons with 10 nodes and Pyramids with 13 nodes. Still, they were adapted to the interface in contact. If the CCL is in contact with wetting layer, the mesh type used adapted to Hexahedron type is Pyramid 13. In other cases, Tet10 is used.

For the local model a similar meshing strategy was used. But the number of elements in the interconnect layers was increased. Table 4 gives the details of the mesh used in the local model. Interconnects were refined compared to the global model. The solder layer contains two elements in the z-direction (along the thickness) with 8 elements in the y-direction (width) and 29 in the x-direction (solder length). The wetting layer and CCL contain the same number of elements along the width and length. But the wetting (M2) layers still contain one element in the z-direction (thickness). Due to the damage observed in CCL and solder layers, the mesh was refined. As defined in global model, sharing topology is also maintained. Moreover, the substrate and the die contain the same element type as defined in global model with more refined mesh, adapted to the refinement used for the interconnects. Finally, both global and local models has quadratic element orders.

Layers	Number of Mesh elements				Element	
	Length	Width	Thickness	Interf.	Type	Order
Dies	Default	Default	5	Shared Topology	Tet10/ Pyr13	Quadratic
Wetting Metal (M2)	29	8	1		Hex20	
Solder	29	8	2		Hex20	
CCL (M1)	29	8	2		Hex20	
Substrate	Default	Default	4		Tet10/ Pyr13	

Table 4: Local model finite element mesh: element types, numbers and discretization orders.

## 4.2. Results

Both models consider temperature dependent CTE and Young's modulus as described above. In order to determine the most damaging sequence between cooling and heating, both sequences were modelled independently.

### *Load transfer and sub-modelling*

First, the load transfer to the local model was checked. The values of all stress components predicted by both models have been compared after cooling from room temperature to  $T_{\min}$ . First, the sub model allows an analysis of stress distribution through all the different layers. Moreover, the stress concentrations at interfaces initially detected in the global model and confirmed in local. The local model gives a continuous stress variation along the thickness of some layers followed by a sharp change in stress at the solder interfaces. The strains in local and global models correspond. This may be expected as the loading in the local model is based on the displacement field of the global model.

### *Stress distribution after cooling and heating*

After validation of the load transfer between the global and local model, the stress evolution along a line in the center of a pad (line 1->2 in figure 11a) was analyzed. At this location, the stress field is not affected by edge effects (border of the pad). First, continuity of the stress vector  $[\sigma_{zz}; \sigma_{xz}; \sigma_{yz}]$  between different layers was checked. Continuity of component  $\sigma_{zz}$  was used to determine the optimal element size.

After mesh validation, the stress distribution was analyzed for both loadings: heating from  $T_{\text{room}}$  to  $T_{\text{max}}$  and cooling from  $T_{\text{room}}$  to  $T_{\text{min}}$ . Figure 12 depicts the normalized von Mises stress after cooling (figure 12a) and after heating (figure 12b). Normalization was done by the real yield strength of each layer. Thus, values above unity indicate yielding and smaller values elastic behavior. The wetting material (M2) exhibits elastic behavior during cooling and heating. The CCL layer (M1) is elastic during cooling and yields during heating. The solder material undergoes extensive yielding after cooling to  $T_{\text{min}}$  but behaves elastically during heating.

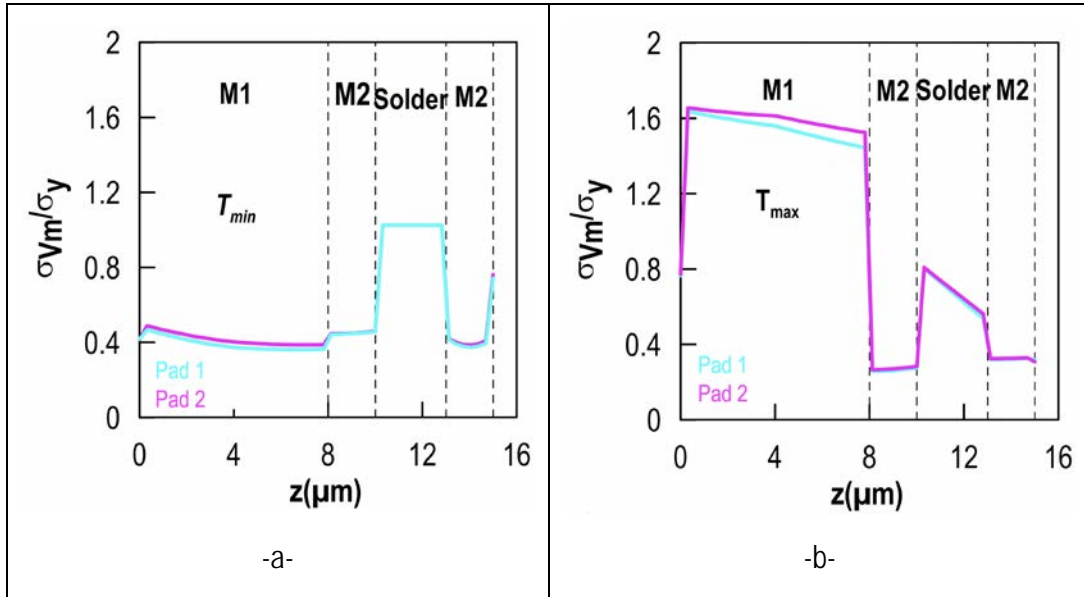


Figure 12: ratio between von Mises and yield limit of each material through interconnect layers at (a)  $T_{\text{min}}$  and (b)  $T_{\text{max}}$ .

Void growth assumes extensive yielding. The solder material is thus essentially damaged during cooling to  $T_{\text{min}}$ . Figure 13 shows the stress field in the pad at  $T_{\text{min}}$ . All the shear components are negligible (figure 13a). In the solder, all components  $\sigma_{xx}$ ,  $\sigma_{yy}$  and  $\sigma_{zz}$  are positive. The solder suffers tensile stresses in all three directions after cooling. Tensile stresses in three directions, characterized by a triaxial state calculation, combined with extensive yielding lead to significant void growth during cooling [19-24]. Components  $\sigma_{xx}$  and  $\sigma_{yy}$  exhibit similar values. The die and substrate prevent the thermal contraction of the solder material and cause these severe tensile stresses. The  $\sigma_{zz}$  is smaller because solder thermal contraction in the  $z$  direction is not completely blocked.

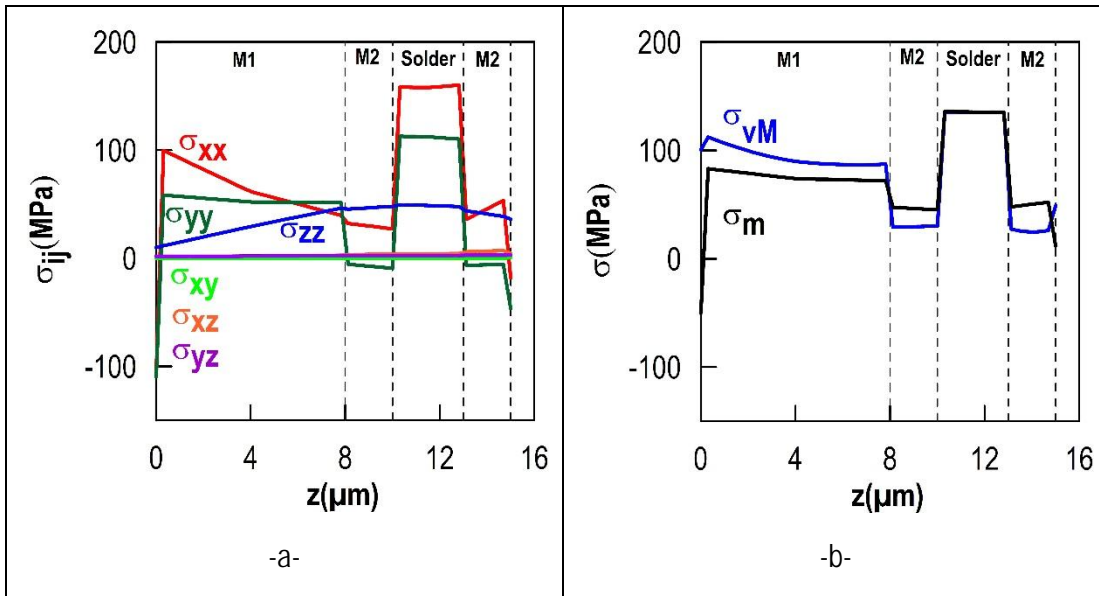


Figure 13: Stress distribution at the center of a pad layers at  $T_{\min}$  (a) the different stress components, (b) von Mises ( $\sigma_{vM}$ ) and mean ( $\sigma_m$ ) stress.

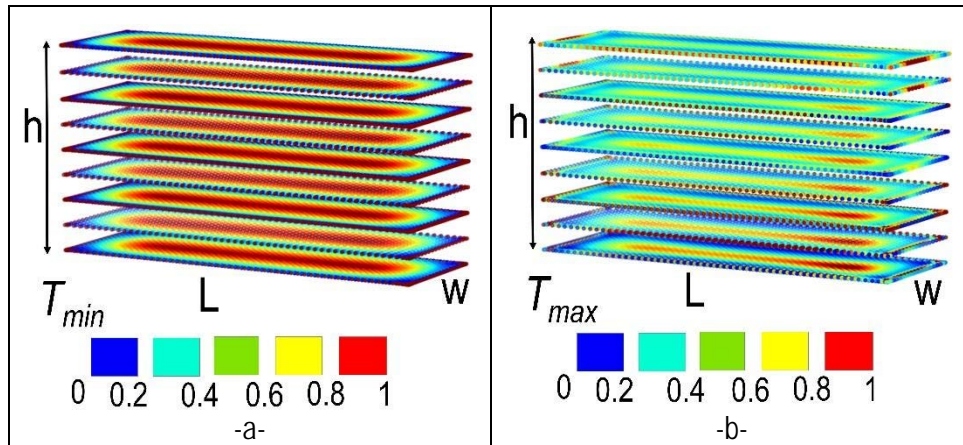


Figure 14: Triaxiality nodes calculation through solder height at (a)  $T_{\min}$  and (b)  $T_{\max}$

During plastic deformation, the void volume increases exponentially in function of the cumulated plastic strain. The coefficient multiplying the plastic strain depends exponentially on the stress triaxiality [25-31]. All stress triaxiality values above 1/3 (uniaxial tension) lead to significant void growth and damage. Figure 14 shows the stress triaxiality distribution in the solder at  $T_{\min}$  and  $T_{\max}$  respectively. At  $T_{\min}$ , the stress triaxiality is close to unity everywhere except from the solder borders where plane stress conditions are met. The thermo-mechanical model shows that the uniform void growth observed experimentally is due to high stress triaxiality ( $T > 1/3$ ) during cooling. The experimental observations and the simulation results already presented, enable us to determine the critical solder locations and the causes leading to CCL cracking.

### ***Critical Solder identification***

The solder material yields during the first thermal shock cycle, as shown in figure 13a. The solders are thus submitted to low fatigue cycle behavior. Solder fatigue is addressed by several models [32]. These models may be divided into five major categories: stress-based, plastic strain-based, creep strain-based, energy-based and damage accumulation based. A detailed description of these categories and related models presented in table 1 in [32]. In present work, comparison of the SEM observations and simulation results clearly shows that solder damage can be simulated based on plastic strain accumulation. Similar criteria were presented in [33-34].

Yielding of the solders is mainly caused by the stress components  $\sigma_{xx}$  and  $\sigma_{yy}$  induced by differential thermal contraction during cooling. Due to their extremely high rigidity, compared to the interconnects, the die and substrate control thermal dilatation or contraction. The solder analysis is based on the values predicted at the center element of each solder (figure 15a in green). The stress components  $\sigma_{xx}$  and  $\sigma_{yy}$  will vanish only at the borders of the dies (figure 15 b, c). As the von Mises and mean stress are due mainly to these components, they will vanish at the same locations. Figure 15d shows the ratio between the calculated von Mises stress and the yield stress. First, all solders except the ones on the border yield during cooling. Only one row of solders at the border of each die is not submitted to yielding. To prevent solders from yielding, they have to be close to a border of the die. Thus, the die dimensions should be decreased tremendously. We suggest die dimensions corresponding to the smallest possible size respecting the stress impact in each direction x and y.

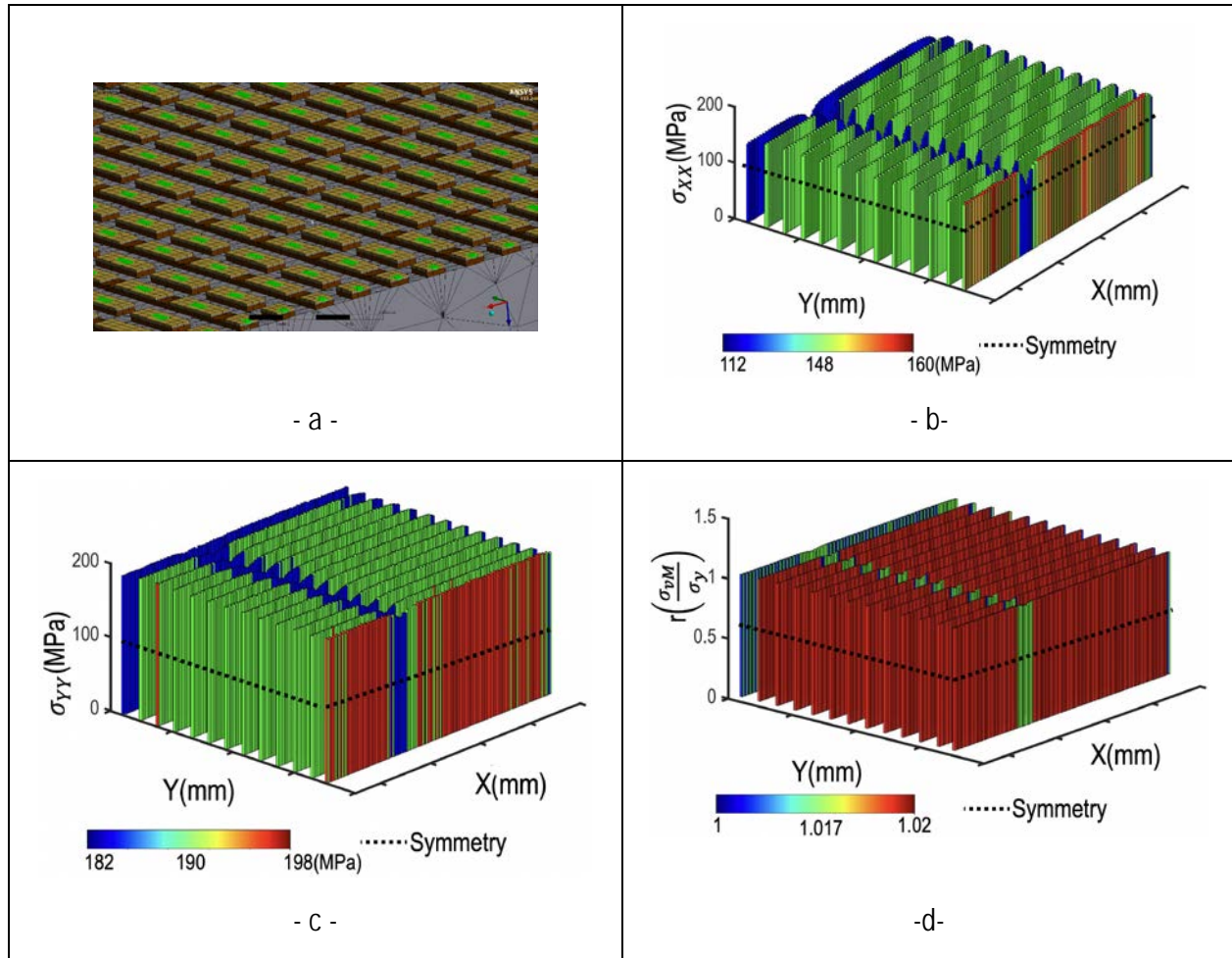


Figure 15: (a) Solders location used for retrieving numerical values, during cooling: (b) stress component  $\sigma_{xx}$  (c) stress component  $\sigma_{yy}$  and (d) von Mises and yield stress ratio.

### *Crack nucleation and propagation in the CCL materials*

No damage was observed after reflow in the CCL. After  $N_2$  thermal shock cycles, cracks have been observed in the corner of the CCL material and close to these corners. During cooling from room temperature to  $T_{min}$ , the CCL is submitted to large tensile stresses (figure 13a). The CCL is electrodeposited and prone to develop cracks under tensile loading. Figure 16 shows the maximum principal stresses predicted by the global model superposed to the SEM observations after  $N_2$  cycles. Clearly, the sharp corners act as stress raisers and cause the crack nucleation and propagation. Cracks A and B could thus be expected. This situation is easily avoided by designing radius on corners of CCL. Crack C at a certain distance from the corner could seem unexpected without the knowledge of the local stress field. Significant principal stresses are observed nearer C. The CCL blocks any degree of freedom in the x direction and the substrate applies heavy tensile stresses to the CCL during cooling. The overall movement will always be controlled by the substrate and the solder on CCL. Preventing tensile stresses at location C implies thus to follow this overall movement with low resistance and decreasing locally the CCL thickness. A similar suggestion was made by Stoney a century ago [35-38].



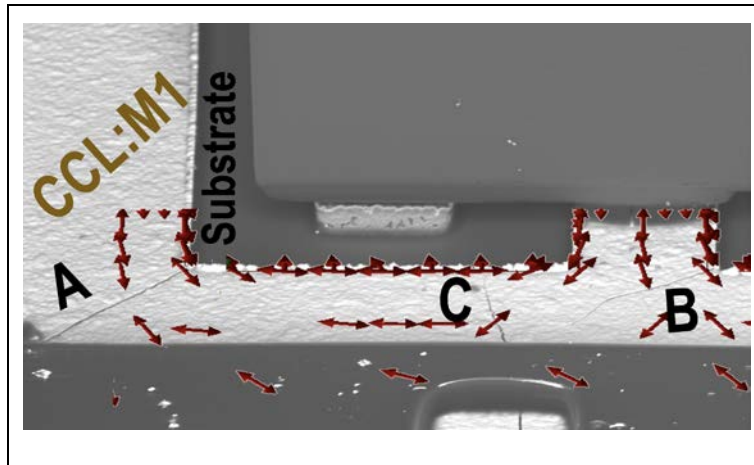


Figure 16: Maximum principal stress through CCL circuit after cooling down to  $T_{min}$ .

## 5. Conclusions

In this paper, damage in optoelectronic components was characterized by SEM observations after reflow and multiple thermal shocks. Damage is initiated after “reflow”. Different damages appear at specific locations in the architecture: Brittle and ductile. Brittle and ductile behaviors were revealed by the SEM observations. Under present conditions, the CCL (material M1) exhibits a “brittle” (prone to crack propagation) behavior. Moreover, the Substrate/M1 interface is also prone to cracking. Only small notches are present after reflow in corner locations of the CCL. After thermal shock cycling, small cracks are observed at the same locations, but much more severe cracks appear at a certain distance from the latter. Moreover, severe interface cracks at the substrate CCL interface were observed. After reflow, small voids were observed in the solder material. During thermal shock cycling, voids were nucleated and showed some growth. Some key conclusions are summarized as follows:

- Damage was characterized by SEM observations. Damage after reflow is limited and does not affect the product reliability. After thermal shock cycles, void growth in the solders, cracking in the CCL and the CCL/substrate interface were observed.
- Two mechanical models were developed. The local model representing a single pixel was used for detailed damage analysis. This model clearly shows solder yielding during cooling. The model identifies the  $\sigma_{xx}$  and  $\sigma_{yy}$  as responsible for yielding.
- The first thermal shock cycle causes the solder to yield. Solder fatigue may be described by cumulated plastic strain.
- The global model clearly shows that limiting the plastic strain in solders implies decreasing the Die dimensions down to a smaller number of PN junctions present between the die and substrate.
- Crack location in the CCL corresponds exactly to the location of the maximum principal stress. To prevent these cracks, avoid corners and decrease the CCL thickness (if possible) close to the solders.

As damage in the solders and the CCL appears essentially during cooling, the steady-state model (without creep deformation) leads to reliable results. The two mechanical models can be used as a validation tool for new LED design. However, further analyzes need modelling multiple thermal shock cycles. Low-cycle solder fatigue modelling [39] needs creep and kinematic hardening experimental data [40-41].

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### Appendix

The variation with temperature of the solder Young's modulus (1) was taken from reference [16]. This equation was used between  $T_{\min}$  and  $T_{\max}$  in present work.

$$E = -0.16T + 100.7 \quad [16] \quad (1)$$

However, no reliable stress strain curves for solder material at the different temperatures could be found in the literature. The solder yield stress was assumed to follow:

$$\sigma_y = 2.10^{-3} * E \quad (2)$$

This reasonable approximation may lead to small errors in the elastic strain irrelevant for plastic strain analysis. The yield stresses predicted by (2) cover the values known at specific temperatures. The solder material and wetting metal were supposed to show similar variations with temperature. The wetting material exhibits linear strain hardening with a known temperature dependence of its tangent modulus ( $E_{\tan}(\text{Metal})$ ). Linear (temperature dependent) strain hardening was considered for solder material:

$$\sigma = \sigma_y + E_{\tan}(\text{solder}) * \varepsilon_{\text{plastic}} \quad (3)$$

Assuming identical ratios between tangent modulus and Young's modulus ( $E_{\tan}/E$ ) for the solder material and the wetting metal, allows to estimate the solder tangent modulus as follows:

$$E_{\tan}(\text{solder}) = \frac{E_{\tan}(\text{Metal}) * E(\text{Solder})}{E(\text{Metal})} \quad (4a)$$