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A Compact 28-nm FD-SOI CMOS 76-81 GHz Automotive Band Receiver Path with Accurate 0.2° Phase Control Resolution

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Abstract — This paper presents a 76-81 GHz receiver path for automotive radar applications in 28-nm FD-SOI CMOS technology. It introduces a new accurate phase control using MOS varactors. The proposed solution implemented in the front-end low noise amplifier (LNA) allows a phase control of maximum 22° with a 0.2° resolution for minimum degradation of the LNA and the receiver performances. The receiver contains a two-stage LNA with 5.5 dB noise figure (NF), a passive mixer, a local oscillator (LO) driver and a baseband (BB) amplifier. The receiver exhibits input compression points (ICP_{1dB}) of -25.2 dBm and -12.6 dBm with and without BB amplifier, respectively. The active area of the receiver path is only 0.057 mm² for a total power consumption of 41.7 mW.

Keywords — automotive, radar, mm-Wave, receiver, phase control, CMOS, varactor, SOI.

I. INTRODUCTION

First embedded automotive radars appeared in the 1970s to reduce road traffic crashes [1]. Automotive radars are a key factor for Advanced Driver Assistance Systems (ADAS) to provide safer driving, whatever the weather and the road conditions. Therefore, robustness, reliability, long range and peripheral covering with high resolution and accuracy are required for automotive radars [2], [3].

The cost reduction and the high level of integrability of nanometer CMOS technology are attractive for automotive radars due to the increasing number of sensors inside vehicles. However, due to wafer's variability in advanced CMOS SOI nodes with Process, Voltage and Temperature variations (PVT) [4], amplitude and phase calibrations are mandatory.

Radar systems determine the range, the speed and the Angle of Arrival (AoA) of a target. The focus of this work is on the accuracy of the AoA determination. The azimuth, or the AoA, of the reflected signal from a target is determined by the phase difference between each receiver chain signal in phased array systems. The intrinsic phase shift difference between receiver chains is a source of inaccuracy. Thus, for an accurate AoA determination, the phase variations must be controlled in the receiver circuit. Analog solutions to calibrate the phase are usually done with phase-shifters, however active phase-shifters are power consuming and passive ones are lossy and require significant area [5]. In addition, it is very complex to achieve an accuracy of less than one degree with phase-shifters at these frequencies [6]. Another method is to use an

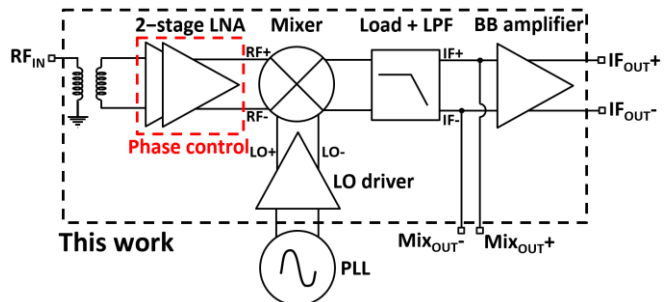


Fig. 1. Receiver block diagram

I/Q architecture but it increases the design complexity and power consumption. Digital solutions using Direction of Arrival (DoA) estimation algorithms such as MUSIC can be very accurate but require high Signal-to-Noise Ratio (SNR > 15 dB) [7]. Furthermore, noise and interferences degrade the accuracy of the DoA estimation: the receiver must be very linear with a low noise contribution.

This paper presents a new accurate phase control technique directly included in the front-end LNA. A compact 76-81 GHz receiver has been achieved using a 28-nm FD-SOI CMOS technology. Section II describes the phase control technique and the receiver architecture, and Section III presents the measurement results. Finally, Section IV concludes this work.

II. RECEIVER ARCHITECTURE

Frequency Modulated Continuous Wave (FMCW) radar principle and Direct Conversion architecture are now commonly used for automotive radar applications. FMCW principle simultaneously provides the range and the speed using Doppler effect in a short computing time. Fig. 1 shows the proposed receiver architecture including a phase control solution embedded inside the LNA. The receiver is composed of a two-stage LNA, an LO driver, a passive mixer with its load also used as a low-pass filter (LPF) and a baseband amplifier (BB). These blocks are described in the following sub-sections.

A. Phase control technique

The front-end blocks are the most susceptible to cause phase variations. Monte Carlo simulations of 2000 trials with mismatch and process variations on the front-end indicate

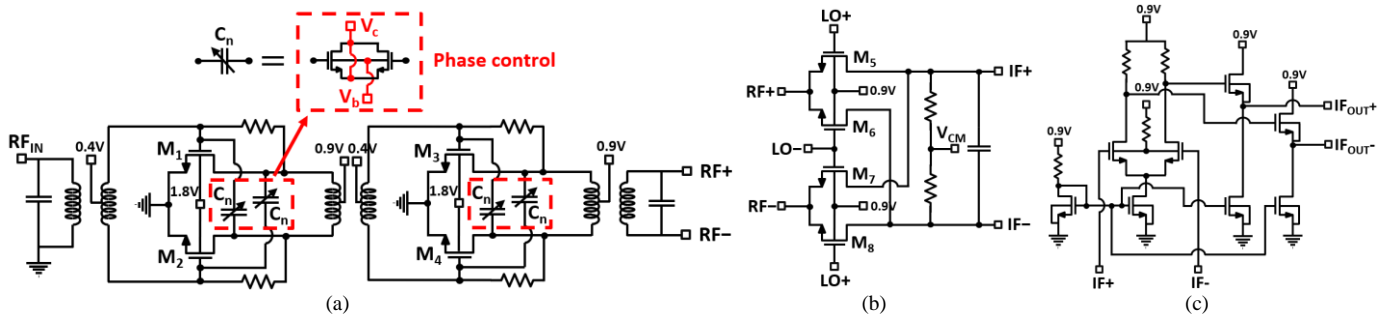


Fig. 2. Schematic of the 2-stage LNA with varactors (a), the passive mixer with its load (b) and the baseband amplifier (c)

phase variations of $\pm 5^\circ$ per amplifier stage. Thus, the proposed solution consists in correcting the phase deviations directly inside the LNA. This technique neither requires a significant silicon area nor power consumption to control the receiver phase variations. The solution includes an LNA with varactors used as variable neutralizing cross-capacitors to tune the phase, shown in Fig. 2 (a). The FD-SOI process allows threshold voltage (V_{th}) modulation through body biasing. Its back-gate access provides each varactor two different voltage controls, which gives both large and fine tuning of its capacitance. Therefore, FD-SOI technology confers a better tuning range than bulk technology.

B. LNA

The topology of the LNA is a differential two-stage common source with capacitive neutralization and resistive feedback, shown in Fig. 2 (a). The differential topology theoretically cancels common mode noise and common mode voltage. Two stages are used as a trade-off between gain and linearity. Both stages are identical to use the same varactors and therefore to have an identical phase tuning at each stage.

To compensate Miller effect and boost the gain, cross-coupling capacitors technique is used. The capacitor C_n in Fig. 2 (a) is a MOS varactor designed to tune the capacitance value used to neutralize the gate-drain capacitance C_{GD} of M_{1-4} transistors and therefore to adjust the phase of the amplifier. The C_{GD} capacitance has a strong impact on the phase. This technique also impacts the gain and the amplifier stability. Varactors offer a non-negligible degree of control on the LNA. Resistive feedback is used to reduce input impedance for the matching and stabilize the amplifier at lower frequencies. The costs of using varactors and resistive feedback are around 1 dB of gain reduction and around 0.8 dB NF degradation.

C. Mixer

The mixer represented in Fig. 2 (b) is a double-balanced passive mixer. The double-balanced topology provides lower losses and better RF-to-IF and LO-to-IF isolations than unbalanced or single-balanced topologies. Passive mixers are very linear and benefit from low on-state resistance of MOS transistors used as switches. Other advantages of passive mixers are the absence of DC current consumption and a reduced flicker noise. The mixer has a simulated ICP_{1dB} of 5 dBm and estimated conversion losses of 4.5 dB from LNA and LNA-Mixer measurement results in Section III. Increasing

M_{5-8} transistors width reduces their on-state resistance but increases parasitic capacitances. The back-gate biasing is used to reduce threshold voltage of the four mixing transistors M_{5-8} , therefore reducing their on-state resistance and improving both linearity and noise performances.

The mixer is loaded by a 100Ω differential resistor to make a trade-off between linearity and voltage conversion gain. Capacitors were added to the resistive load to filter unwanted RF signals, as a low-pass filter. A common mode voltage V_{CM} of 450 mV is applied to supply the following baseband amplifier.

D. LO Driver

The LO driver is used as a buffer for the LO signal. It is the same amplifier topology than the LNA in Fig. 2 (a) but with only one stage and a fixed varactors capacitance value. As the LO signal is sinusoidal, there is a short time where both transistors of the same side of the mixer are ON, which degrades the NF of the mixer. Thus, LO signal must have a large voltage swing to shorten the common ON time. LO signal symmetry is important for NF, ICP_{1dB} and conversion gain performances of the mixer. The input and output baluns of the LO driver are carefully designed to reduce asymmetries.

E. Baseband Amplifier

The baseband amplifier is a classic common source differential amplifier with a source follower stage, shown in Fig. 2 (c). This amplifier is designed for LNA-Mixer testability to compensate for the passive mixer losses and to improve NF measurements. The BB amplifier only consumes 3 mW from a 0.9 V supply voltage.

F. MOS varactors

The varactor C_n inside the LNA in Fig. 2 (a), used to tune the phase, is composed of two NMOS transistors like in [8] with their drain and source nodes connected to a common node arbitrarily named V_c . Their back-gate accesses are also connected to a common node arbitrarily named V_b . Thus, there are two voltage control nodes for a more accurate capacitance tuning and therefore a more accurate phase tuning. The back-gate control node allows a very fine tuning. V_c and V_b voltage control ranges are respectively 0 to 0.9 V and 0 to 1.8 V. The MOS transistors in varactor C_n are matched to the LNA MOS transistors to present the same PVT variations. C_{max} and C_{min} values are carefully chosen to ensure LNA stability and to offer the maximum phase control.

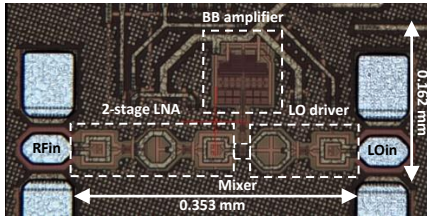


Fig. 3. Die photograph

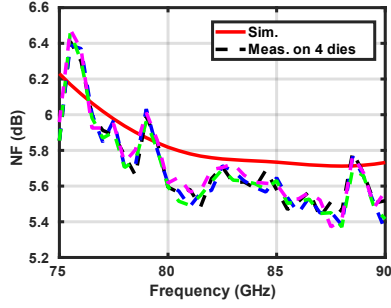


Fig. 4. Measured NF of the receiver front-end LNA versus frequency

III. EXPERIMENTAL RESULTS

The proposed receiver was fabricated in 28-nm FD-SOI CMOS technology from STMicroelectronics. The active area of the receiver depicted in Fig. 3 is only 0.057 mm^2 , including decoupling capacitors.

Measurements were realized at 25°C . The LNA was measured in standalone and the receiver path was measured in two different configurations as illustrated in Fig. 1: LNA-Mixer measurements were done at the outputs of the mixer load, named Mix_{OUT} , and LNA-Mixer-Baseband Amplifier measurements at IF_{OUT} outputs. The receiver measurements were performed at 10 MHz intermediate frequency (IF).

Wafer level measurements in Fig. 4 on the two-stage LNA report 5.5 dB NF at 81 GHz with only 0.9 dB of variation within the 76-81 GHz frequency band. A very good correlation is observed between the simulated NF and the measured NF on four different dies, with 0.2 dB measurement accuracy. Depending on the varactors tuning, measurements of the LNA also exhibit 17.1 dB gain and an input compression point of -11.3 dBm in the 76-81 GHz frequency band. It consumes 29.4 mW from 0.9 V supply voltage and has a 1.8 V back-gate biasing.

The receiver consumes 41.7 mW, including the LO driver and the baseband amplifier. Voltage gain measurements illustrated in Fig. 5 (a) indicates that the LNA-Mixer of the receiver achieves a voltage conversion gain G_C of 12.5 dB at 78.5 GHz and an $\text{ICP}_{1\text{dB}}$ of -12.6 dBm . A good correlation between the simulated and measured conversion gains is observed as well. The 1 dB difference is mainly explained by the measurement accuracy at these frequencies. The LO-to-RF isolation is 39.9 dB and both RF and LO input reflection coefficients are below -14.7 dB in the 76-81 GHz frequency band as illustrated in Fig. 5 (b).

Due to LO jitter and synchronization issues between the IF output signals and a frequency reference, the phase variations have been measured on the LNA in stand-alone, where the phase control is directly implemented, for an accurate phase

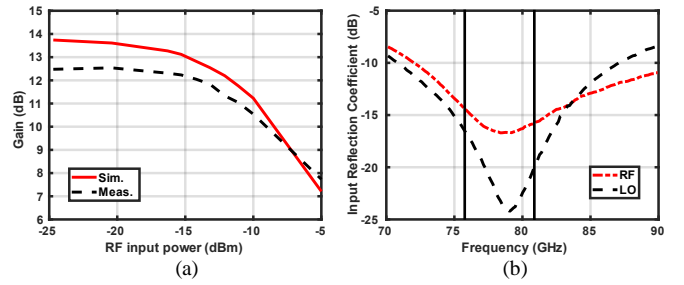


Fig. 5. Measured LNA-Mixer gain versus RF input power at 78.5 GHz (a) and measured RF and LO input reflection coefficients versus frequency (b)

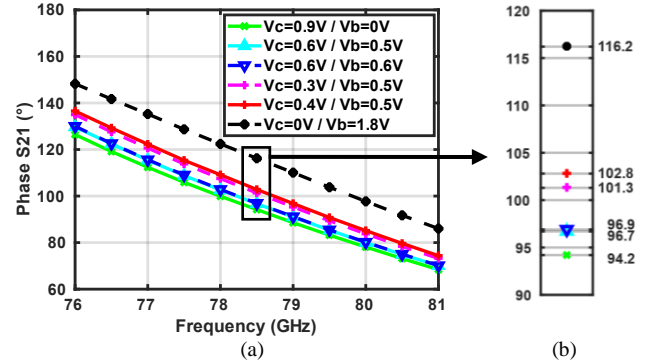


Fig. 6. Measured phase of the receiver front-end LNA with varactors tuning versus frequency (a) and a zoom in at 78.5 GHz (b)

Table 1. Measured performances variations with maximum varactors tuning

	NF (LNA)	$\text{ICP}_{1\text{dB}}$ (LNA)	S_{21} (LNA)	G_C (LNA-Mixer-BB Amp.)	G_C (LNA-Mixer)
Best value	5.5 dB	-11.3 dBm	17.1 dB	24.9 dB	12.7 dB
Variation worst case	0.2 dB	2.5 dB	1.9 dB	0.8 dB	1.1 dB

measurement. Fig. 6 (a) presents the phase variations measurements of the receiver front-end LNA for different voltage controls of the varactors in the 76-81 GHz frequency band. In this band, the maximum range of phase control is 22° (at 78.5 GHz) and the minimum is 17.6° (at 81 GHz). At 78.5 GHz, shown in Fig. 6 (b), the varactor's drain/source node V_c , used for coarse tuning, has a phase control resolution of $1.5^\circ/100 \text{ mV}$ and its back-gate node V_b , used for fine tuning, has a phase control resolution of $-0.2^\circ/100 \text{ mV}$. The $V_c = 0 \text{ V} / V_b = 1.8 \text{ V}$ configuration in Fig. 6 corresponds to the highest capacitance value of the varactor. Measurements on four different dies of the same wafer in the 76-81 GHz band indicate very few variations of the phase control resolution: $\pm 0.2^\circ$ on the coarse tuning and $\pm 0.1^\circ$ on the fine tuning; and few variations of the maximum phase control range: $\pm 1^\circ$.

Table 1 shows that the addition of the varactor offers a tuning element with minimum noise, linearity and gain degradation, for a given frequency between 76 and 81 GHz with an IF of 10 MHz.

The front-end receiver exhibits performances in line with the best-in-class state-of-the-art receivers reported in Table 2. The proposed phase control technique achieves a fine 0.2° phase control resolution while managing a trade-off between linearity, power consumption and occupied area, which are key factors in automotive radar applications.

Table 2. Receiver performances comparison

	This work		RFIC 19 [9]	ISSCC 21 [10]	TMTT 13 [11]	TMTT 21 [12]	JSSC 17 [13]
Technology	28-nm FD-SOI CMOS		40-nm CMOS	45-nm CMOS	65-nm CMOS	28-nm FD-SOI CMOS	130-nm SiGe
Frequency (GHz)	76-81		77-81	76-81	76-77	77	76-81
Integrated RF & analog blocks	2-stage LNA, passive mixer, LO driver	2-stage LNA, passive mixer, LO driver, BB amplifier	3-stage LNA, mixer, 4-stage VGA, LDO, PLL	2-stage LNA, passive I/Q mixer, VGA	5 stage LNA, sub-harmonic mixer, passive mixer	Mixer, VGA, LPF	Mixer, BB multiplexer, IF buffer
ICP_{1dB} (dBm)	-12.6	-25.2	-22.3 (VGA off)	-10	-15 ⁵	-23.5	>1
NF_{DSB} (dB)	6.1 (sim.), 5.5 (LNA)	6.5 (sim.), 5.5 (LNA)	7.3 (at 77 GHz LO), 6 (at 81 GHz LO)	10.8 ⁴	10	8.2	7-8
G_C (dB)	12.5	24.9	30.8	N.A.	16	33	15
Phase control / resolution (°)	22 max. / 0.2 ¹ (at 78.5 GHz)	22 max. / 0.2 ¹ (at 78.5 GHz)	N.A.	N.A.	N.A.	N.A.	N.A.
Power (mW)	38.7, 29.4 ²	41.7, 29.4 ²	143 ³	3500	28.2 ⁶	27 ⁷	1800 (1TX/6RX)
Supply (V)	0.9, 1.8 (body biasing)		1.1 (RF), 1.8 (BB)	1/1.2/1.8	1.2	1	3.3
Active area (mm²)	0.046	0.057	0.8	22 (analog area)	2.3 (with pads)	0.96	12.7 (2TX/6RX)
Notes	¹ LNA measurements ² Without LO driver		Packaged die, ³ LNA, mixer, BB amplifier	4RX/3TX chip, ⁴ Supposed DSB	⁵ LNA only ⁶ Without LO blocks	⁷ Without LO buffer	Wafer level measurements, 2TX/6RX chip

IV. CONCLUSION

A compact 28-nm FD-SOI CMOS receiver path for 76-81 GHz automotive radar applications was presented. A new compact analog phase control solution has been implemented in the receiver through the LNA using MOS varactors as variable neotrodyne capacitors. This solution exhibits a 22° phase control range and a resolution accuracy of 0.2° at 78.5 GHz, which compensates for phase variations from mismatch and process variations, simulated at ± 5° per amplifier stage. Phase measurements over four dies indicate a good reproducibility of this solution. The receiver front-end LNA achieves a minimum 5.5 dB NF at 81 GHz. NF measurements among different dies also point out the design robustness. The receiver path presents a 24.9 dB voltage conversion gain G_C with -25.2 dBm ICP_{1dB}, a power consumption of 41.7 mW and an active area of only 0.057 mm². The receiver path without the baseband amplifier (LNA-Mixer only) presents a 12.5 dB voltage conversion gain G_C with -12.6 dBm ICP_{1dB}, a power consumption of 38.7 mW and an active area of 0.046 mm². The demonstrated receiver path shows state-of-the-art performances and includes an accurate phase control solution. This contributes to the reduction of both analog area and power consumption for a precise angle of arrival determination. Indeed, a major part of the phase control is done with compact varactors in the front-end of the receiver. The proposed solution guarantees dies alignment in post-production and therefore improves the production yield of radars circuits.

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REFERENCES

- [1] H. H. Meinel, "Evolving Automotive Radar - from the very beginnings into the future", *IEEE European Conference on Antennas and Propagation*, 2014.
- [2] K. M. Strohm et al., "Development of Future Short Range Radar Technology", *IEEE European Radar Conference*, 2005.
- [3] M. Murad et al., "Requirements for next generation automotive radars", *IEEE Radar Conference*, 2013.
- [4] E. G. Ioannidis et al., "Statistical analysis of dynamic variability in 28nm FD-SOI MOSFETs", *44th European Solid State Device Research Conference*, 2014, pp. 214-217.
- [5] S. Y. Kim and G. M. Rebeiz, "A 4-Bit Passive Phase-Shifter for Automotive Radar Application in 0.13 μm CMOS", *IEEE Compound Semiconductor IC Symposium*, Oct. 2009, pp. 1-4.
- [6] D. Pepe and D. Zito, "A 78.8–92.8 GHz 4-bit 0–360° active phase shifter in 28nm FDSOI CMOS with 2.3 dB average peak gain", *European Solid-State Circuits Conference*, 2015, pp. 64-67.
- [7] H. Fu et al., "A Robust Phase-Ambiguity-Immune DOA Estimation Scheme for Antenna Array", *IEEE International Conference on Communication Systems*, 2018, pp. 30-34.
- [8] C. Zhang and M. Otto, "A wide range 60 GHz VCO using back-gate controlled varactor in 22 nm FDSOI technology", *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference*, 2017, pp. 1-3.
- [9] T. Murakami et al., "A 9 dB Noise Figure Fully Integrated 79 GHz Automotive Radar Receiver in 40 nm CMOS Technology", *IEEE Radio Frequency Integrated Circuits Symposium*, 2019.
- [10] K. Dandu et al., "High-Performance and Small Form-Factor mm-Wave CMOS Radars for Automotive and Industrial Sensing in 76-to-81GHz and 57-to-64GHz Bands", *IEEE International Solid-State Circuits Conference*, 2021.
- [11] V.-H. Le et al., "A CMOS 77 GHz Radar Receiver Front-end", *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 10, pp. 3783-3793, Oct. 2013.
- [12] G. Papotto et al., "A 27-mW W-Band Radar Receiver With Effective TX Leakage Suppression in 28-nm FD-SOI CMOS", *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 9, pp. 4132-4141, Sept. 2021.
- [13] T. Fujibayashi et al., "A 76- to 81-GHz Multi Channel Radar Transceiver", *IEEE Journal of Solid-State Circuits*, vol. 52, pp. 2226-2241, Sept. 2017.