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i-InGaAs

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# Remote Doping of Scalable Nanowire Branches

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**ABSTRACT:** Selective-area epitaxy provides a path toward high crystal quality, scalable, complex nanowire networks. These highquality networks could be used in topological quantum computing as well as in ultrafast photodetection schemes. Control of the carrier density and mean free path in these devices is key for all of these applications. Factors that affect the mean free path include scattering by surfaces, donors, defects, and impurities. Here, we demonstrate how to reduce donor scattering in InGaAs nanowire networks by adopting a remote-doping strategy. Low-temperature magnetotransport measurements indicate weak anti-localization—a signature of strong spin-orbit interaction—across a nanowire Y-

junction. This work serves as a blueprint for achieving remotely doped, ultraclean, and scalable nanowire networks for quantum technologies.

KEYWORDS: InGaAs, nanowires, selective-area epitaxy, weak anti-localization, spin-orbit interaction

#### INTRODUCTION

In the last two decades, semiconductor nanowires (NWs)<sup>1</sup> have opened multiple new perspectives in a wide variety of applications including photovoltaics, <sup>2-6</sup> photodetectors, <sup>7-10</sup> lasers, <sup>11-15</sup> single-photon emitters, <sup>16,17</sup> photoelectrochemistry,<sup>18</sup> nanoscale electronics,<sup>19</sup> and research into topological quantum computing.<sup>20–24</sup> While most NW fabrication approaches result in free-standing structures, selective-area epitaxy (SAE) has recently been revived for the fabrication of horizontal NW assemblies that can be directly contacted on a wafer. 25,26 SAE has thus been used to obtain lateral III-V NWs, with high NW crystal quality and with scalability unmatched by any other bottom-up NW growth method. The ability of SAE NWs to be grown into NW networks,<sup>27</sup> and the relative ease with which they can be further processed directly on the original substrate, makes them extremely attractive for use in experiments exploring topological quantum transport physics. <sup>28-32</sup>

It has generally been reported that surface scattering in NWs reduces carrier mean free paths which, by extension, also reduces carrier mobility with respect to their bulk counterparts. This is especially pertinent in InAs NWs, where the surface Fermi level pinning results in most of the conduction occurring at the surface.<sup>33</sup> Room-temperature electrically measured mobilities for undoped, vertically grown InAs NWs thus fall in the range of  $\sim 20-3000 \text{ cm}^2/(\text{V s})$ . Noncontact measurement techniques such as THz pump-probe spectroscopy report slightly higher mobilities of ~4000-6000 cm<sup>2</sup>/

(V s) due to the smaller length scale of the assessment and a possible selection bias (higher mobility sections contributing more to the signal). Still, mobilities remain significantly lower than the reported values for thin films of around 30000 cm<sup>2</sup>/(V s).<sup>41</sup> InGaAs nanowires with In:Ga ratios around 50%, on the other hand, have been reported with somewhat lower mobilities ranging from  $\sim$ 500 to 1500 cm<sup>2</sup>/(V s).<sup>42,43</sup>

Over the years, modulation doping has proven to be a staple technique to many applications employing high-performance semiconductor heterostructures. This technique allows for the creation of two-dimensional electron gases (2DEGs) with high carrier concentration combined with extremely high mobilities. From groundbreaking scientific discoveries such as the integer and fractional quantum Hall effects, 44-46 and enabling novel concepts such as topological qubits 47-50 to high-power applications using high electron mobility transistors (HEMTs), 51,52 a wide range of fields have benefited and are continuing to benefit from remotely doped 2DEG heterostructure schemes. With current knowledge and modern epitaxy techniques, state-of-the-art 2DEG devices can achieve mobilities regularly exceeding 10<sup>7</sup> cm<sup>2</sup>/(V s).<sup>53,54</sup> Similarly to

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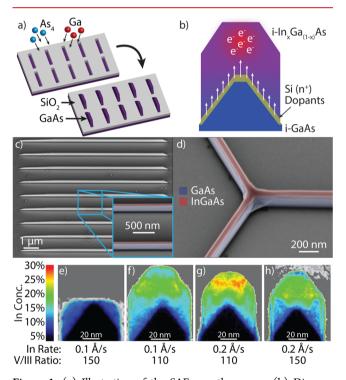


bulk, direct doping of NWs reduces carrier mobilities due to ionized dopant scattering. To circumvent this carrier scattering mechanism, vertically grown free-standing GaAs NWs with a remote-doping design exhibit both high carrier densities and high mobility.  $^{35-58}$ 

In this work, we demonstrate the growth of quasi-1D InGaAs NW heterostructures hosting coherent transport by combining remote doping with SAE. The InGaAs NWs are obtained on a GaAs nanomembrane (NM) buffer in which the doping is located. The band alignment naturally results in the localization of electrons in the region with higher indium content (and lower bandgap). Improved electrical transport is demonstrated by low-temperature field-effect and magneto-transport measurements across InGaAs NW Y-branches, demonstrating high-quality NW junctions. This research thus lays the groundwork for future exploitation of remote-doping schemes in scalable NW networks, including materials beyond InGaAs.

# **■** GROWTH

Remotely doped InGaAs NWs were grown on top of GaAs NM buffers using a SAE approach, as depicted in Figure 1a. A



**Figure 1.** (a) Illustration of the SAE growth process. (b) Diagram showing the desired doping profile for remotely doped InGaAs NWs on GaAs NMs. (c) Tilted SEM image of an array of NWs after MBE growth. (d) Close-up tilted SEM image of a Y-junction showing uniform coalescence of InGaAs NWs. (e—h) Elemental maps of In concentration taken with STEM EDS on NW cross sections showing the dependence of growth conditions on NW composition.

GaAs (111)B substrate was covered by a SiO<sub>2</sub> mask to achieve high growth selectivity. The SiO<sub>2</sub> mask was then patterned with stripes along the three equivalent  $\langle 1\ 1\ \overline{2}\rangle$  directions on the substrate using e-beam lithography and reactive ion etching. The resist was stripped with an O<sub>2</sub> plasma, and the substrate was etched in a dilute buffered HF solution before being loaded into the molecular beam epitaxy (MBE) cluster for growth to ensure an ultraclean surface.

Figure 1b corresponds to the general scheme of the structures in this work. Silicon dopants are introduced at a distance from the InGaAs channel. We expect carriers to localize into the lower-bandgap NW region. As a result, the NWs benefit from an increased carrier concentration thanks to the extrinsic dopants, while ionized impurity scattering is limited due to the physical separation between the doped and transport regions.

Figure 1c shows a representative scanning electron microscopy (SEM) image of the remotely doped NW structures. We recognize a high degree of uniformity in both the buffer NMs and the NWs. Similarly, as shown in Figure 1d, Y-branched structures result from the merging of NWs growing in three equivalent directions.<sup>27</sup> These branched structures exhibit a high degree of NW uniformity, which is further confirmed by X-ray fluorescence (XRF) measurements performed at the ID16B beamline of the European Synchrotron Radiation Facility (ESRF) shown in the Supporting Information.

In-Ga intermixing is commonly observed at the interface between InAs and GaAs. 59 This is also the case for InAs grown on GaAs buffer NMs. In a previous study, we demonstrated InGaAs NWs with a relatively low In content.<sup>27</sup> Increasing the In content is key to enhancing spin—orbit interaction (SOI). In this context, we explored different growth conditions to increase the In concentration. In particular, we varied temperature along with In and As<sub>4</sub> fluxes. We present four representative samples with a variation in the In deposition rate and As<sub>4</sub> beam equivalent pressure (BEP). The composition was analyzed by performing elemental maps by scanning transmission electron microscopy (STEM) energy dispersive X-ray spectroscopy (EDS) on prepared cross sections. The resulting In concentration maps are shown in Figure 1e-h. Here, the atomic concentration of In is calculated as  $C_{In}/(C_{In} + C_{Ga} + C_{As})$  with the maximum possible concentration being 50% for pure InAs. In Figure 1e, we see that an In rate of 0.1 Å/s and V/III ratio of 150 yields a selfterminating growth and a flat (111) top facet with an In concentration of ~10% at the two upper corners of the structure. Decreasing the V/III ratio to 110, as shown in Figure 1f, results in a more pointed structure that does not selfterminate. This results in a larger amount of material being deposited and a maximum In concentration of ~20%. Doubling the In deposition rate to 0.2 Å/s (while halving the growth time to keep the total deposited volume constant) gives a similarly shaped structure; however, now the peak In concentration is ~25%, as shown in Figure 1g. Finally, Figure 1h shows the result of also increasing the V/III ratio to 150 with an In deposition rate of 0.2 Å/s. We observe a structure very similar to Figure 1f with a pointed shape and maximum In concentration of 20%.

We, therefore, observe that a higher In flux yields an increased In concentration in the NW, up to about 25%. On the other hand, at low In rates, In concentrations of only 10% or less are observed. The InAs growth temperatures are relatively low for solid-phase diffusion which is typically only observed above  $750\,^{\circ}\text{C}.^{60-62}$  The In–Ga intermixing could instead be mediated by surface adatom diffusion during growth. This is a thermodynamically driven effect which, consequently, can be suppressed at higher deposition rates where the system approaches a kinetic regime.  $^{63}$ 

Also, the V/III ratio is known to affect the atomic surface reconstruction which in turn affects facet-dependent growth

rates and the resulting shape. 64,65 In Figure 1e, at high V/III ratios and low growth rates, InGaAs grows to form a flat (111) B top facet, after which NW growth stops. This suggests that desorption of In species from this flat top facet is higher than the incoming flux. However, if the In rate is increased, as in Figure 1h, then NW growth is re-established which can be explained by the fact that the increased incoming flux becomes greater than the desorbing flux, thus continuing NW growth. Similarly, if the V/III ratio is decreased, as in Figure 1f, a similar effect is achieved. This, therefore, suggests that, at the higher V/III ratio, the abundance of As atoms also plays a role in inhibiting growth on the (111)B top facet. Thus, higher In rates and lower V/III ratios should be pursued to reduce Ga intermixing in the NW. This result is at least partially supported by recent reports on (100) GaAs substrates where very low V/III ratios are used to grow pure InAs NWs on top of GaAs(Sb) buffers.<sup>28</sup>

The highest In concentration was about 25% absolute, corresponding to  $In_{0.5}Ga_{0.5}As$ . This sample was obtained with a high In flux and lower V/III ratio. These conditions were kept for the rest of the structures presented in this study.

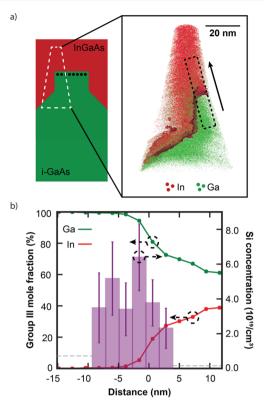
#### ATOM-PROBE TOMOGRAPHY

As the silicon dopant concentration was well below the detection limits of STEM EDS, atom probe tomography (APT) was used as a technique to image the three-dimensional distribution of the dopants in the structure.

APT was used to analyze the distribution of the dopants in the nanowire heterostructures, as shown in Figure 2.27,66 Samples were prepared by lift-out and annular milling using a focused ion beam to isolate the nanowire region for analysis. 67,68 Details of the specimen preparation and APT analysis conditions can be found in the Experimental Section. Figure 2a shows the APT reconstruction of the region indicated by the dashed white line in the schematic. Silicon dopants were mostly detected on the GaAs top facet, as shown in Figure S8. The analysis here focuses on the subregion indicated in the dashed black line. To accurately measure the Si dopant distribution despite this artifact, a proximity histogram<sup>69</sup> was generated, as shown in Figure 2b on either side of a 16% In mole fraction isosurface. The Si concentration peaks below the NM-NW interface, as expected from the doping scheme. APT analysis of two additional heterostructures (see the Supporting Information) found a similar distribution of Si concentrated at the NM-NW boundary. Moving 5-10 nm away from the interface, Si was not detected above the noise level (see Figure S8). The upper bounds on the Si concentration in the upper and lower regions away from the interface are  $2 \times 10^{18}$  and  $7 \times 10^{18}$  cm<sup>-3</sup>, respectively, as indicated by dashed lines in Figure 2b. These measurements demonstrate that Si was incorporated at a distance from the InGaAs transport channel, validating the remote doping from the compositional mapping point of view.

# MAGNETOTRANSPORT

NW structures were electrically contacted for four-point measurements on all three arms of the Y-junctions (see the Experimental Section). A top gate was fabricated by first covering the junction with a 40 nm thick HfO<sub>2</sub> gate oxide by atomic layer deposition (ALD) followed by metal evaporation. An SEM image of an electrical device illustrating the overall design is displayed in Figure 3a. A false-colored cross-sectional



**Figure 2.** (a) APT reconstruction of an InGaAs NW on a GaAs NM. The white dashed line in the schematic indicates the region analyzed by APT. Ga and In atoms are shown in green and red, respectively. As atoms are omitted for clarity. The NM—NW boundary is rendered with an isoconcentration surface of 5% In mole fraction. (b) Proximity histogram across the NM—NW interface showing the Si dopant distribution. Gray dashed lines show the upper bounds on Si concentration in regions away from the interface, where Si counts were not above the noise level. The isoconcentration surface of 16% In mole fraction is at 0 nm as a reference.

focused ion beam (FIB) STEM image is displayed in Figure 3b with the identification of the different layers of the device. It is important to note that the metallic contact layers are continuous through the whole high-aspect-ratio structure, as a result of the dual-angle evaporation.

The samples were then cooled down and electrically characterized at cryogenic temperature. The conductance as a function of top gate voltage  $V_{\rm g}$  is shown in Figure 3c in units of  $e^2/h$ , giving very similar results over all pairs of arms of the Y-junctions. From this measurement, the field-effect mobility is extracted using  $^{70}$ 

$$G(V_{\rm g}) = \left(R_{\rm s} + \frac{L^2}{\mu C(V_{\rm g} - V_{\rm th})}\right)^{-1} \tag{1}$$

with L=600 nm being the length of the channel,  $\epsilon_0=8.854\times 10^{12}~{\rm F/m}$ ,  $\epsilon_{{\rm HfO}_2}=6.5$ ,  $^{28}$  and C the gate capacitance. The contact resistance  $R_{\rm s}$ , the conductance threshold voltage  $V_{\rm th}$ , and the mobility  $\mu$  are the fit parameters. The gate capacitance was estimated numerically using a finite element simulation in COMSOL, though similar values were calculated analytically using coaxial cable or parallel plate capacitor models. The contribution of the GaAs NM to the electrical transport is negligible, as already previously demonstrated.  $^{27}$ 

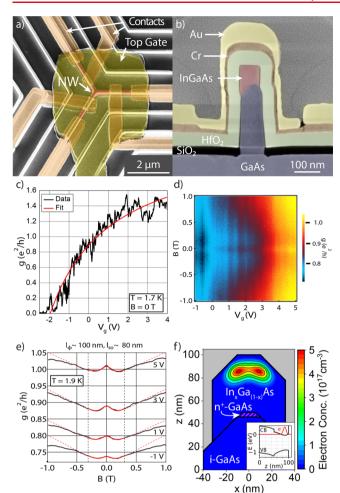


Figure 3. (a) False-colored SEM image of a fabricated electrical device showing three pairs of contacts to enable four-point measurements and a global top gate. (b) False-colored cross-sectional STEM high-angle annular dark-field (HAADF) image showing the layers in a fabricated electrical device. (c) Differential conductance as a function of top gate voltage  $V_{\rm g}$ , from which the field-effect mobility  $\mu$  = ~480 ± 50 cm<sup>2</sup>/(V s), the conduction threshold  $V_{\rm th}$  = -1.9 ± 0.2 V, and the contact resistance  $R_s = 12.2 \pm 0.6 \text{ k}\Omega$  were extracted. (d) Differential conductance plot (color scale) as a function of magnetic field perpendicular to the substrate and top gate voltage with  $V_{
m gAC}$  = 200 mV (peak-to-peak) oscillation added. (e) Magnetoconductance cuts (black) with fits (red) as labeled, exhibiting clear WAL. The WAL model is valid between the dashed vertical lines, which also denote the fitting range (solid red). Theory curves are extended to the full B-range (dashed red). Over the full gate range, average values of  $l_{th}$ = 100  $\pm$  20 nm and  $l_{\rm so}$  = 80  $\pm$  20 nm, where the mean free path  $l_{\rm e}$  = 20 nm was held fixed here. (f) Finite element simulation in nextnano of remotely doped structure obtained from APT measurements showing an electron distribution in the InGaAs NW which is spatially separated from the n-type silicon dopants and disordered GaAs/ InGaAs interface. Inset: band structure cut along x = 0 nm with electron concentration overlaid in red.

We extract a field-effect mobility  $\mu$  of ~480  $\pm$  50 cm²/(V s). At zero gate voltage, this corresponds to a mean free path  $l_{\rm e}$  of ~300  $\pm$  30 nm in the 1D limit and ~20  $\pm$  5 nm in the 3D limit. The associated Fermi wavelengths  $\lambda_{\rm F}$  are smaller than the effective width of the nanowire, suggesting that a 3D approach is appropriate. Given a rather high carrier density from the capacitance models, the conductance of ~1  $e^2/h$  corresponds to partial transmission of many transverse quantum modes,

corresponding to a multimode conductor. This mean free path  $l_{\rm e}$  represents a significant improvement over previous work, <sup>27</sup> where  $l_{\rm e}$  was found to be limited by ionized dopant scattering on an  $\sim$ nm length scale.

Reported electron mobility values in free-standing InGaAs NWs at room temperature range between 500 and 1500 cm $^2$ / (V s), for similar In content. <sup>42,43</sup> We associate this difference, in part, to the reduced diameter and the presence of strong surface and boundary scattering at both the top surface and disordered GaAs/InGaAs interface. In addition, the presence of alloy scattering due to disorder, as evidenced by the STEM EDS investigations, is also likely to play a role in limiting mobility in this ternary system. <sup>71</sup> While our result is on the low end of this spectrum, we stress that our wires, grown by a SAE approach, enable scalability not achievable via standard growth techniques.

The magnetoconductance of the devices was then probed. Figure 3d and e displays the conductance as a function of the applied perpendicular magnetic field *B*. Again, the results are independent of which Y-junction arms are used. The enhanced conductance at zero field indicates the presence of weak anti-localization (WAL), a hallmark signature of the SOI. WAL is the result of the accumulating spin precessions around momentum-dependent effective magnetic fields arising from spin—orbit coupling in the Dyakonov—Perel mechanism. In the quasiclassical, clean limit 73–76

$$\Delta G = \frac{e^2}{h} \frac{1}{L} \left[ 3 \left( \frac{1}{l_{\phi}^2} + \frac{4}{3l_{so}^2} + \frac{1}{l_{B}^2} \right)^{-1/2} - \left( \frac{1}{l_{\phi}^2} + \frac{1}{l_{B}^2} \right)^{-1/2} - 3 \left( \frac{1}{l_{\phi}^2} + \frac{1}{l_{e}^2} + \frac{4}{3l_{so}^2} + \frac{1}{l_{B}^2} \right)^{-1/2} + \left( \frac{1}{l_{\phi}^2} + \frac{1}{l_{e}^2} + \frac{1}{l_{B}^2} \right)^{-1/2} \right]$$

$$(2)$$

for a multimode quasi-1D wire, where the phase coherence length  $l_{\phi}$  is exceeding the wire width W and  $l_{\rm e}\gg W$ . Here, e is the electron charge, h is the Planck constant,  $l_{\rm so}$  is the spinorbit length, and  $l_{\rm B}$  is the magnetic dephasing length, which in the clean limit  $l_{\rm e}\gg W$  is given by

$$l_{\rm B}^{\ 2} = \frac{C_1 l_{\rm e} l_{\rm m}^{\ 4}}{W^3} + \frac{C_2 l_{\rm e}^{\ 2} l_{\rm m}^{\ 2}}{W^2} \tag{3}$$

where  $l_{\rm m} = \sqrt{\hbar/eB}$  is the magnetic length and  $C_{1,2}$  are constants dependent on the type of boundary scattering.<sup>73</sup> Here, similar values were obtained in using both specular and diffusive boundary scattering. The coherence length,  $l_{\phi}$ , is a measure for how far an electron will travel on average before having its phase randomized due to inelastic scattering events. The spin-orbit length,  $l_{so}$ , is the typical length for the spin to precess appreciably and is, thus, a key measure for the strength of the SOI, with a shorter  $l_{so}$  corresponding to stronger spinorbit coupling. We mention here that our extracted mean free path falls outside the clear validity of either of the clean ( $l_e \gg$ W) or diffusive  $(l_e \ll W)$  limits. Thus, we have done the fits in both regimes (see the Supporting Information for details), giving very good agreement with the experiment. We obtain values of  $l_{\phi} \sim 100$  nm and  $l_{\rm so} \sim 80$  nm using both the clean and diffusive limits. For the clean regime fits,  $l_e = 20 \text{ nm}$  was held

fixed in order to extract  $l_\phi$  and  $l_{\rm so}$  unambiguously. The presence of WAL indicating strong SOI in the system is also a clear advance over previous results,  $^{27}$  in addition to the longer mean free path. Also, the coherence and spin—orbit parameters extracted here are very similar to other studies.  $^{28,29,48}$ 

Both Dresselhaus and Rashba SOIs are key resources for topological quantum computation and spin qubits. Dresselhaus SOI, on the one hand, is due to a lack of crystal inversion symmetry. NWs, particularly those with low symmetry and/or large aspect ratio cross sections, can have a strong Dresselhaus SOI, as recently predicted.<sup>77</sup> Rashba SOI, on the other hand, is due to a breaking of structural inversion symmetry, often appearing at an interface or surface. Both types of SOI may be gate-controlled, i.e., by changing the electric field (Rashba)<sup>78–80</sup> or by gate-tuning the wave function asymmetry (Dresselhaus). Given the width of the present NWs, the estimated Dresselhaus contribution is negligible. We have measured the gate voltage dependence of the magnetoconductance. The resulting plot is shown in Figure 3d. Universal conductance fluctuations and charge switchers can often obscure the results of the magnetoconductance. In order to mitigate this, we coupled an AC-oscillation to the top gate.<sup>81</sup> Using the model from eq 2 over the full gate voltage range,  $l_{\phi}$ and  $l_{so}$  are found to be essentially independent of gate voltage (see Figures S5 and S6). This can be attributed to the wraparound geometry of the gate, effectively shielding the NW from applied electric fields, while still allowing one to gate-tune the density (see Figure 3b). Thus, the WAL observed here is presumably due to the Rashba effect arising from built-in electric fields in the structure, such as gradients in the bandgap, presence of ionized dopants, or surface effects. In the Supporting Information, we give more details and a full analysis of the data with and without the AC oscillation.

# CONCLUSION

We have demonstrated that remote doping of InGaAs NW networks grown by SAE is a promising approach to improving their quantum transport properties. Remote doping has enabled significant improvement of the key transport parameters such as the mean free path and SOI strength over previous bulk-doped NWs.<sup>27</sup> Together with increased In content lowering the band gap, the Y-junctions exhibit WAL, indicating strong SOI, which is a necessary ingredient for future applications in topological quantum computation. These measurements further serve as proof of the quality of the crystal across NW Y-junctions, and this work opens up new perspectives into using this approach in networked quantum computing schemes.

#### **■ EXPERIMENTAL SECTION**

**Growth.** MBE growth was performed in a DCA P600 solid-source MBE chamber. Twenty-five nm of  $SiO_2$  was deposited on GaAs (111)B substrates by plasma-enhanced chemical vapor deposition (PEVCD). These were patterned by e-beam lithography using 35 nm of ZEP resist and etching in an SPTS APS dielectric etching tool employing  $SF_6$  and  $CHF_3$  chemistry. After resist stripping in an  $O_2$  plasma, the samples were etched for 10 s in a highly dilute buffered HF solution to remove  $\sim$ 5 nm of  $SiO_2$  everywhere and smoothen the mask. Samples were then loaded and annealed at 400 °C for 2 h in a degassing chamber followed by 630 °C for 30 min in the growth chamber immediately before growth. The GaAs buffer

NMs were grown at a temperature of 630 °C at an equivalent 2D GaAs growth rate of 1 Å/s with an arsenic BEP of  $4\times10^{-6}$  Torr. They were grown to an equivalent 2D thickness of 100 nm, resulting in structures with a height of  $\sim\!300$  nm. Toward the end of the buffer growth, Si dopants were introduced for a short duration via a Si sublimation cell at a rate of  $10^{13}~\rm cm^{-2}~\rm s^{-1}$  to achieve the desired doping profile, nominally 2 nm below the surface of the NM. After GaAs growth, the substrate temperature was decreased to 540 °C, while the As BEP was increased to  $8\times10^{-6}$  Torr for InAs deposition. The In flux corresponded to an InAs equivalent growth rate of 0.1 Å/s. The In flux was closed after the 2D equivalent grown thickness of 60 nm of InAs, and the sample was then cooled down under As flux.

**STEM.** Cross sections of the samples were prepared first in a FEI Nova 600 Nanolab dual-beam SEM/FIB tool before being loaded into a FEI Tecnai Osiris microscope operating at 200 keV in STEM mode. Elemental contrast was obtained by EDS thanks to four cryo-cooled Super-X silicon drift detectors (SDDs).

APT. To protect the sample from damage during FIB milling, the sample was coated with 120 nm of Ni using ionbeam sputtering at 9 kV and 7 mA. Then, a further protective Pt capping layer was deposited by ion beam induced deposition prior to lift-out using a FEI Helios dual-beam focused ion beam. Wedge-shaped lift-outs were welded onto Si microposts, and annular milling was used to isolate the region of interest within a needle-shaped tip with a diameter of 20-60 nm. APT analysis was performed using a local-electrode atom-probe (LEAP) 5000 XS (CAMECA, Madison, WI) with a 355 nm wavelength laser under the following conditions: 250 kHz pulse rate, 30 K background temperature,  $2.5 \times 10^{-11}$ Torr background pressure, and 0.4% target detection rate. An initial pulse energy of 3 pJ was used to evaporate through the surface oxides; pulses of 0.65-0.74 pJ were used in the region analyzed. APT data were reconstructed using IVAS 3.8.5 software. The tip profile method was applied, in which SEM images of the nanotips before analysis were used to determine the reconstructed radius as a function of analyzed depth.

**Contacts and Electrical Measurements.** The devices were cleaned with standard solvents, and the contacts were patterned with e-beam lithography, followed by an  $O_2$  plasma cleaning. Before metallization, the samples were then exposed to an ammonium polysulfide  $(NH_4S_x)$  solution for 150 s to remove the native oxide. <sup>82</sup> Contacts were deposited by dualangle evaporation of 14/50 nm of Cr/Au to achieve suitable sidewall coverage. Next, 40 nm of HfO<sub>2</sub> was deposited by ALD followed by another round of e-beam lithography and metallization to pattern the top gates. Finally, the sample was bonded into a chip carrier and measured using standard lock-in techniques in a variable temperature insert cryostat. Similar results were reproduced on another sample from the same wafer.

# ASSOCIATED CONTENT

# Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.0c00517.

Finite element simulations, indium signal mapping by X-ray fluorescence, further magnetotransport measurement results, and atom-probe tomography on additional heterostructures. (PDF)

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### **Author Contributions**

\*M.F., K.C.: Equal contribution.

### **Notes**

The authors declare no competing financial interest.

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