Influence of LDD spacers on total ionizing dose response of the transconductance for bulk MOSFETs working at cryogenic temperatures

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Abstract

In this work, the radiation responses of 0.25 µm bulk transistors irradiated up to 300 krad are discussed. The electricals characteristics shown are measured after irradiation at 95 K, 150 K, and 300 K. The transconductance improves significantly with total ionizing dose (TID) at low temperature and does not vary at room temperature. The impact of incomplete ionization of impurities introduced into the Lightly Doped Drain extensions is examined. Since the transconductance increase is more pronounced for the shortest transistors, positive charges trapped in spacer oxides are likely to constitute the source of this increase. The Technology Computer-Aided Design simulations help us to discuss the influence of charge build-up at the spacers' locations on the drain to source resistance. By the means of a resistivity analysis, the influence of LDD doping level and operating temperature on the TID response of devices is analyzed. Its potential evolution with technological integration is investigated.

Keywords: Cryogenic effect, total ionizing dose, transconductance, TCAD simulation, spacers

1. Introduction

Exploration of Jovian icy bodies or infrared imaging applications relies on electronics working at cryogenic temperatures in space environments. Natural radiative environments such as space are known to cause negative effects on Current-Voltage characteristics, which can result in on-board electronics failures. Consequently, space-system designers and space agencies must precisely understand the combined effect of radiations and very low temperature electronics. For practical application reasons, the impact of radiation on electronic components is most often studied at room temperature. However at room temperature, some effects of the Total Ionizing Dose (TID) on transconductance cannot be observed. These effects come from the specificities of transistors working at cryogenic temperatures [1] and will be subject of discussion in this article.

Cryogenic temperatures demonstrate significant improvements on DC characteristics (subthreshold slope, leakage current, noise). At the same time, TID degradations are often more pronounced at low temperatures in the literature [1]–[5]. Carrier freeze-out and incomplete ionization of doping species make radiation hardness of cryogenic electronics a challenging issue with notable technology, design, and operation conditions dependencies. It is commonly accepted that the charged traps created by irradiation degrade the free carrier mobility. The main mobility decay, usually observed at room temperature, is caused by interface traps acting as scattering centers at Si/SiO_2 interface [6]. It has also been shown that oxide trapped charges play a key role in mobility degradation at low temperature [7], [8] through Coulomb scattering effects. Usually, a change in transconductance is related to a change in the mobility [9].

In contrast, in this work, our data show a transconductance (g_m) improvement with the dose level at low temperature. A high g_m peak could result in device damage induced by a too large switching current. Then transconductance evolution understanding with TID is crucial. A partial peak transconductance improvement has already been observed [10], [11]. The influence of spacers on g_m degradation for pMOS at ultrahigh dose level has already been discussed in great detail [12]–[15]. In this work, the objective is to explain the strict g_m improvement with dose levels encountered during

space exploration missions, for nMOS transistors working at cryogenic temperatures. This work demonstrates the physical effects taking place specifically at cryogenic temperatures, explaining why this phenomenon was not described until now.

First, the experimental setup used to obtain data at cryogenic temperatures is presented. Second, the experimental data of transconductance are analyzed to see the evolution of its behavior for different temperatures and dose levels. Then, the same analysis is carried out with conductance measurements. Third, the influence of charges trapped in spacers is investigated by the mean of Technology Computer-Aided Design (TCAD) simulations. The final section discusses in more detail the reason why the increase in transconductance is only observed at cryogenic temperatures. The evolution of this increase with the technological node is also considered.

2. Experimental Setup

In this work, the devices under test (DUT) are constituted of 0.25 µm transistors designed and provided by Lynred (manufacturer of cooled IR detectors). All MOSFETs have a gate width of 10 µm (except one with W=0.8 µm) and gate lengths ranging from 0.35 µm to 10 µm. Each DUT is composed of 7 nMOS and 6 pMOS transistors bonded with common body and source electrodes. The 13 MOSFETs are packaged in a DIP24 ensuring compatibility with the used electrical characterization system. The γ-ray irradiations were performed with the help of ONERA's ^{60}Co facility (MEGA); with different test conditions summarized in Table I.

Table I
Campaign Summary

Irradiation temperature (K)	Maximum dose level (krad(SiO_2)	Dose rate (krad(SiO_2)/h
95	210	1
150	185	1
300	300	3

Measurements were made for three DUT during each experimental campaign. The irradiations were carried out with a 3.3 V polarization on nMOS transistor gates connectors while other pins are grounded. All pMOS transistors connectors were grounded. The electrical characterization was made with a Keithley 4200-SCS parameter analyzer connected with a triaxial connector to a Keithley 707A Switching Matrix. The experimental setup induces a minimum measurable current in the order of pA, which only affects pre-irradiation measurements at low temperature. I_{DS}-V_{GS} characteristics were measured in the linear region (V_{DS}=100mV) at room temperature, at irradiation temperature before starting irradiations, and repeated at each TID step stress. The DUTs were enclosed in 3mm thick copper pieces so that the temperature is homogeneous around the components. The copper pieces were placed against a heat exchange plate where liquid nitrogen circulates. The photos in Fig. 1(a), Fig. 1(b) show the copper pieces, whereas Fig. 1(c) displays the thermal and electrical connections of DUT.

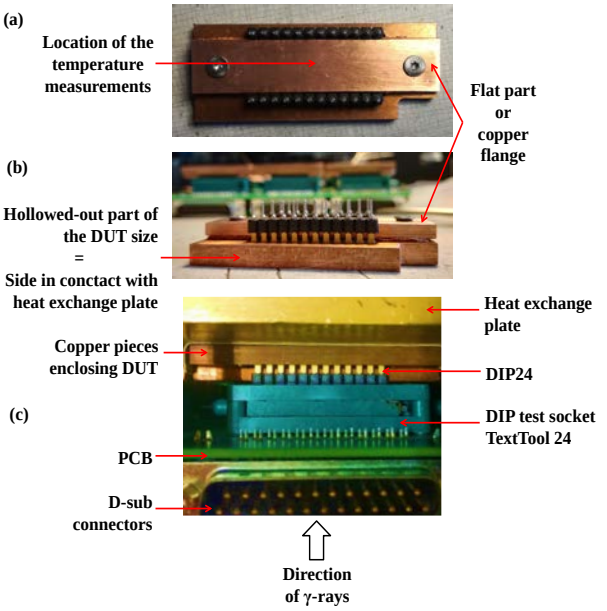

Fig. 1. (a) Top view (b) Front view of the DUT enclosed into copper pieces. (c) Front view of thermal and electrical connection of components inside the irradiation chamber.

The temperature was sensed with two platinum resistance thermometers (PT100). One was fixed to the back of a copper piece, and the second to the heat exchange plate. The temperature, and therefore the liquid nitrogen flow rate, was monitored by a Chauvin Arnoux-STATOP 4860 temperature controller. The temperature control was maintained throughout irradiation and electrical measurements with temperature variations in the range of Kelvin. The dosimetry was done inside the cryogenic chamber. Dose rate uncertainties were less than 9% and were mostly due to the radial spatial distribution of DUT irradiated at the same time.

3. Radiation results

3.1. TID response of transconductance

Fig. 2 presents I_{ds}-V_{gs} characteristics measured pre-irradiation and post-irradiation (maximum dose levels

are different see Table I) at 95 K, 150 K, and 300 K for transistors with a width and a length of 10 µm and 0.5 µm respectively. The left Y-axis is in log scale, right Y-axis in linear scale. The plotted characteristics correspond to the average of the three DUT irradiated at the same time.

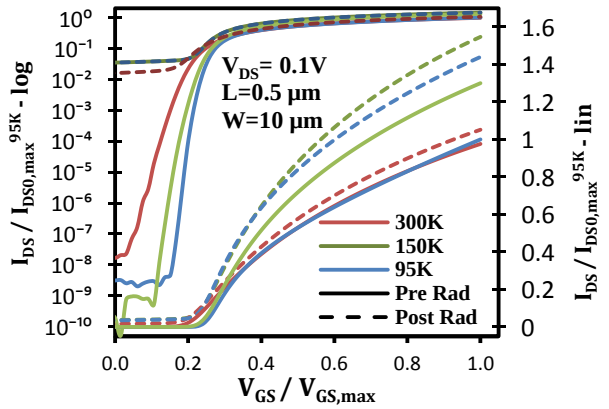

Fig. 2. Current-Voltage characteristics measured at V_{DS}=0.1V for the three temperatures considered in this study. Axis values are normalized for confidentiality reasons.

The temperature effects are analyzed with pre-irradiation curves corresponding to full lines in Fig. 2. As it is well known, a decrease in temperature increases the threshold voltage V_{TH}. The threshold voltage is obtained with Second-Derivative method [16]. At 95 K, V_{TH} is 135 ± 7 mV bigger than at room temperature. As seen with dashed curves in Fig. 2, TID has a strong impact on transistors characteristics. All the transistors are leaking at about $0.03\times I_{d0,max}^{95K}$ for a distinct maximum dose level. All the transistors show a V_{TH} shift to a smaller value. $\Delta V_{TH}/V_{TH0}$ is around 8%, 9%, and 13% at 300 K, 150 K, and 95 K respectively. In modern CMOS, gate oxides are sufficiently small to accumulate very few charges due to the tunnel effect [17]. Thick silicon oxides such as Shallow Trench Isolation (STI) and spacers used as a mask for Lightly Doped Drain (LDD) engineering are becoming the major TID degradation sources. The influence of temperature on the ΔV_{TH} and I_{OFF} is consistent with the state of the art. Moreover, a very good correspondence with previous results has been observed, whose analysis can be found in [2]. In this paper a focus on the transconductance is made which had not been examined previously.

In Fig. 2, the current-voltage characteristics demonstrate notable differences for gate voltages above the threshold voltage (i.e. $V_{GS}/V_{GSmax} > 0.3$). At 300 K, the ON state I-V slope does not differ much after 300 krad(SiO_2) exposure, whereas cooled nFETs display a major slope improvement after irradiation.

The transconductance is defined as the slope with the following equation:

$$g_m = \frac{dI_{DS}}{dV_{GS|V_{DS}}} \quad (1)$$

The transconductance curves are plotted as a function of the gate voltage for two different gate lengths in Fig. 3. The transconductance is normalized by the maximum value obtained at 95 K pre-irradiation called $g_{m0,max}^{95K}$. For confidentiality reasons, the transconductance metric is presented as a function of the gate voltage divided by its maximum value. The transconductance peak G_m, which is defined as the transconductance maximum, is relatively close from 95 K to 150 K in Fig. 3(a). Its maximum value is obtained at 150 K before any radiation exposure. At the lowest temperature 95 K, g_m shows a sharp decline directly after its maximum and remains steady afterwards. In Fig. 3(b), pre-irradiation transconductance is strictly decreasing with temperature, with a peak value 5 times higher at 95 K than at 300 K.

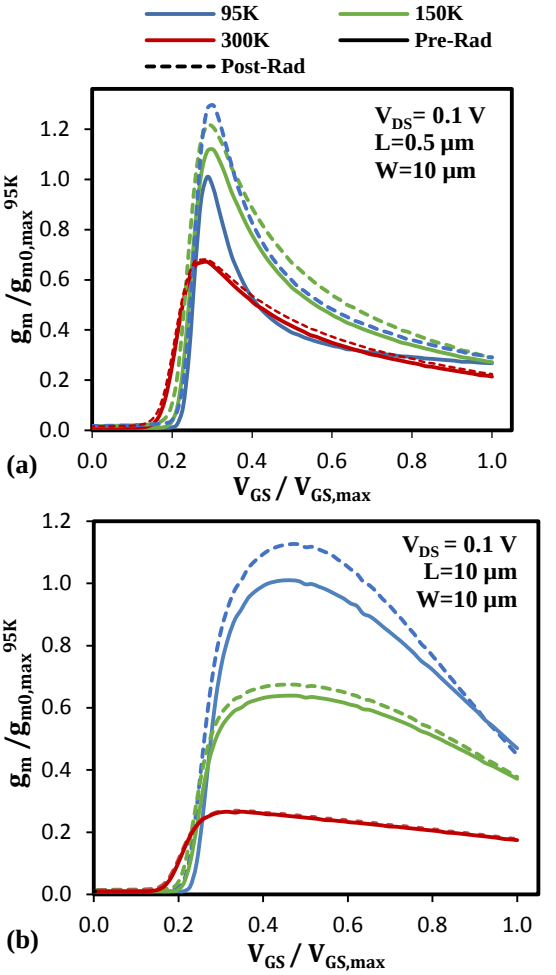

Fig. 3. Transconductance evolution versus gate voltage at V_{DS}=0.1 V. Axis values are normalized for confidentiality reasons. (a) L=0.5 µm (b) L=10 µm.

The bell-shaped blue curve observed in Fig. 3(b) is

the same as the one expected at 77 K, with effective mobility peaking at intermediate transverse field [18]. This thermal influence on mobility can be explained: when the temperature drops, the thermal vibrations of atoms around their equilibrium position diminish. The effective collision cross-section occupied by the atoms is reduced. The transport of carriers is therefore conditioned by coulombic interactions of ionized impurity. In conclusion, the phonon scattering can be neglected at low temperature. Then Coulomb scattering is becoming the major contribution of mobility for a moderate transverse electric field. It is also for a moderate transverse electric field that the transconductance peak is located [6], [18].

Another interesting point that can be noticed is the impact of the radiations on the electrical characteristics by looking at dashed curves in Fig. 3(a). The gamma irradiation has no significant effect on the g_m at 300 K. On the opposite, at 95 K and after 210 krad(SiO_2) deposited G_m increases by about 30% in comparison to its value before irradiation. The peak transconductance value is now the highest at 95 K. After its peak, post-irradiation g_m falls off with V_{GS} in a smoother way at 95 K, to finally reach its pre-irradiation value for a high transverse field. At 150 K, the G_m growth is smaller (about 8%) and the transconductance slope is the same with the curve translated upwards.

For long transistors shown in Fig. 3(b), the change in transconductance after gamma rays exposure is smaller than for L=0.5 µm transistors. G_m increases by 11% at 95 K, 5% at 150 K, and 1% at 300 K for the 10 µm long transistor. In conclusion, irradiated nFETs operating at 95 K see its G_m value raised and the sharp decline opposed. In the linear region, the following equation is defined [19]:

$$g_m = V_{DS} C_{ox} \frac{W}{L} \frac{\mu_0}{1+\theta_1(V_{GS}-V_{TH})^2} \quad (2)$$

with C_{ox} the gate oxide capacitance, μ_0 the low field mobility and ϑ_1 the first-order attenuation mobility directly proportional to Drain to Source Resistance (R_{SD}). Thus, such a transconductance increase after irradiation at cryogenic temperature could be explained by 1) R_{SD} decrease and/or 2) μ_0 increase.

3.2. TID response of conductance

The conductance g_D is analyzed in this section. It corresponds to the inverse of the total device resistance, including the contribution of drain to source parasitic resistance. It is defined as the following equation: $g_D = dI_{DS}/dV_{DS}$. Fig. 4 shows g_D as a function of V_{DS} at various temperatures. The conductance is normalized by the maximum value obtained at 95 K pre-irradiation ($g_{d0,max}^{95K}$). The drain voltage is shown divided by its maximum value.

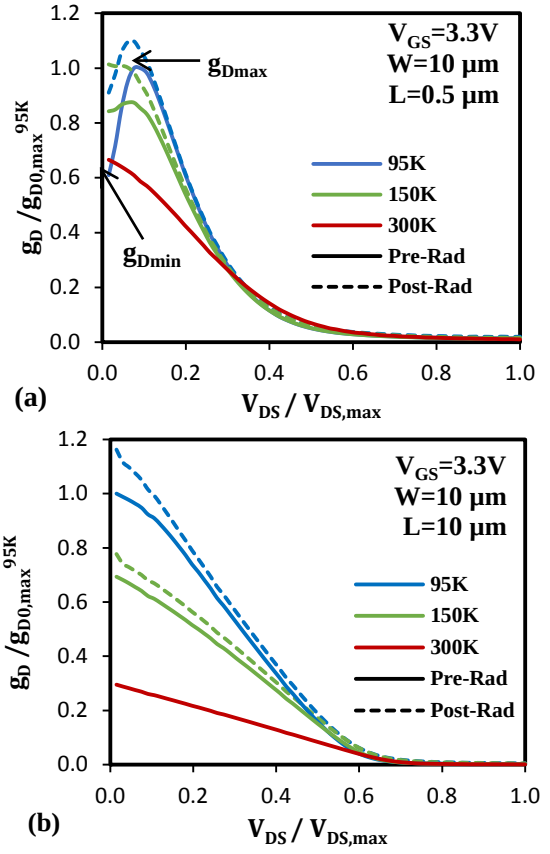

Fig. 4. Experimental conductance evolution with drain voltage at V_{GS}=3.3 V. Data are shown for the 3 different temperatures. Axis values are normalized for confidentiality reasons. (a) L=0.5 µm (b) L=10 µm. Dashed curves represent post-irradiation measurements.

Pre-irradiation data are represented with full lines and data measured at maximum dose level with dashed lines (not measured at room temperature). Before irradiation and at low drain voltage, g_D shows a great increase at 95 K, before reaching a maximum at approximately $V_{DS}/V_{DS,max} \approx 0.1$ as shown in Fig. 4(a). At higher drain voltage the conductance starts to decrease to reach its saturation value, common for all temperatures. The local minimum appearing when V_{DS} tends to zero is named g_{Dmin} in the following of the paper. g_{Dmax} is defined as the maximum of the output conductance. The difference between g_{Dmin} and g_{Dmax} is way less marked at 150 K and totally absent at 300 K in Fig. 4(a). This temperature-related minimum phenomenon illustrates the drastic increase in R_{SD} due to impurity freeze-out occurring in the LDD areas. This result is consistent with a previous work from Hafez, *et al.* [20]

As it can be seen in Fig. 4(a), both g_{Dmin} and g_{Dmax} grow after gamma exposure (210 krad(SiO_2) at 95K

and 185krad(SiO_2) at 150K). g_{Dmin} growth is more significant than g_{Dmax} at 95 K, but nearly equal at 150 K. The evolution of these quantities with the dose is detailed in Fig. 5.

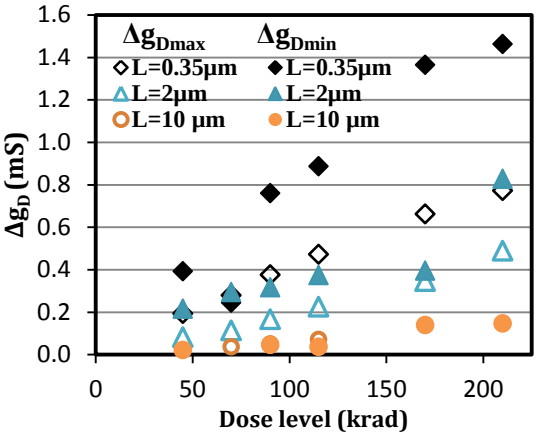

Fig. 5. Conductance variation as a function of dose level at 95 K. Data shown are for L=0.35, 2, 10 µm.

In Fig. 5, Δg_{Dmax} (empty symbols) and Δg_{Dmin} (solid symbols) are plotted as a function of the dose level, measured at 95 K. All the measured conductance are for nFETs with W=10 µm and various gate lengths. The conductance increases linearly with the dose for all lengths. For long transistors (L=10 µm), minimum and maximum are equals thus the orange symbols overlap. Also, it can be clearly seen that g_{Dmin} increase is stronger than g_{Dmax} for short transistors. As described by [20], the ratio g_{Dmin} / g_{Dmax} is directly related to the proportion of ionized dopants. When the ratio is equal to 1, all the dopants are supposed to be ionized. Since g_{Dmin} increases faster than g_{Dmax}, the ratio is also increasing to a value close to 1. Hence, irradiated nFETs show a more complete ionization of LDD dopants.

According to [20] at high drain voltage the parasitic LDD resistance is also highly reduced thanks to the Poole-Frenkel effect or shallow level impact ionization. The Poole-Frenkel effect describes the release of an electron trapped in a potential well. The presence of an electric field reduces the height of this barrier. Applied to our problem, it would be the electric field close to LDD areas that would lower the height of the energy barrier E_D needed for the impurity to be ionized. With a sufficiently large electric field, the potential barrier is lowered enough so that thermal energy enables the electron to reach the conduction band, even at 95 K. Therefore, the charges generated by radiation and trapped in spacers create the electric field responsible for the increase in the ionized dopant amount N_D^+ in LDDs.

With a complete ionization of LDDs, the most resistive part would be the channel as it is the case at room temperature. By decreasing parasitic series resistances of LDD regions, conductance grows with the dose. As it can be seen in Fig. 5, this effect is more significant as the transistor length decreases. This is attributable to the increasing relative importance of LDD resistance when the channel length is smaller.

It is important to note that g_{Dmax} is also increasing. This is the case for FETs with L=10 µm (see Fig. 4(b)) or at 150 K, where the non-ionized LDD dopants have no or hardly perceptible effects on conductance. Even with LDD completely ionized, space charge effects can be observed. Indeed, positive trapped charges in the spacers attract negative free carriers close to the LDD/channel transition. These additional free carriers participate in the current, reducing the conductance. The free carrier mobility might be improving with dose as well. Finally, since V_{TH} shifts to a smaller value with TID, the current flowing at constant gate voltage (V_{GS}=3.3 V) increases (i.e. conductance g_D) for a fixed drain voltage. Then, even with a constant parasitic R_{SD}, the conductance should be rising with the dose level. That is why experimental R_{SD} values extracted with [21] are not shown.

It was not possible to conclude whether what caused the resistance to decrease were space charge effects, doping, mobility, or just a mechanical decrease with this data. These ideas will be further developed with the help of numerical simulations instead. The transconductance (Fig. 3) and conductance (Fig. 5) improvements are lower for the longer transistors with a fixed width. Effects related to the gate length can be attributed to the charge build-up located in spacers thick insulators [15] and will be analyzed with TCAD simulations in the next section.

4. Spacer related effects

4.1. Simulation set-up

The interplay with charges trapped at the spacer' location and electrical characteristics is investigated with Sentaurus TCAD simulations. First, a 3D structure has been calibrated with pre-irradiation I_{ds}-V_{gs} characteristics at room temperature with the help of the design kit. Since the TID-induced increase in transconductance appears to be related to the accumulation of charges localized in the spacers, the simulations are considered to be independent of the transistor width. Consequently, in this work, the electrical characteristics are obtained with a 2D TCAD structure as shown in Fig. 6. The metal work function, gate oxide thickness, doping concentration of bulk, drain and source have been unchanged. The transconductance characteristic obtained with the numerical 2D structure is plotted and compared to the experimental transconductance in Fig. 7.

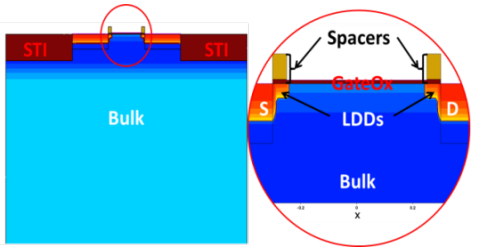

Fig. 6. Schematic 2D nFETs modeled with TCAD. Yellow=Si_3N_4, brown=SiO_2, blue=p-Si, red/orange=n-Si.

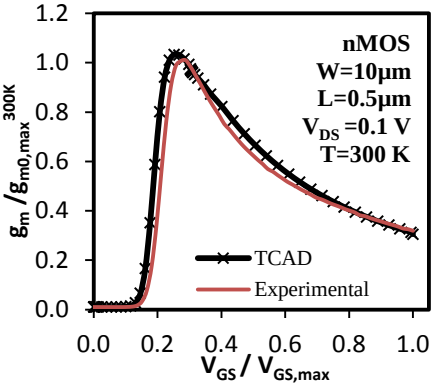

Fig. 7. Calibrated transconductance at room temperature obtained with 2D nFETs with spacers.

The mobility models used are Arora for mobility doping dependence and Lombardi for transverse field mobility dependence (both of them take into account temperature). To model impurity freeze-out, the Fermi statistics and Incomplete Ionization models are used [22]. Furthermore, since the temperature of the devices during exposure and the maximum dose levels reached are different, post-irradiation trapped charge density should also be. These values will not be adjusted to match the experimental curves.

4.2. LDD Resistance

Fig. 8 shows the g_m characteristics (black curves) obtained with TCAD simulations at 95 K and 300 K and compared to experimental measurements respectively (colored curves). The simulated as-processed structure (i.e. pre-irradiation) is simulated without any charges. The impact of the ionizing dose is considered only with additional positive charges in spacers with different densities. The black dashed curves represent $g_m(V_{GS})$ obtained with a positive charge density of $5x10^{11}$ cm^{-2} introduced at LDD/spacers oxides interface.

The charge introduction in spacers leads to a very slight transconductance increase at both temperatures, which is also observed experimentally in Fig. 8(b). The relative increase of G_M approaches 1% in Fig. 8(a).

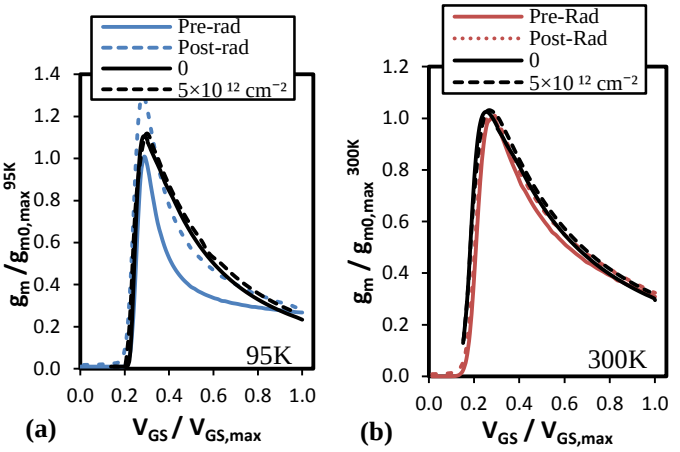

Fig. 8. Experimental (colored curves) and simulated (black curves) transconductance characteristics with calibrated TCAD structure

This value is far from the 30% increase measured at 95 K. Another limitation is the modeled pre-irradiation behavior at 95 K, which is unsatisfactory. The sharp decline after g_m peak is totally absent. The TCAD model completely misses the representation of the TID effects for transistors operating at cryogenic temperature, although it is convincing at 300 K.

The remaining difference in pre-rad curve is explained by a change in LDD doping level induced by TID. N_{LDD0} is the maximum introduced value of n-type dopants at the LDD/spacer interface. The given value of N_{LDD0} is the one preceding the calculation of the incomplete ionization. N_{LDD0} has been lowered to 10^{18} cm^{-3} to retrieve pre-irradiation behavior. The curves plotted in Fig. 9 are obtained with the same method as in Fig. 8, with reduced doping levels for LDDs.

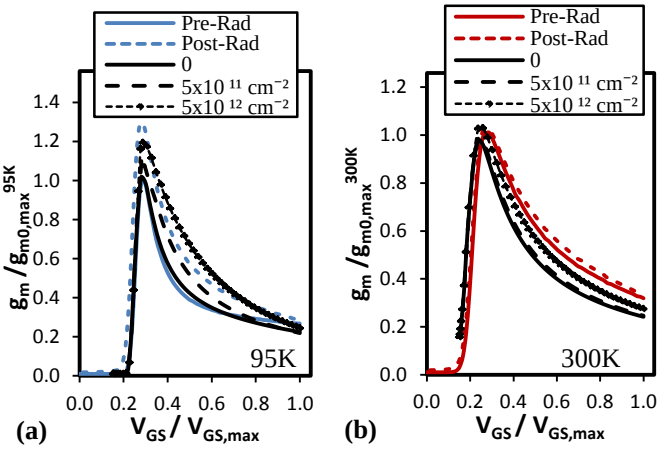

Fig. 9. Experimental (colored curves) and simulated (black curves) transconductance characteristics with lowered LDD doping (10^{18} cm^{-3}) at (a) 95 K (b) 300 K.

In Fig. 9(a), the modeled pre-irradiation transconductance at 95 K is much more representative. After introducing charges, the decrease of simulated g_m is the same as the experimental one, characterized by

the mobility dependence with V_{GS}. At 300 K (Fig. 9(b)), even when LDD are completely ionized, the transconductance increases to a lesser degree. At this temperature, a large number of free carriers are present at the LDDs. The free carrier density increase caused by space charge effect is thus weaker in proportion at 300 K.

The same simulation parameters have been used to obtain the characteristics $g_m(V_{GS})$ for transistors with different gate lengths. The results are shown in black for nFETs with L=0.35 µm and in orange for nFETs with L=10 µm in Fig. 10. The solid lines represent the pre-irradiation characteristics and the dashed lines represent the post-irradiation characteristics simulated by charged spacers.

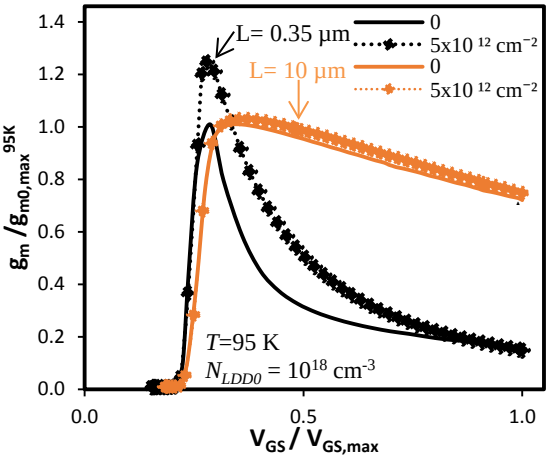

Fig. 10. Simulated transconductance characteristics for nFETs with (a) L=0.35µm (b) L=10µm. The $g_{m0,max}$ value used for normalization is the one obtained for each length.

Fig. 10 evidently demonstrates the impact of gate length on the G_m increase. For L=0.35 µm, the g_m characteristics are similar to the previous one (cf. Fig. 9). The main difference is the peak value, which increases by 24% in Fig. 10. For L=10 µm, the behavior is significantly different. The G_m increase is only about 2%, and the gap between the curves does not vary with the gate voltage.

We can conclude that the LDDs have more influence on the radiation response of smaller transistors. In addition, the decrease of the parasitic $R_{SD,}$ due to charged spacers, is not sufficient to reproduce the experimental behavior for long transistors. This suggests that mobility improvement is the dominant mechanism in the g_m variation with the deposited dose for long transistors. This is consistent with the analysis of conductance done in section 3.2. The authors were unable to demonstrate, using TCAD simulations, an increase in the free carrier mobility after the introduction of irradiation-related charged traps. Further work will concern DUTs compatible with split C-V mobility measurements. Thanks to that, the transconductance increase could be related to mobility increase directly. On one hand, we could study the channel length effect on the mobility. On the other hand, isolate the effects of mobility from the effects of resistance which both act on electrical measurements [23].

4.3. Temperature and technology dependence

4.3.1. Resistivity peak

As forecasted with experimental conductance, the electron density in the LDD regions depends on the net doping and the space charge effects. The mobility is also dependent from the net doping since the ionized impurities deflect the free carriers. All these parameters have an impact on the resistivity ρ defined as:

$$\rho = (en\mu_e)^{-1} \quad (3)$$

With e the elementary charge, n the electron density and μ_e the electron mobility. This simplified formula only takes into account the drift component of the current. The contribution of holes can be totally neglected in strong inversion regime. The mobility and the electron density are obtained from the simulation by the mean of a TCAD cutline taken 2 nm underneath the Si/SiO_2 interface as illustrated in Fig. 11(a). Four different sets of parameters are shown: two doping levels $N_{LDD0}=10^{18}$ cm^{-3} (Fig. 11(b)) and $N_{LDD0}=10^{19}$ cm^{-3} (Fig. 11(c)) at 95 K and 300 K. The cutlines with charged spacers are shown with a positive charge density of D_{SP} = 5×10^{12} cm^{-2} (dotted colored lines). The vertical dashed lines show the delimitation of the LDD, and the vertical dotted lines the delimitation of the spacers. The resistivity is approximately equal for both temperatures in the channel and in the drain. The area of interest where the resistivity peak appears is between x=0.25 µm and x=0.3 µm.

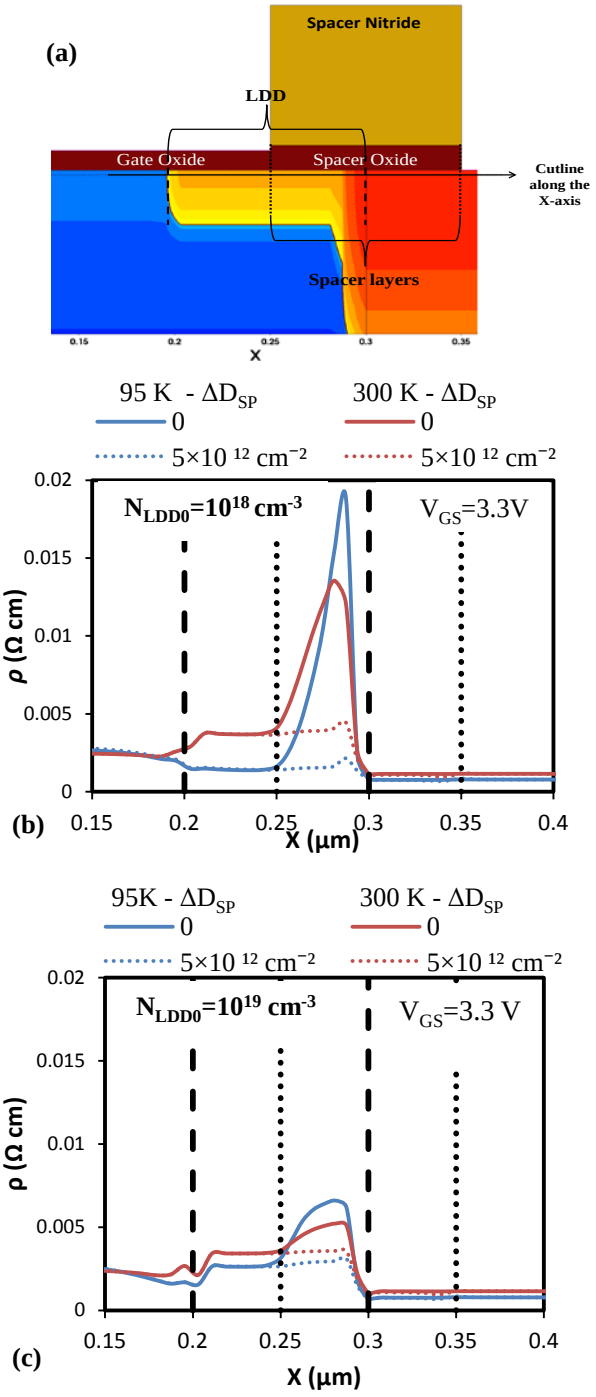

Fig. 11. (a) Illustration of the modeled structure and the cutline obtained with TCAD. The resistivity is plotted as a function of x position. x=0 corresponds to the middle of the channel. (b) At low LDD doping level. (c) At high LDD doping level.

With the low doping level in Fig. 11(b), a resistivity peak is observed at LDD position, before the radiation exposure. It is also observed at 300 K. Therefore the g_m characteristic at 300 K before exposure is too low compared to the experimental characteristic as observed in Fig. 9(b). This peak disappears with charges introduced in the spacers as stated with dashed curves in Fig. 11. The resistive peak is divided by a factor of 9 at 95 K and by a factor of 3 at 300 K after introducing charges in spacers.

The ρ value of LDD area is approximately the same as the channel area. As the channel is longer than the LDD, the channel conductance has a greater impact on the output conductance. Then, the behavior of the transconductance is characterized by the transportation of carriers in the channel. Thus, the mobility of the carriers in the channel is dependent on the gate voltage, as observed with the post-irradiation g_m characteristic in Fig. 9(a).

At a higher doping level as in Fig. 11(c), ρ peak is divided by a factor of 2 and 1.4 at 95 K and 300 K respectively. Also, the ρ peak value is closer to the ρ channel value before radiation. Consequently, the transconductance varies only slightly with the introduction of charges into the spacers (data not shown).

4.3.2. Discussion on transconductance increase evolution

The net increase in transconductance is never observed for nFETs in other papers studying the impact of spacers [12], [13], [15] and the radiation-induced short channel effects. This is probably because, at room temperature, a change in LDD resistivity due to trapped charge has no visible effects on output transistors characteristics. Indeed, the channel intrinsic mobility is greatly improved when transistors are cooled down with the absence of the phonon contribution to scattering processes. As it was described for long nFETs in Fig. 3(b), the G_m peak is 4-5 times greater at 95 K than at 300 K. In a simplified approach, we can consider that the channel has a 4-5 times greater equivalent resistance at 300 K than at 95 K. In addition, LDDs are completely ionized at room temperature. Their equivalent parasitic resistance is drastically lower at 300 K, as discussed in Fig. 11. In conclusion, at 300 K a change in the parasitic resistance of the LDDs due to radiation is smaller and represents a much less significant contribution to the equivalent device resistance. The device resistance is the sum of parasitic resistance and channel resistance. Therefore the transconductance and conductance improvements with TID, both related to device resistance, cannot be observed at room temperature. In contrast, this effect is particularly pronounced for short transistors operating at cryogenic temperatures.

Additionally, the interface traps generation is severely reduced below 140 K since the H^+ ion transport is blocked [24]. Although the studied devices are more advanced technology nodes, it has been

shown in [12] that H^+ transport plays the leading role in transconductance degradation. This phenomenon, opposed to our observations, cannot be observed at cryogenic temperature.

The very large scale integration (VLSI) roadmap demonstrate in addition to the reduction in transistor size , an increase in the channel doping to achieve a constant electric field scaling [25]. With highly advanced technology nodes, the capacity of the drain/substrate is becoming a limiting element because of the induced frequency limitations. In order to mitigate this effect, the LDD doping level is increased in the same way as the channel doping level.

ΔE_D is the energy needed for impurity to be ionized (or activation energy), defined as the difference between energy level of the conduction band E_C and the donor ionization energy E_D. At high impurity concentration N_{LDD0}, the energy barrier for dopant activation ΔE_D is reduced [26]. This energy barrier vanishes at $3x10^{18}$ cm^{-3} [20]. As a consequence, the impurity band overlaps the conduction band and the carrier freeze-out does not occur anymore. If LDDs are completely ionized, the drastic drop of the conductance observed in Fig. 4 should no longer be perceived. It means that the radiation-induced dopant ionization either. Only space charge effects need to be considered, which are also reduced when the doping level increases as illustrated in Fig. 11(c) and [14].

The resistance shift dependencies on doping and temperature are summarized in Fig. 12. It shows the relative deviation of transconductance peak versus N_{LDD0}. Two different charge densities are introduced into spacers. The dashed vertical line marks the doping value at which the ionizing energy of impurities vanishes. All curves decrease with the density of dopant atoms introduced. They also all tend towards a zero value for a high doping level. By looking at diamond symbols, we can see that with complete ionization, the deviation is 6% whereas it is 18% at 95 K for the doping levels considered in Fig. 9. With a higher doping level, there is little change in transconductance since the channel is the most resistive part. Space charge effects are not visible for a charge density of 5×10^{12} cm^{-2} with a relevant doping level of 10^{19} cm^{-3} for LDD. This could explain why the g_m degradations are starting to be observed experimentally after a dose level of about a Mrad [3], [12], [15], [27].

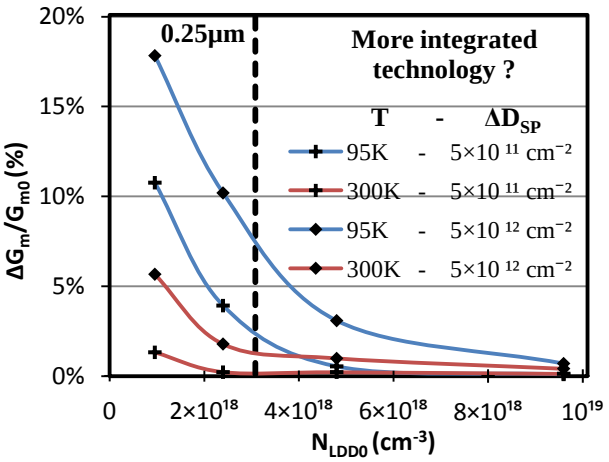

Fig. 12. Relative deviation of transconductance peak for a given ΔD_{SP} introduced as a function of LDD doping level.

With the following results, we can forecast that there will be no more variation of transconductance after an exposure to radiation for dose levels met during space missions. On the other hand, a too high level of LDD doping is opposed to the primary function of LDD in reducing hot-carrier effects. Also, as the gate length decreases, the LDD will influence an increasing part of the device response if they are not reduced in length as well. In conclusion, the radiation response of cryogenic electronics is a complex concern, with significant technology, bias conditions and design dependencies.

5. Conclusion

This work explores the transconductance behavior of nMOSFETs irradiated at cryogenic temperatures. An unusual transconductance increase, unobserved at 300 K, is experimentally demonstrated at 95 K after gamma irradiation. The positive charges trapped in spacer oxides are likely to be responsible for the increase in transconductance, since it is more pronounced for shortest transistors. Thanks to conductance measurements, it can be concluded that the radiation-induced trapped charges reduce the incomplete ionization of LDD in nMOSFETs. The parasitic R_{SD} created by LDD is therefore also reduced after the low temperature irradiation. For long transistors where LDD effects are hardly perceptible, the conductance also increases after a TID exposure. The low field mobility μ_0 increase could explain such transconductance improvement. The effect of the interaction between the charged spacers and the LDDs on g_m are discussed and validated by the mean of TCAD simulations. Based on our simulations, a change in LDD doping level results in a very variable radiation response of the device. This work demonstrates that spacers and LDD regions need to be

thoroughly modeled to account for the radiation effects, especially at cryogenic temperatures. As the electric field governs the motion of the trapped holes at low temperature, possible future works could concern the effect of the drain polarization on the TID response at cryogenic temperatures.

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