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# Interpretation of 28 nm FD-SOI quantum dot transport data taken at 1.4 K using 3D Quantum TCAD simulations

Ioanna Kriekouki<sup>1,2,3</sup>, Félix Beaudoin<sup>4</sup>, Pericles Philippopoulos<sup>4</sup>, Chenyi Zhou<sup>4</sup>, Julien Camirand Lemyre<sup>3</sup>, Sophie Rochette<sup>3</sup>, Salvador Mir<sup>2</sup>, Manuel J. Barragan<sup>2</sup>, Michel Pioro-Ladrière<sup>3</sup> and Philippe Galy<sup>1</sup>

1 STMicroelectronics, 850 rue Jean Monnet, 38920 Crolles, France

2 Université Grenoble Alpes, CNRS, Grenoble INP, TIMA F-38000 Grenoble, France

3 Institut quantique, Université de Sherbrooke, 2500 Boulevard de l'Université, Sherbrooke QC J1K 2R1, Canada

4 Nanoacademic Technologies Inc., Suite 802, 666 rue Sherbrooke Ouest, Montréal QC H3A 1E7, Canada

## 1. Abstract

Reliable operation of nanoscale CMOS quantum dot devices at cryogenic temperatures fabricated with standard manufacturing techniques is of great importance for quantum computing applications. We investigated the very low temperature behavior of an Ultra Thin Body and Buried oxide (UTBB) Fully Depleted Silicon-On-Insulator (FD-SOI) quantum dot device fabricated using the standard fabrication process of STMicroelectronics. The performance of the quantum dot device is simulated and analyzed using the 3D Quantum Technology Computer Aided Design (QTCAD) software recently developed by Nanoacademic Technologies, achieving convergence down to 1.4 K. In this paper we present preliminary simulation results of this work and compare them with experimental data collected from the measurements on a device with the same geometry.

## 2. Introduction

Quantum computers, which use quantum bits (qubits) as their building blocks, promise to harness quantum mechanics to deliver disruptive advantages over a wide range of classical technologies. Quantum dots in silicon offer a promising approach to implement physical qubits. In this architecture the quantum information is encoded into the spin of a single electron or hole confined in the quantum dot [1, 2].

Qubits based on silicon quantum dots in conventional CMOS technologies promise to enable reproducible, high-yield industrial manufacturing [3] and co-integration [4] with classical control hardware, two decisive steps toward scalability [5-9]. In addition, by shortening R&D cycles, industrial spin-qubit production promises to accelerate the development of novel scaled-up devices coupling several qubits together for large scale, high-fidelity logical operations. A milestone towards a scalable qubit architecture is to develop a silicon-based qubit structure fabricated using exclusively CMOS industrial manufacturing techniques.

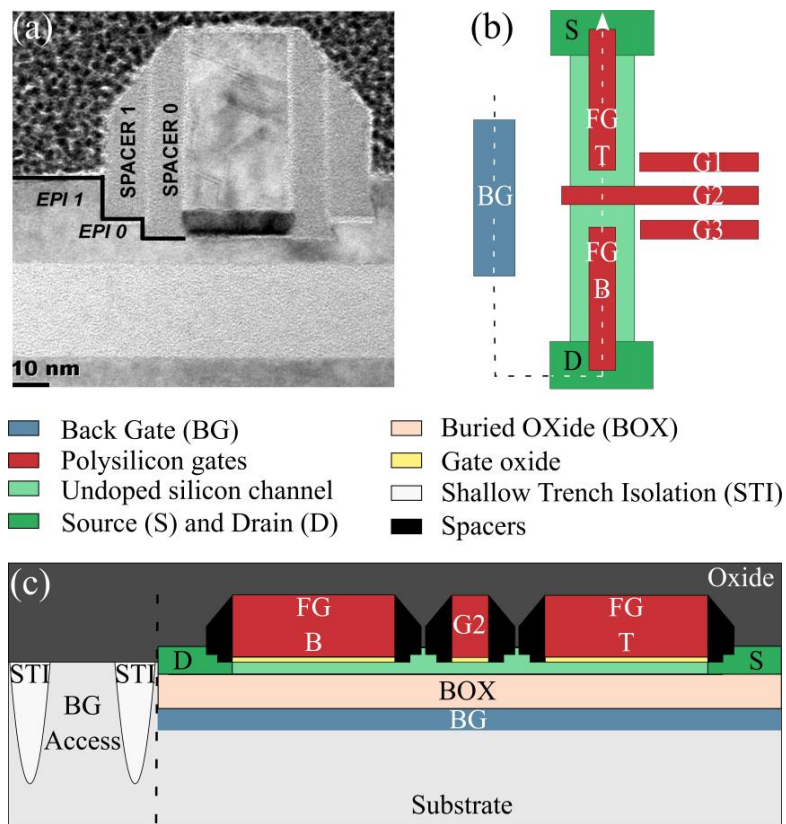
Our device is based on the 28 nm Ultra-Thin Body and Buried oxide (UTBB) Fully Depleted Silicon-On-Insulator (FD-SOI) technology node of STMicroelectronics which has already demonstrated functional operation at cryogenic temperatures [10-15]. In order to define a consistent and fast design flow for quantum dot devices, it is crucial to predict their performance at cryogenic temperatures and to understand the electrical and quantum phenomena that occur using a simulation environment, before actually fabricating the device. This is a key step to avoid lengthy fabrication-and-measurement optimization loops that are time-consuming due to the long fabrication and characterization cycles. As a step forward towards this direction, we

demonstrate the use of a 3D Quantum Technology Computer Aided Design (QTCAD) simulation tool for modeling our quantum dot device at cryogenic temperatures.

### 3. 28 nm UTBB FD-SOI technology

The quantum dot architecture developed and studied in this work is based on a modification of a conventional MOSFET using the 28 nm UTBB FD-SOI technology node [16].

Figure 1 (a) shows a TEM image of a typical UTBB FD-SOI MOSFET. This four-terminal device consists of a source, a drain, a top gate, and a back plane that can be used as a back gate thanks to a thin 25-nm thick layer of Buried OXide (BOX). The device possesses a thin and undoped 7-nm thick silicon film playing the role of the body channel between the source and the drain.



**Figure 1:** (a) TEM image illustrating the cross-section of a typical FD-SOI MOSFET. The spacers and epitaxial layers are indicated on the device. Image taken from [17]. (b) Schematic representation showing the top view of the split-gate device. (c) Schematic representation showing the cross-section of the split-gate device taken along the dashed line depicted in the top-view.

### 4. 28 nm UTBB FD-SOI split-gate device

The quantum dot device that we studied is based on the split-gate architecture [18] and was designed and fabricated using the thick-gate-oxide Regular  $V_{th}$  option of the 28 nm STMicroelectronics FD-SOI technology. As illustrated in Fig. 1 (b) and (c), the source and the drain are n-doped and epitaxially grown to reduce the access resistance. Spacers are used to limit the source/drain extensions (also known as lightly doped drains) under the gate. The top gates are made of polysilicon, and the back plane is p-doped. Shallow Trench Isolation

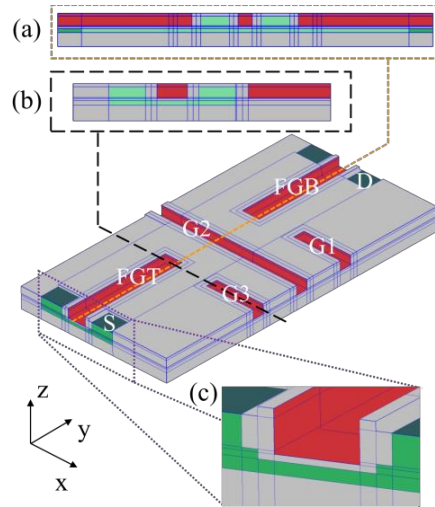
(STI) trenches filled with oxide allows electrical contact to the back gate. To complete the CMOS fabrication process, silicide is formed almost everywhere on top of the source, drain and gates, excluding the region over the channel where the quantum dot is expected to be formed.

The gate (G2) is designed to control the quantum dot potential in the silicon channel splits the front gate in two parts: Front Gate Top (FGT) and Front Gate Bottom (FGB). A positive voltage on both parts of the front gate is used to form the two-dimensional electron gas (2DEG) at their interface with the oxide to create the source (drain) reservoir. The two additional lateral gates (G1 and G3) were initially designed to obtain extra control over the tunnel barriers between the reservoirs and the quantum dot by controlling their heights and widths. We will see that, instead, they lead to the formation of corner dots.

## 5. Quantum Technology Computer Aided Design model at cryogenic temperatures

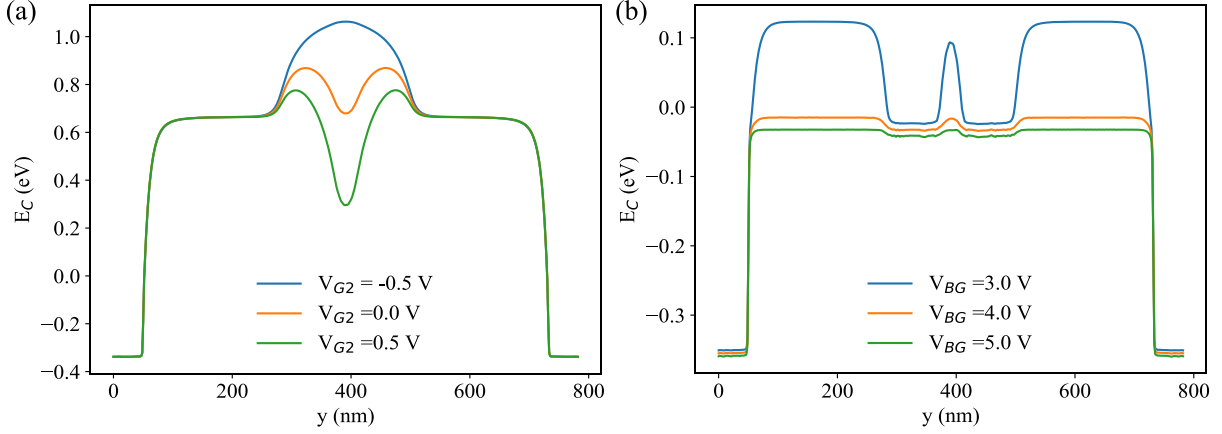
We modeled our quantum dot device using the Quantum Technology Computer Aided Design (QTCAD) simulation tool [19, 20]. This finite-element modeling (FEM) software developed by Nanoacademic Technologies Inc. allows the simulation of the electrical and quantum behavior at cryogenic temperatures.

The 3D geometry of the quantum dot structure was defined via the FEM mesh generating tool Gmsh [21]. A first-order mesh containing 2.5 million nodes was generated, with local refinements in regions of fast potential variations to improve precision and convergence. Once the different materials and regions were defined, the electrodes and the doping were specified. The resulting computer-aided design (CAD) model is illustrated in Figure 2. Isothermal conditions were assumed in all simulations with a uniform temperature of 1.4 K imposed throughout the device. Polysilicon gates (red surfaces in Fig. 2) and Ohmic contacts (surface at the bottom of the BOX, dark green surfaces at source and drain in Fig. 2) set Dirichlet boundary conditions on the electrostatic potential. All simulations were executed on the Niagara cluster of Compute Canada [22].



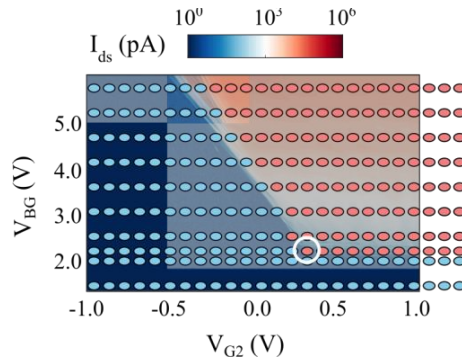
**Figure 2:** 3D model of the FD-SOI nanostructure from the layout used for fabrication of the device via Gmsh [21] and the QTCAD simulation tool. The device is used to form electrostatically defined quantum dots under the electrodes for quantum computing applications. (a) Cross-section along the y-axis illustrating the two parts of the front gate (red), the gate G2 (red) and the silicon channel (pale green) grown on the BOX (gray). (b) Cross-section along the x-axis illustrating the channel, the front gate lying on the silicon film and the gate G3 that lies on the oxide. (c) Cross section along the x-axis presenting the channel, the epitaxially grown source and drain, the spacers, the gate stack and, finally, the gate oxide. The darkest green shade indicates surfaces at which Ohmic boundary conditions are imposed in the simulations.

Assuming thermodynamic equilibrium, the non-linear Poisson equation [23, 24] is solved self-consistently, yielding the electrostatic potential and the classical charge distribution that corresponds according to the statistical physics of semiconductors. Figure 3 shows the conduction band edge plotted for different voltages applied on the gate G2 and the back gate following a linecut located along the y-axis in the middle of the front gate (see Figure 2) and at 0.1 nm above the BOX.



**Figure 3:** Simulated conduction band profile using the simulation tool QTCAD at 0.1 nm from the BOX into the silicon film along y-axis parallel to the transport (see Fig. 2). A 2DEG at the Si/SiO<sub>2</sub> interface is observed, along with an ability to tune the potential barrier height by applying the appropriate voltages to G2 and the back gate. (a) A voltage sweep is performed on the gate G2 with all the other gates grounded. (b) A voltage sweep is performed on the back gate with all the other gates grounded. The zero of energy corresponds to the Fermi level.

The formation of a single electrostatic quantum dot under the gate G2 was not observed experimentally. Nevertheless, this gate can be used for tunnel barrier control when the conduction channel is activated by the



**Figure 4:** Measured current as a function of  $V_{BG}$  and  $V_{G2}$  forming the charge stability diagram. Density plot: experimentally measured current. Blue dots: numerical calculations of the band diagram predicting blocked transport. Red dots: numerical calculations predicting allowed transport. In the device measured at 1.4 K, a transport apex is identified at  $(V_{G2}, V_{BG}) = (0.34, 2.24)$  V (white circle). In the simulated device, it is identified at  $(V_{G2}, V_{BG}) = (0.0, 3.7)$  V. The numerical data have been shifted in the  $V_{G2}$  and  $V_{BG}$  axes by 0.34V and -1.46V, respectively, so that these two apexes fit together.

BG and the rest of the gates are grounded, as shown by the simulation results in Fig. 3 (b). Here, we show that experimental data demonstrating channel activation is well explained by QTCAD simulations at 1.4 K.

Figure 4 shows the stability diagrams extracted for a voltage sweep performed on G2 while the voltage on BG was stepped. We could distinguish two regimes in this diagram starting from the transport apex that is indicated in the figure with a white circle. First, beyond this point, the transport is activated only by the back gate. Second, below this point, G2 acts as a tunnel barrier and  $V_{BG}$  must be increased to overcome the barrier and activate transport. This behavior is well reproduced by QTCAD simulations shown by the red and blue dots in the figure, with the slope of the oblique line delimiting transport regions being nearly identical in theory and experiment. The shift of the theoretical transport apex with respect to experiment is expected because numerical simulations do not account for surface charges trapped at the gate oxide interfaces; in fact, these shifts may eventually be used to estimate the magnitude of the charge trap density.

## 6. Observation of corner dots in the FD-SOI split-gate device

We now show numerical and experimental evidence that corner quantum dots [25] can be formed in front of G1 and G3 when these lateral gates are polarized positively.

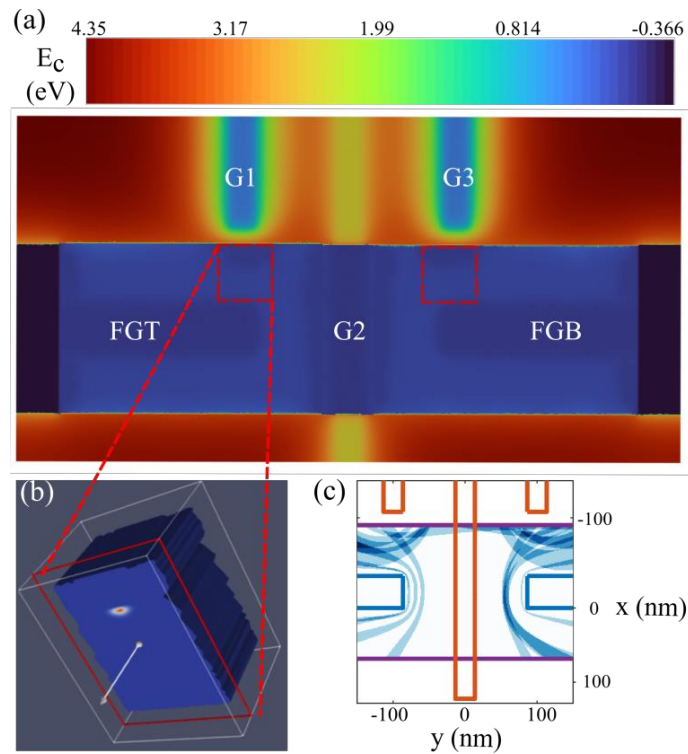
At low voltage and without back body biasing, the tunneling barriers due to the distance between the gates FGT, G2 and FGB do not allow transport to be measured experimentally without exceeding the polysilicon gates nominal supply voltage (1.8 V) of this technology. However, when a voltage of the order of 10 V is applied on G1 and G3, the additional potential forces the conduction band under the Fermi level and forms a conduction channel. It is possible to apply voltages much higher than 1.8 V on these gates without risking damaging the structure, since the lateral gates are not built on the gate oxide layer as opposed to FGT, G2, and FGB. Reference [26] reports current measurements resulted in charge stability diagrams which enabled a triangulation analysis suggesting the formation of quantum dots near G1 and G3 (Figure 5 (c)).

QTCAD simulations predict the appearance of corner dots at positions that are compatible with experimental observations. More precisely, Figure 5 (a) shows the numerically calculated conduction band edge profile over a slice along the x-y plane, 1 nm below the interface between the channel and the gate oxides. This band edge displays clear energy-potential minima in front of G1 and G3. The numerical solution of the 3D single-electron effective-mass Schrödinger's equation resulted in bound eigenstates that are localized near the top edge of the channel in front of G1 and G3 (Figure 5 (b)).

Sequential tunneling simulations were also done using QTCAD's many-body and master equation solvers to better understand transport measurements. These simulations predicted that single electrons may in principle be loaded in the corner dots at G1 and G3 voltages approaching 2 V. However, at this voltage, potential barriers surrounding the dots are too high to lead to measurable currents, explaining why the single-electron regime was not observed at the experimental gate bias of 10 V at which Coulomb diamonds were measured.

## 7. Conclusions

We reported our work on the simulation of a 28 nm UTBB FD-SOI split-gate device at cryogenic temperatures with the QTCAD simulation tool. Electrostatic simulations done with QTCAD at 1.4 K elucidated channel activation via the combined action of G2 and the back gate. In addition, effective-mass Schrödinger calculations corroborated the experimental observation of quantum dots near G1 and G3, and clarified their corner-dot nature. Finally, transport simulations explained why the single-electron regime was not



**Figure 5:** Experimental evidence and numerical simulations supporting the presence of corner dots near G1 and G3. Fixed voltages are applied on the gates. In this particular example:  $V_{G1}=V_{G3}=4\text{V}$ ,  $V_{FG}=0.843\text{V}$ ,  $V_{BG}=0\text{V}$ ,  $V_{G2}=1.7\text{V}$ . (a) Numerical calculation of the conduction band edge. (b) Numerical calculation of the ground state of single electrons near G1. (c) Quantum dot triangulation analysis based on experimental data. Quantum dots are expected to form in the darkest blue areas.

experimentally observed for these dots. These results pave the way to the integration of QTCAD into the gated quantum-dot design workflow.

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**Ioanna Kriekouki** received a M.Sc. degree in Nanosciences and Nanotechnologies in 2017 from the University Grenoble Alpes (UGA) of Grenoble, France, and is currently a CIFRE (Convention Industrielle de Formation par la Recherche) fellow PhD candidate in UGA and Université de Sherbrooke in France and Canada respectively, in collaboration with STMicroelectronics in France. Her research is focused on silicon MOS nanostructures and quantum devices designed and fabricated with standard manufacturing techniques for quantum computing applications.

**Felix Beaudoin** first obtained an M. Sc. in theoretical physics from Université de Sherbrooke under the supervision of Prof. Alexandre Blais, followed by a Ph.D. in theoretical physics from McGill University with Prof. William A. Coish. He then worked as a postdoctoral associate and university lecturer at Dartmouth College in the research group of Prof. Lorenza Viola, in close collaboration with the Quantum Information and Integrated Nanosystems Group led by Prof. William D. Oliver (Massachusetts Institute of Technology). He cumulates over 10 years of research experience in the field of quantum technology, with more than 10 scientific publications in peer-reviewed journals on quantum noise, quantum control, quantum metrology, and modeling of spin qubits and superconducting qubits alike. He joined Nanoacademic in 2019 as a Research Scientist and is now Director of Quantum Technology managing the development of the QTCAD quantum modeling tool.

**Pericles Philippopoulos** obtained his PhD in Physics from Prof. William Coish's group at McGill University in 2020. The focus of his work was to gain a better understanding of spin interactions, specifically hyperfine and spin-orbit couplings, in semiconductor nanostructures. He also has experience using first-principles methods (DFT) to calculate fundamental properties (e.g. hyperfine couplings, electric-dipole moments) for electrons and holes in semiconductors. He joined Nanoacademic Technologies in 2020. Since then he has been working on developing features (e.g. valley-coupling, EDSR) and modeling tools for the QTCAD software.

**Chenyi Zhou** obtained his PhD from McGill University in the field of theoretical/computational condensed matter physics, with a specialization in modelling nanoscale transport in the presence of disorder and many-body interactions. He is also experienced in numerical programming for materials simulations in the Density Functional Theory (DFT) framework. He joined Nanoacademic in 2020 where he is the lead developer of our NEGF-based quantum transport modules.

**Julien Camirand Lemyre** holds a PhD from Université de Sherbrooke where he designed, developed, and fabricated quantum devices for various qubit architecture. He is specialized in building qubits architecture with scaling in mind. He is now President and CTO of Nord Quantique, where he developed a superconducting-based bosonic qubits platform to reduce the quantum hardware overhead toward fault-tolerant quantum computing.

**Sophie Rochette** received a Ph.D. in Physics from Université de Sherbrooke, Quebec, Canada, in 2020. She studied silicon quantum dots for quantum information applications, with a focus on design optimization towards fabrication with industrial standard processes.

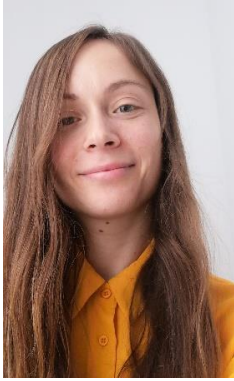
**Salvador Mir** (Member, IEEE) received an Industrial Engineering degree (Electrical, 1987) from the Polytechnic University of Catalonia, Barcelona, Spain, and M.Sc. (1989) and Ph.D. (1993) degrees in Computer Science from the University of Manchester, UK. He is a Research Director of CNRS (Centre National de la Recherche Scientifique) at TIMA Laboratory in Grenoble, France. He founded the Reliable Mixed-signal Systems Group at TIMA Laboratory in 2002 which he led until 2014 when he became director of the Laboratory until December 2020. His area of expertise is analog/mixed-signal/RF/MEMS design for test. He has been General, Program, Topic Chair and member of the Steering Committee of many IEEE/IFIP International Conferences. He is editor and co-author of two books on silicon Microsystems, and the co-author of 5 best paper awards in IEEE ETS'09, IFIP/IEEE VLSI-SoC'10, IEEE ETS'12, IEEE ETS'15 and IEEE ETS'18.

**Manuel J. Barragan** received a M.Sc. degree in Physics in 2003 and a PhD in Microelectronics in 2009, both from the University of Seville, Spain. He is currently a researcher with the French National Research Council (CNRS) at TIMA Laboratory, France, where he leads the Reliable RF and Mixed-Signal Systems group. His research is focused on the topics of test and design for test of advanced analog, mixed-signal, and RF integrated systems.

**Michel Pioro-Ladrière** received his Ph.D. in experimental physics from Université de Sherbrooke, in 2005 in partnership with the National Research Council of Canada (NRC), winning the NRC Exceptional Accomplishment Award in the process. He was then welcomed as a Post-Doctoral Fellow with the Japan Science and Technology Agency from 2005 to 2009, where he pioneered a micromagnet approach to realize efficient single spin rotations, which is currently used worldwide in spin-based quantum information processing research. He was recruited as an expert in spin qubit technology back in 2009 by Université de Sherbrooke, in collaboration with the Canadian Institute for Advanced Research (CIFAR), to jumpstart the first research program in Canada that utilize components found in today's microchips to ultimately create a quantum computer. He has been the Deputy Director of Institut quantique, Université de Sherbrooke since 2016. He has authored 50 peer-reviewed articles and three patents. He is a member of Unité Mixte Internationale – Laboratoire Nanotechnologies et Nanosystèmes, CNRS, France, and was a CIFAR Fellow with the Quantum Information Science Program for 10 years.

**Philippe Galy**, born 1965, obtained his Ph.D. from the University of Bordeaux (France) in 1994. He holds a H.D.R. (academic research supervisor) from LAAS CNRS University of Toulouse in 2005. He has authored or co-authored over 155 publications, 4 books, and 136 patents portfolio. Philippe serves in several Technical Program Committee and he is a reviewer for many symposiums and journals (Ex: ESREF / ESSDERC / ICICDT /EUROSOI / CAS / VLSI / TED/ TON/SSE). He joined STMicroelectronics in 2005, working on ESD and new solutions for device to SOC level in advanced CMOS and mature technologies (Bulk / FDSOI / planar & 3D). He develops tooling concepts for robust IP integration and supervises its developments till production. His main R&D topics are on SCR, T2, TFET, BIMOS transistor, Beta-structure and other innovative memory devices for emerging neuromorphic, silicon qubit cryogenic applications. Based on these topics he supervises 15 PhD. He was

involved in National & European projects: Examples: Fr. Nano 2017-2020 / Eu. ROBIN / REMINDER / Neuram3/QLSI). Also, he is a member of the QuEng CDP group in Grenoble, France.



Ioanna Kriekouki



Felix Beaudoin



Pericles Philippopoulos



Chenyi Zhou



Julien Camirand Lemyre



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