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Macrosteps formation on 4H-SiC surfaces via Si melting within a sandwich configuration

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Abstract

With a view to designing a homogeneous and controlled step-bunched morphology on large monocrystalline 4H-SiC(0001) surfaces, a sandwich configuration was investigated. A piece of silicon was melted between two 4H-SiC 4° off wafers, allowing a better spreading of the liquid than with a Si drop approach. Using as low liquid Si thickness as 30 μm, homogeneously highly step-bunched surfaces were obtained, though with irregular step shapes. This was found to be the result of time dependent dissolution of the SiC-bottom wafer under the natural vertical thermal gradient of the setup. The most parallel step and terrace structures were generated using 400 μm thick liquid Si though this led to long range inhomogeneities associated with complex mass transport. The proposed mechanism includes the combined effect of H₂ etching at the edges acting as C pump and electromagnetic convection rolls for long range transport of these dissolved C atoms.

Keywords: B.2 Semiconducting silicon compounds, A1. Crystal morphology, A1. Surface structure, A1. Solubility, A1. Convection, A3. Liquid phase epitaxy

1. Introduction

Among wide bandgap semiconductors, silicon carbide (SiC) has become the most mature and mainstream material for power electronics applications. It has superior physical properties such as high breakdown field, high thermal conductivity and high electron saturation velocity compared to Silicon (Si) [1] while showing great compatibility to Si-based fabrication technologies as SiC and Si share the same native oxide, SiO₂. These characteristics have notably led to the intensive development of SiC-based metal oxide semiconductor field effect transistors (MOSFETs), which are nowadays the most fostered switches to improve the efficiency in electric energy conversion

systems [2]. 4H is the polytype of choice for MOSFET fabrication due to its higher bulk carrier mobility as compared to 6H [3].

Despite their attractivity and already wide use, 4H-SiC MOSFETs have not yet reach their full potential as their performances remain limited due to low channel mobility [4]. A high density of electrically active defects at the SiO₂/SiC interface is being held accountable for this limitation [5]. While the origin of these interfacial traps is still under debate, recent experimental studies [6] attribute them to the step-and-terrace morphology inherent to commonly used 4° off-axially grown epitaxial surfaces [7]. Indeed, after epitaxial growth by chemical vapor deposition (CVD) for the fabrication of the n-doped active layer, the obtained surface morphology is not atomically flat: it is composed of a sequence of atomic steps (having height of few Si-C bilayers) called microsteps, along with so called macrosteps corresponding to bunched microsteps, leading to step heights and terrace widths (space between two steps) in the 1 to 5 nm range [8]. This morphology is expected to crucially impact the creation of the SiO₂/SiC interface, for instance by initiating non-ideal oxidations and nonstoichiometric near-interface regions [9]. The negative impact of the steps was confirmed later by Woerle et al. [6] who used different spatially resolved analysis techniques to see that the highest density of interface defects is located on the step edges of the SiO₂/SiC interface. Terraces, which are atomically flat, revealed the lowest interface defect density. It goes in the same direction as another recent related study showing that MOS capacitors fabricated on large terraces of a macrostepped surface display a systematic decrease of the interface traps density of ~10-15% compared to “standard” samples [10]. In order to further investigate this effect, one needs to reproducibly control the formation of these wide terraces which should be as large and parallel as possible for being able to separate the contributions of step edges and terraces.

Liquid phase growth of 4H-SiC is known to generate very large terraces but one cannot use this technique for elaborating the n-doped epilayer of a MOSFET due to too high residual doping level of these liquid phase grown layers [11]. Alternatively, the only contact of a Si-based solution onto a 4°off 4H-SiC surface is known to generate a reconstruction leading to macrosteps formation [12][13]. These few related works systematically involved the use of pure liquid Si, in a sessile drop configuration, to produce terraces of a few μm in width, which is more than 100 times wider than those found in standard epitaxial surfaces grown by CVD. This sessile-drop approach was appropriate for preliminary demonstration and for small areas of ~0.5 cm². Nevertheless, if one wants to further investigate such surface towards fabrication of improved power devices, extrapolation of this liquid-induced macrostepping process to larger areas is required. Simply increasing the Si amount of the droplet in the sessile-drop configuration would not work due to the

too high amount of Si required, which could even break the 4H-SiC wafer upon solidification and cooling. One needs to develop a process in which the liquid Si is more spread over the surface than with the only natural spreading allowed by thermodynamic equilibrium (wetting angle of $\sim 40^\circ$ [14]). This should allow drastic reduction of the Si amount and better control of the reconstructed area dimensions. The present work aims at studying the use of a sandwich configuration for liquid spreading and thus the potentialities of such configuration for increasing the size of the liquid Si-treated 4H-SiC 4° off (Si face) surfaces. This will be discussed in regards to the macroscopic homogeneity of the surface reconstruction and to the resulting morphologies of 4H-SiC surfaces.

2. Experimental

The samples consisted in a SiC/Si/SiC stacking where a piece of n-type Si wafer was placed in between two 4H-SiC (0001) 4° off Si-face wafers (Figure 1.a). Commercial 4H-SiC wafers from SK Siltron CSS were used as-received, they display a surface RMS roughness as low as ~ 0.2 nm for a $YY \times YY$ μm atomic force microscopy (AFM) scan. To avoid any liquid Si loss at the SiC wafers sides, the chosen lateral size of the bottom wafer (SiC-bottom) was larger than the one on top (SiC-top), i.e., 2×2 cm^2 and 1.2×1.2 cm^2 for the bottom and top wafers, respectively. The pressure applied by the top wafer is expected to force the liquid Si to spread on both surfaces until reaching the square edges of the SiC-top wafer (Figure 1.b). Such natural spreading is expected to lead to homogeneous Si liquid thickness between the SiC wafers, which are thus considered parallel. One important parameter of this work is the value of Si thickness between the two SiC wafers. We noticed that measuring this thickness after the experiment can lead to important errors due to systematic and significant Si overflows out of the sandwich upon solidification. That is why we used an indirect way for estimating this thickness. Assuming that the area occupied by the liquid Si is equal to the surface of the SiC-top wafer ($= 1.44$ cm^2), with no liquid overflow when molten (as confirmed experimentally), we can calculate the liquid Si thickness (th_{Si}) during the experiments from this area and the mass of the initial Si wafer piece using the following equation:

$$th_{\text{Si}(\mu\text{m})} = \frac{m_{\text{Si}}}{d_{\text{Si}} \times S} \times 10^4$$

with m_{Si} and d_{Si} the mass of the Si piece (in g) and the Si density (in $\text{g}\cdot\text{cm}^{-3}$) respectively, and S the area of the top-SiC wafer (1.44 cm^2).

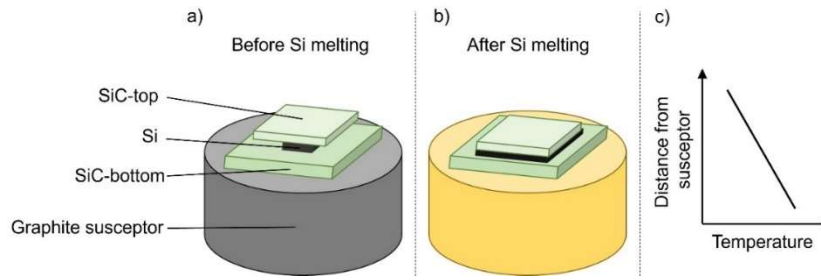


Figure 1. Schematic drawings of the investigated sandwich setup a) before and b) after Si melting and c) the expected vertical thermal gradient in this configuration.

Each part of the assembly was degreased in methanol using an ultrasonic bath. After drying, the stacking was assembled directly on the SiC-coated graphite susceptor which was then inserted into a homemade vertical cold wall CVD reactor working at atmospheric pressure. All experiments were performed under 12 slm hydrogen (H_2) gas flow. The use of inert gas (argon) was not considered in this work since it is known to generate gas trapping (and thus unwetted areas) in similar configuration [13]. We observed the same phenomenon in a preliminary attempt using Ar (not shown) so that it was replaced by H_2 which never led to any similar gas trapping feature. The graphite susceptor was heated up to the targeted temperature by radio-frequency (15 kHz) from an external induction coil. The temperature was set using an Eurotherm temperature controller and measured by an optical pyrometer directly on the susceptor. The melting temperature and plateau duration were varied in the 1550-1600°C and 30-120 min ranges, respectively. The heating rate to reach the temperature plateau was as fast as $\sim 400^\circ\text{C}/\text{min}$. At the end of the plateau, the assembly was cooled down naturally under flowing H_2 which led to the very fast solidification of Si just after few seconds of cooling. The elaboration conditions of the samples studied in this paper are listed in Table 1.

Sample	Temperature [°C]	Time [min]	Liquid Si thickness [μm]
A	1550	30	30
B	1550	120	30
C	1600	30	30
D	1550	30	400

Table 1. Elaboration conditions of the investigated samples.

After cooling to room temperature and removal of the samples from the reactor, they were etched in a mixture of hydrofluoric (HF) and nitric acid (HNO_3) for several hours/days in order to remove elemental Si and hence detach the two SiC pieces. After rinsing, the obtained reconstructed surfaces of both SiC-top and -bottom wafers were characterized by various means: Nomarski differential interference contrast optical microscopy (NDIC), scanning electron microscopy (SEM, FEI Quanta

250 FEG) and AFM using Nano-Observer apparatus in resonant mode (CSInstruments). For each sample, the average width was measured on NDIC and SEM pictures, over a population of 100 to 300 terraces. The obtained values are listed in Table 2. Step heights were calculated from the terrace width values and the 4° off angle of the 4H-SiC surfaces. Mechanical profilometry (Veeco Dektak 150) was performed on the areas of interest (where liquid Si/SiC interaction took place) to check the homogeneity of the surface structuring process and the possible occurrence of any mass transport phenomenon.

		Sample A	Sample B	Sample C	Sample D
SiC-top	Terrace width (μm)	1.97±1.12	2.88±1.60	2.49±1.32	3.42±1.88
	Step height (nm)	137±78	202±112	174±92	239±131
SiC-bottom	Terrace width (μm)	4.16±2.34	4.20±2.34	5.09±2.94	6.78±3.15
	Step height (nm)	290±164	294±164	356±206	474±220

Table 2. Mean and standard deviation values of the terrace width and step height measured on the reconstructed surface of the investigated samples.

3. Results and discussion

The first observation that stands out from this series of experiments is that none of the SiC wafers broke during or after the melting process. The Si solidification did not mechanically overstress the 4H-SiC crystals. Another common point of all these samples is that every SiC wafer displays a pronounced step-bunched morphology, which is easily visible by optical microscopy (Figure 2). Such structuring occurred on all the surfaces in contact with the liquid Si phase, with no obvious unreacted areas that could have resulted from gas trapping for instance [13,15]. Closer observations by SEM and AFM are shown in Figure 3. Note that no step bunching was spotted on SiC-bottom wafer outside the wetted area (thus exposed to H₂ only), where the RMS values measured by AFM are less than 1 nm compared to 50-120 nm RMS measured within the step-bunched zones.

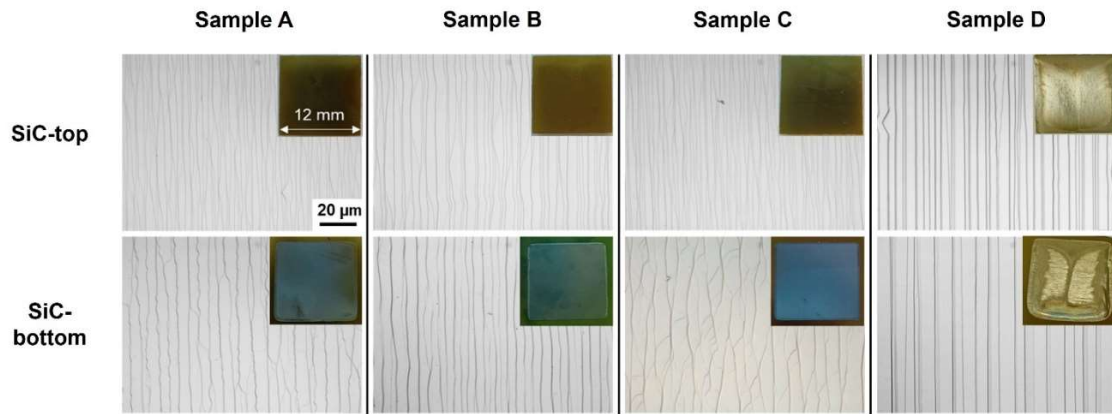


Figure 2. NDIC images taken using the same magnification (x100) on both top and bottom wafers of each investigated sample. In inserts are shown the photographs of the entire reconstructed areas.

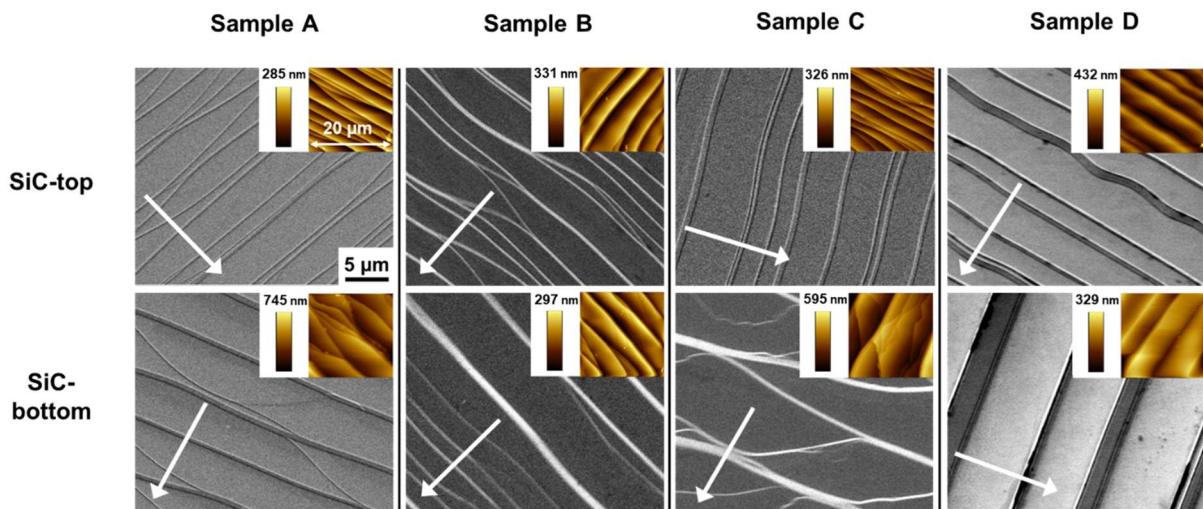


Figure 3. SEM images obtained on both wafers of each investigated sample. The $\langle 11\bar{2}0 \rangle$ direction is marked in each image with a white arrow. In inserts are shown the AFM images (20x20 μm scan) of the same sample. All images were taken at the center of the respective reconstructed areas.

It is important to specify that all the images in Figure 2 and 3 were taken at the center of each wafer. Especially in the case of sample D for which the morphology varies significantly across the surface (this will be discussed further later on). For the three other samples, the morphology is rather homogeneous (inserts of Figure 2) so that these images are representative of the entire surface.

Every NDIC and SEM image shows terrace widths of several μm and step heights of few hundreds of nm (see Table 2). These observations confirm the potential of the liquid Si interaction approach for macro-structuring of 4H-SiC surfaces on large areas.

Regarding the precise step edge shape, it differs from one sample to another. Both the position of the wafer within the stack (top or bottom) and the experimental conditions impact this structuring. Yet, a common point between all these samples is the fact that the bottom wafers always display

wider terraces in average than the top ones. But these larger terraces also display more smaller crossing-steps on top of them. Let us now discuss each parameter separately.

The effect of temperature can be seen by comparing samples A and C. Increasing temperature from 1550 to 1600°C leads to obvious terraces enlargement (see also Table 2) but also to the enhanced formation of crossing and wavy small steps on these large terraces for the SiC-bottom. The SiC-top wafer morphology seems less affected by temperature. The effect of plateau duration is illustrated by samples A and B. Longer plateau leads to wider step-free terraces on both bottom and top wafers, as if steps tended to merge over time. This change in morphology indicates that a time dependent process is taking place and that thermodynamic equilibrium is not reached after 30 min of interaction with liquid Si, unlike in [13].

Coming now to the effect of liquid thickness (comparison between samples A and D), increasing Si liquid thickness from 30 to 400 μm led to significant improvement of the straightness of the steps which are now clearly all parallel and without smaller crossing-steps on the terraces. Due to the terrace width measurement method, which does not take into account the straightness and continuity of the steps, the standard deviation values in Table 2 do not reflect this change in step edge morphology. However, the mean terrace widths are significantly higher in the case of sample D, especially for the SiC-bottom. These observations highlight the more important impact of the liquid thickness than the other parameters on the surface structuring mechanism. Finally, it is important to recall that sample D was found to display the less homogeneous morphology of the present set of samples (photographs in Figure 2) so that one can imagine some connections between this heterogeneity and the occurrence of parallel steps. In order to better understand these connections and the mechanism behind them, mechanical profilometry was performed on the processed surfaces.

Before discussing the profilometry results, it is worth mentioning that any bow of the substrates that could have resulted from the process was difficult to measure or even estimate, especially when considering that the SiC-bottom wafer is always subjected to close-space SiC growth on the back side from the SiC-coated graphite susceptor. As a result, we did not try measuring precisely this effect using the profilometry data. The 3D profiles of sample A (with only 30 μm liquid thickness) are reasonably flat on both top and bottom wafers, except for the presence of mild features (depressions and bumps) localized on the corners and edges of the reconstructed area (Figure 4). Samples B and C (for which 30 μm liquid thickness was also used) showed similar 3D maps. This is not the case of sample D for which both top and bottom wafers exhibit a butterfly-like pattern with positive height (up to +6 μm) at the center while the peripheries are delimited with deeper

depressions, from -6 to -9 μm . This butterfly pattern is similar to the one which can be distinguished by naked eye (photographs in Figure 2). This pattern having positive height compared to the unwetted area, it should result from some material gain and thus SiC deposition. Conversely, the edge depressions should correspond to some material loss and thus SiC etching. Associating these two observations, one could propose that some SiC matter transport may occur from the edges to the center.

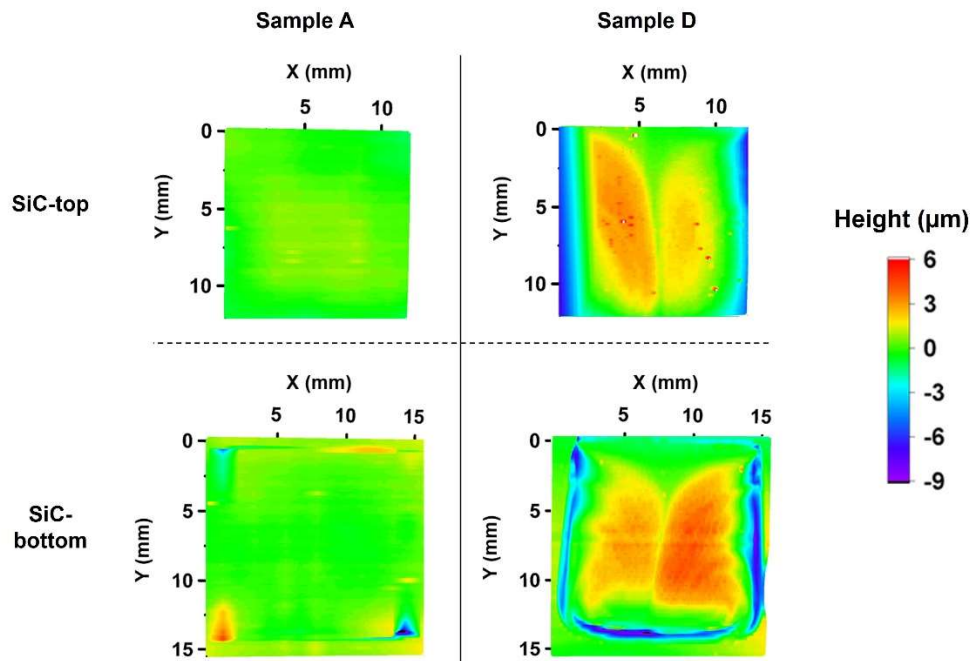


Figure 4 (in color). 3D mechanical profilometry maps obtained on samples A and D. For the SiC-bottom maps, the zero level was taken outside the reconstructed area; this was obviously not possible for the SiC-top wafers which were fully reconstructed.

Deeper investigation of samples with 30 μm Si thickness could contribute to the understanding of the phenomenon. Figure 5 shows a 2D (linear) profile obtained on SiC-bottom of sample C (treated at 1600°C and which displays the most disturbed step-bunching). One can recognize the very localized edge depressions on both sides (1.5 to 1.8 μm deep) while the step-bunching-induced roughness appears clearly in the reconstructed central area. Interestingly, the average level of this reconstructed area is ~ 0.4 μm below the one of the sample surface outside the liquid. This suggests that the area in contact with the liquid was not only reconstructed but also etched, yet in a less pronounced manner than the edges. If some etching occurs (at the center and at the edges), it is important to check whether it is time dependent or not. Some additional experiments were therefore performed with 30 μm Si thickness in order to study this evolution with time. The results are summarized in Figure 6 which plots the evolution of both the edge depression and the central area depths as a function of time. One can see that both parameters are linearly time dependent. The

edges undergo a constant etching at a rate of $\sim 2.8 \mu\text{m/h}$ (at 1550°C) which slightly increases to $\sim 3 \mu\text{m/h}$ at 1600°C . The etching rate of the reconstructed area is lower, being almost zero at 1550°C while increasing to $\sim 0.6 \mu\text{m/h}$ at 1600°C . This time dependent etching means that the system is not at thermodynamic equilibrium. Also, the difference in etching rate between the edges and the center suggests that different mechanisms are taking place.

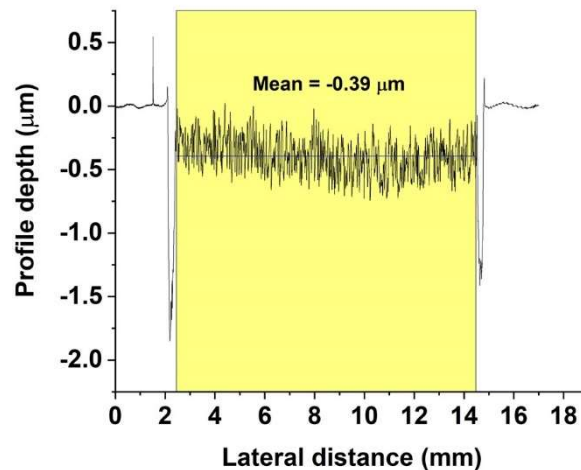


Figure 5. 2D mechanical profile of sample C (SiC-bottom)

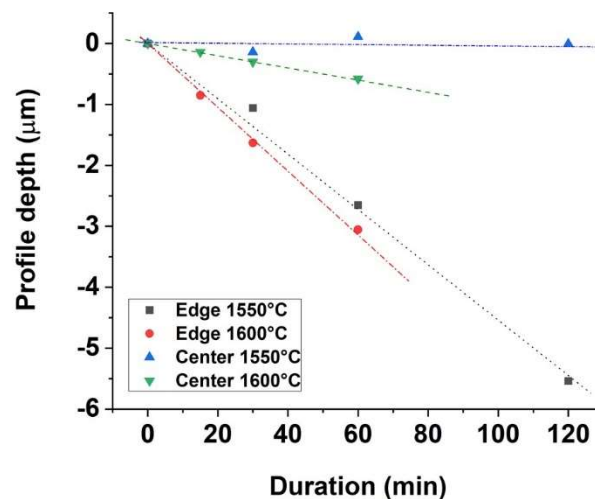


Figure 6 (in color). Time dependence of the depth measured by mechanical profiling at the edge depressions and at the center. All measurements were performed on the SiC-bottom wafers.

Though H_2 should obviously not interfere with the etching reaction occurring in the central area, we believe that it can play a role at the edges where these deep depressions are observed. This is indeed the only area where liquid Si is in direct contact with H_2 . Locally, H_2 can react with the carbon (C) atoms dissolved inside the liquid Si forming volatile hydrocarbon (C_xH_y) species, in the same way as reported in [16]. This C atom removal would thus act as a C pump and locally generate a

continuous dissolution of the SiC substrates by the liquid Si. If we consider that this mechanism is unlikely to occur far from the edges, the etching of the central area should only be due to SiC dissolution inside liquid Si. Assuming a C solubility in the 0.01 at% range at the considered temperatures [17][18] and 30 μm of liquid Si thickness, this would lead to the dissolution of ~ 3 nm of SiC. This is maybe what can happen at 1550°C but surely not at 1600°C for which etching depth of ~ 0.6 μm was measured after 1h. Adding this to the fact that this etching process is time dependent, we think that some mass transport is occurring, from the SiC-bottom to the -top wafer, driven by the natural thermal gradient inherent to the setup (Figure 1.c): the SiC-top wafer should be cooler than the bottom one due to the combination of both H₂ cooling from the above and the higher distance to the heating source (susceptor). Therefore, SiC-bottom and -top wafers should not undergo the same process: the bottom should be dissolved while the top should receive epitaxial growth. This could explain the morphological differences observed between the SiC-top and -bottom in Figures 2 and 3.

One should also consider the fact that SiC is known to be thermally etched by H₂, under moderate rate (1-2 $\mu\text{m}/\text{h}$ [19]). As a matter of fact, outside the liquid, the 4H-SiC crystal is most probably etched by H₂. Consequently, the zero level of the mechanical profile taken outside of the reconstructed area is not the one of the initial substrate surface before the thermal treatment. In other words, the above-measured etching rates under liquid Si should be underestimated and one should probably add the H₂ etching rate of SiC to these values. Though the determination of such H₂ etching rate in our conditions is beyond the scope of this work, one can use the values from [19] obtained in rather close conditions. This would mean that the central dissolution rate by liquid Si at 1550°C is not zero (Figure 6) but rather of the same order as the outside etching by H₂ (1-2 $\mu\text{m}/\text{h}$). At 1600°C, this dissolution rate is slightly higher than the one of H₂ etching outside the liquid, thereby rendering it measurable.

Coming back to sample D, which displays the butterfly-like feature significantly above the substrate surface level, the 400 μm liquid Si obviously did not lead to SiC-bottom dissolution but rather to some growth. The only common thread with thinner liquid Si samples is the presence of depressions at the periphery suggesting that the above-proposed H₂ etching phenomenon is still valid at the edges. Note that the depth of these edge depressions is significantly higher for sample D compared to thinner liquid-Si samples (see Figure 4).

If growth occurs at the center of the hotter (bottom) wafer, it is against the natural vertical thermal gradient. It is known that increasing liquid Si thickness can generate the formation of convection rolls inside the liquid during SiC solution growth [20]. The thickness value considered here is

probably too low for buoyancy-induced convection, but a turbulent flow could be activated by the strong electromagnetic field inside the reactor [21][22]. Indeed, because of its high electrical conductivity, liquid Si is easily subjected to induced currents, which are responsible for electromagnetic convection. Combining the deeper edges and the central growth on the SiC-bottom wafer of sample D, we propose the following mechanism which is summarized in Figure 7. The C atoms released in the liquid at the edges by a H_2 -induced C pump may be partially redirected towards the center by an electromagnetic convection roll. The transport distance and the created C supersaturation may be sufficient to generate SiC precipitation and hence epitaxial growth far from the edges. This forced transport of C could lead to precipitation and growth on both SiC wafers. The butterfly pattern observed on sample D would then reflect the forced convection scheme that happened inside the liquid Si.

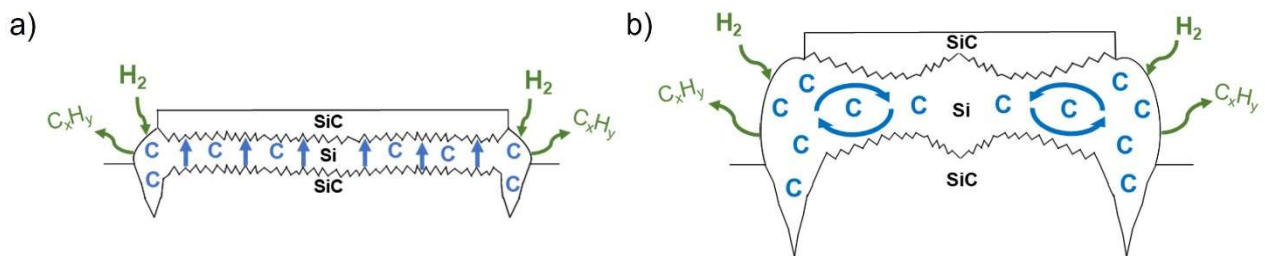


Figure 7. Schematic drawings of the proposed mechanisms occurring in both cases of a) thin and b) thick liquid Si within the 4H-SiC sandwich configuration. Circle arrows on b) represent the hypothetical direction of convection rolls.

Since the morphology of sample D is essentially attributed to epitaxial growth from the liquid phase, it can be interesting to compare with the morphology usually obtained during top seeded solution growth (TSSG). Using pure Si as liquid phase and 4° off 4H-SiC(0001) substrate, high meandering of the macro-steps is commonly obtained in the literature [23-25] while we do not see significant step meandering on sample D. Such discrepancy could originate from the key differences between this work and the usual TSSG experiments, i.e. the use of hydrogen instead of Ar and the peculiar short range dissolution/precipitation process discussed above.

Regarding the main goal of such surface structuring process (which is the formation of as large and parallel terraces as possible for being able to separate the contributions of step edges and terraces), are the terraces obtained in this work wide enough? The answer is "YES" considering the further academic work to be done on the characterization of the SiC/SiO₂ interface and fundamental understanding. Of course, considering the final application of MOSFET fabrication, the answer is

probably "NO" except maybe for specific demonstrator using unconventional fabrication routes. Wider terraces should probably be better.

Another aspect to consider together with such application is that the surface structuring has to be implemented on a n-doped epitaxial layer of the targeted MOS device without affecting the n-doping level of this epitaxial layer. It means that uncontrolled and random dissolution and precipitation of SiC over the wafers during the structuration process could be a crucial drawback. Indeed, the doping level of the grown material, which is far to be controlled in such a process, may not be adapted for fabricating a good MOSFET. In addition, the long-range roughness generated by such growth may also be detrimental to proper device fabrication. Limiting or avoiding such electromagnetic convection rolls is therefore required before going further with this sandwich configuration. Towards this end, reducing liquid Si thickness to 30 μm is efficient but the macrosteps structure is not well defined and parallel enough for being of any use. Intermediate liquid Si thickness (between 30 and 400 μm) could lead to some interesting compromise without the appearance of convection rolls. Of course, using resistance heating instead of RF heating would probably be effective for eliminating the magnetic field induced effects but such setup is not available to the authors. Beside this, the use of Ar ambiance instead of H_2 would probably allow avoiding the etching of the edges, and then limiting the amount of dissolved C atoms, resulting in less C transported within the liquid. But as stated earlier, Ar implementation is not straightforward since it leads to random gas trapping and thus unwetted areas. Finally, another way to better evaluate the mass transport occurring during the process would be to use differently doped upper and lower 4H-SiC wafers, with for instance a p-type epilayer on the top-SiC wafer before the sandwich treatment.

4. Conclusion

In this study, the development of a sandwich configuration for the simultaneous macrosteps structuring of two 4H-SiC 4° off substrates on square 1.2x1.2 cm surfaces was investigated. The entire targeted areas were homogeneously wetted by liquid Si and presented macrostepped morphologies after cooling and etching of the remaining Si. Mechanical profilometry mapping on such surfaces gave an overview of the complex processes occurring within this sandwich configuration. The formation of the obtained macro-steps results from the joint contributions of the vertical thermal gradient, H_2 etching and electromagnetic field inherent to the experimental setup. Lowering the Si amount in the stack allowed a significant mitigation of this phenomenon while leading to more disturbed macrosteps. Interestingly, the use of such a thin liquid Si led to

homogeneous and time dependent dissolution of the SiC-bottom wafer under the natural vertical thermal gradient.

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References

- [1] X. She, A. Q. Huang, O. Lucia, and B. Ozpineci, Review of Silicon Carbide Power Devices and Their Applications, *IEEE Trans. Ind. Electron.*, 64, 10, (2017), 8193–8205
- [2] G. Liu, B. R. Tuttle, and S. Dhar, Silicon carbide: A unique platform for metal-oxide-semiconductor physics, *Appl. Phys. Rev.*, 2, 2, (2015)
- [3] J. B. Casady and R. W. Johnson, Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review, *High-Temperature Electron.*, 39, 96, (1998), 511–524
- [4] K. Matocha, Challenges in SiC power MOSFET design, *Solid. State. Electron.*, 52, 10, (2008), 1631–1635
- [5] A. Chatterjee, A. Bhat, and K. Matocha, Investigation of electrically active defects of silicon carbide using atomistic scale modeling and simulation, *Phys. B Condens. Matter*, 401–402, (2007), 81–84
- [6] J. Woerle, B. C. Johnson, C. Bongiorno, K. Yamasue, G. Ferro, D. Dutta, T. A. Jung, H. Sigg, Y. Cho, U. Grossner, and M. Camarda, Two-dimensional defect mapping of the SiO₂/4H-SiC interface, *Phys. Rev. Mater.*, 3, 8, (Aug. 2019), 084602
- [7] T. Kimoto, Zhi Ying Chen, S. Tamura, S. I. Nakamura, N. Onojima, and H. Matsunami, Surface morphological structures of 4H-, 6H- and 15R-SiC (0001) epitaxial layers grown by chemical vapor deposition, *Jpn. J. Appl. Phys.*, 40, 5 A, (2001), 3315–3319
- [8] M. Camarda, A. Severino, P. Fiorenza, V. Raineri, S. Scalese, C. Bongiorno, A. La Magna, F. La Via, M. Mauceri, and D. Crippa, On the “step bunching” phenomena observed on etched and homoepitaxially grown 4H silicon carbide, *Mater. Sci. Forum*, 679–680, (2011), 358–361
- [9] I. D. P. Fiorenza, F. Iucolano, G. Nicotra, C. Bongiorno, and F. A. L. Magna, F. Giannazzo, M. Saggio, C. Spinella, and Roccaforte, Electron trapping at SiO₂/4H-SiC interface probed by transient capacitance measurements and atomic resolution chemical analysis, *Nanotechnology*, 29, 39, (2018).
- [10] M. Camarda, J. Woerle, V. Souliere, G. Ferro, H. Sigg, U. Grossner, and J. Gobrecht, Analysis of 4H-SiC MOS Capacitors on macro-stepped surfaces, *Mater. Sci. Forum*, 897, (2017), 107–110
- [11] K. Kusunoki, Y. Kishida, H. Kaido, K. Kamei, K. Seki, K. Moriguchi, and N. Okada, Development of High Quality 4H-SiC Single Crystal Wafers Grown by Solution Growth Technique, *Nippon Steel Sumitomo Met. Tech. Rep.*, 117, (2017), 49–55.
- [12] V. Soulière, D. Carole, M. Camarda, J. Woerle, U. Grossner, O. Dezellus, and G. Ferro, 4H-SiC(0001) surface faceting during interaction with liquid Si, *Mater. Sci. Forum*, 858, 0001, (2016), 163–166
- [13] X. Xing, T. Yoshikawa, O. Budenkova, and D. Chaussende, A sessile drop approach for studying 4H-SiC/liquid silicon high-temperature interface reconstructions, *J. Mater. Sci.*, 57, 2, (2022), 972–982
- [14] H. Iyer, Y. Xiao, D. Durlik, K. Danaei, L. Tafaghodi Khajavi, and M. Barati, Wettability of Carbon (C), Silicon Carbide (SiC), and Silicon Nitride (Si₃N₄) with Liquid Silicon (Si), *Jom*, 73, 1, (2021), 244–252
- [15] T. Mitani, M. Okamura, T. Takahashi, N. Komatsu, T. Kato, and H. Okumura, Control of void

- formation in 4H-SiC solution growth, *Mater. Sci. Forum*, 717–720, (2012), 57–60
- [16] K. Alassaad, V. Soulière, F. Cauwet, D. Carole, and G. Ferro, Behavior and chemical reactions of liquid Si and Ge on SiC surface, *Mater. Sci. Forum*, 821–823, (2015), 121–124
- [17] R. I. Scace and G. A. Slack, Solubility of Carbon in Silicon and Germanium, *J. Chem. Phys.*, 30, (1959), 1551–1555
- [18] K. Yanaba, M. Akasaka, M. Takeuchi, M. Watanabe, T. Narushima, and Y. Iguchi, Solubility of Carbon in Liquid Silicon Equilibrated with Silicon Carbide, *Materials Transactions*, 38, 11. 990–994, 1997.
- [19] C. Hallina, F. Owmana, A. Ellison, A. Konstantinova, and E. Janzha, In situ substrate preparation for high-quality Sic chemical vapour deposition, *ELSEVIER J. Cryst. Growth*, 181, (2024), 241–253.
- [20] F. Mercier, J. M. Dedulle, D. Chaussende, and M. Pons, Coupled heat transfer and fluid dynamics modeling of high-temperature SiC solution growth, *J. Cryst. Growth*, 312, 2, (2010), 155–163
- [21] U. Burr and U. Müller, Rayleigh-Bénard convection in liquid metal layers under the influence of a horizontal magnetic field, *J. Fluid Mech.*, 453, (2002), 345–369
- [22] Y. Tasaka, T. Yanagisawa, K. Fujita, T. Miyagoshi, and A. Sakuraba, Two-dimensional oscillation of convection roll in a finite liquid metal layer under a horizontal magnetic field, *J. Fluid Mech.*, 911, (2021), 1–24
- [23] K. Ariyawong, Y.J. Shin, J.M. Dedulle, D. Chaussende, Analysis of Macrostep Formation during Top Seeded Solution Growth of 4H-SiC, *Cryst. Growth Des.* 16 (2016) 3231–3236
- [24] Y.J. Shin, T.Y. Park, S.Y. Bae, S.M. Jeong, The effect of rotation on the macro-steps formation during 4H-SiC solution growth, *J. Korean Crystal Growth and Crystal Technology* 29(6) (2019) 294–297
- [25] S. Endo, K. Kamei, Y. Kishida, K. Moriguchi, Effects of crystalline polarity and temperature gradient on step bunching behavior of off-axis 4H-SiC solution growth, *Mater. Sci. Forum* 821-823 (2015) 26-30