Ultra-low Power Computing with CGRAs

an architecture, compilation, and application triptych

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Outline

Introduction

Mismatching energy constraints and trends

Energy constraints

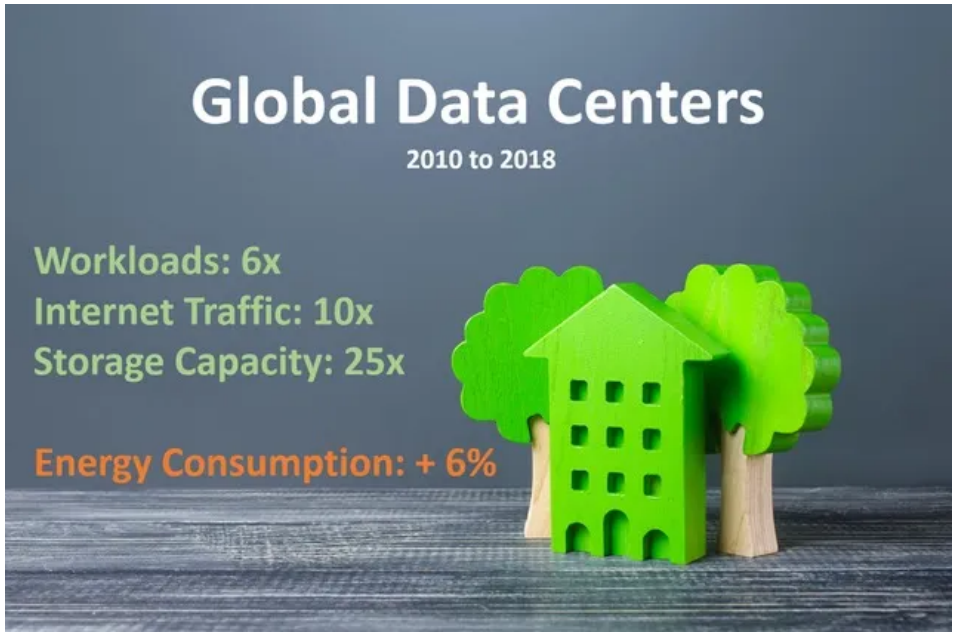
- Carbon neutral society
  - Low carbon footprint
- Battery powered devices

Energy trends

- Consume everywhere
  - Internet of (every-)Things (IoT), IoET, Industrial IoT (IIoT), fog/edge computing
- Energy hungry workloads
  - AI/ML, autonomous driving, computer vision, video streaming, etc.
- The scary figures
  - Communication technology is expected to become 21% of global electricity usage [2] (903 TWh)
  - the “Global DataSphere” will grow to 175 ZB by 2025 [51]
  - 62.7% of the total system energy, on average, is spent on data movement between main memory and the compute units [8]

Introduction

Issues and challenges



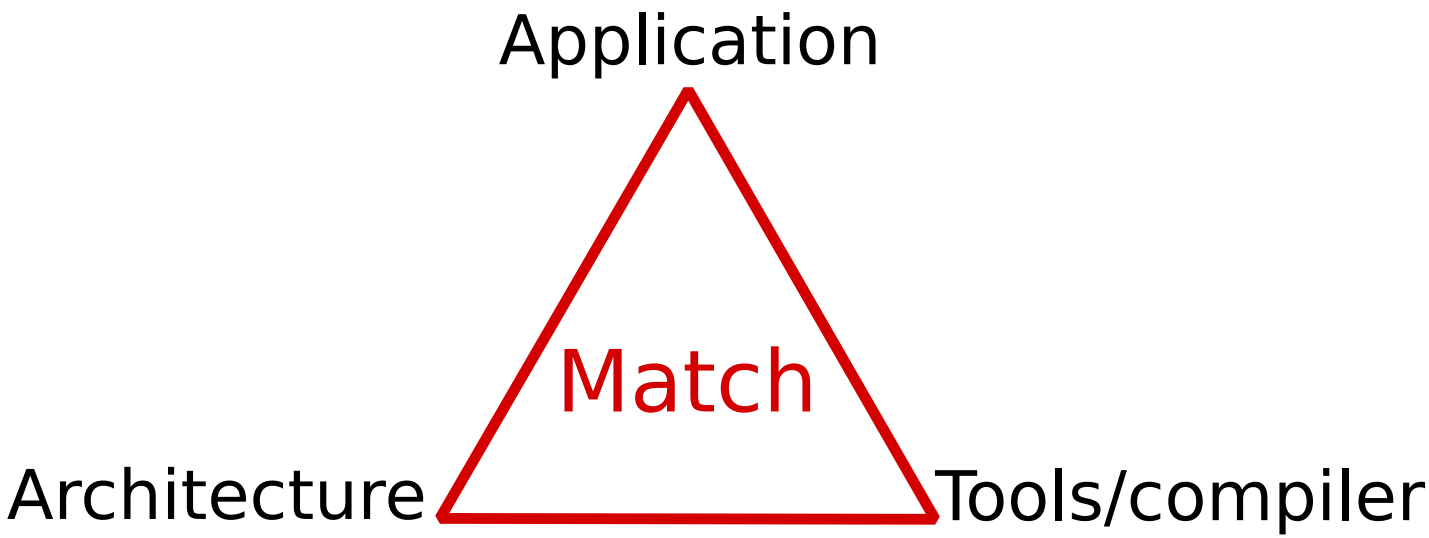
Source: https://i2.wp.com/semiengineering.com

Ultra-low-power

Energy efficient architectures for the IoT-edge-cloud computing continuum

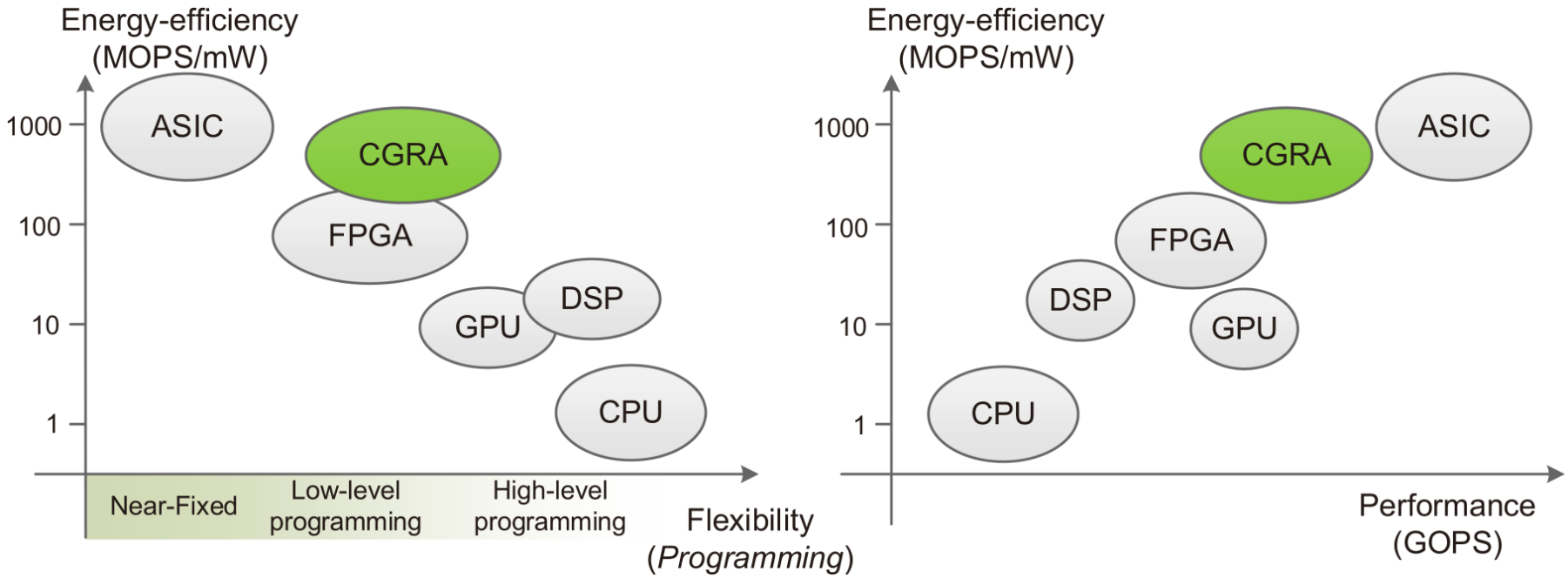
Introduction

The quest for (energy) performance



Introduction

Architectural solutions



Source: Liu et al. [39]

Coarse Grained Reconfigurable Architecture

- energy efficient solution
- trade-off performance/flexibility

Three decades of CGRA

CGRA architectures

30 years of architectures

Inventory of existing CGRAs done in [29, 56, 13, 60, 39, 48]

- Hartenstein 2001 [29]: the first decade
- De Sutter et al. 2010 [19]: book chapter
- Wijtvliet et al. 2016 [60]: 25 years of CGRAs
- Liu et al. 2019 [39]: taxonomy, classification
- Podebas et al. 2020 [48]: performance perspective

Main limitations

- Many programmed by hand (assembly level)
- Unadapted programming model
- How to efficiently make use of the available computing resources?

Three decades of CGRA

Example of CGRA

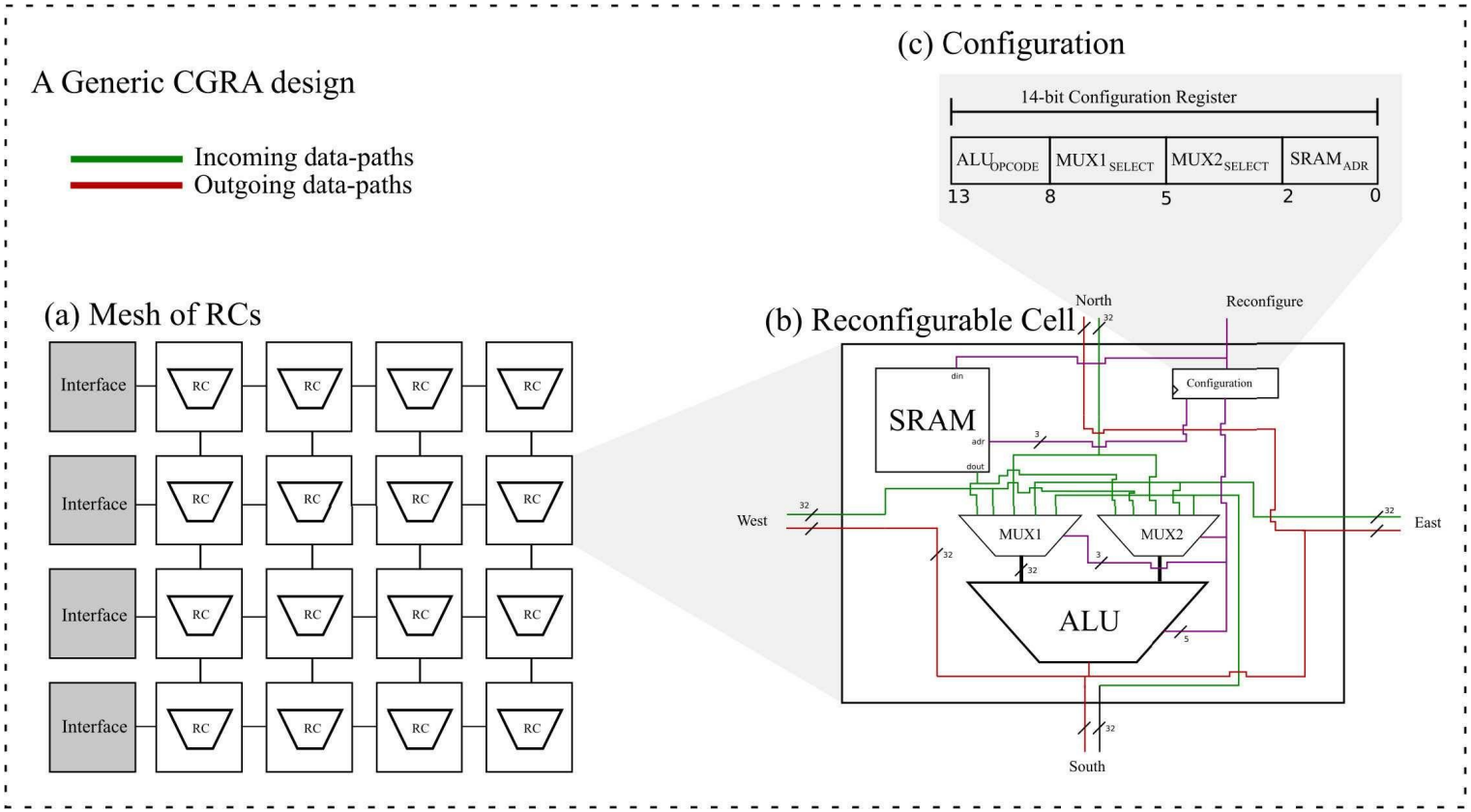


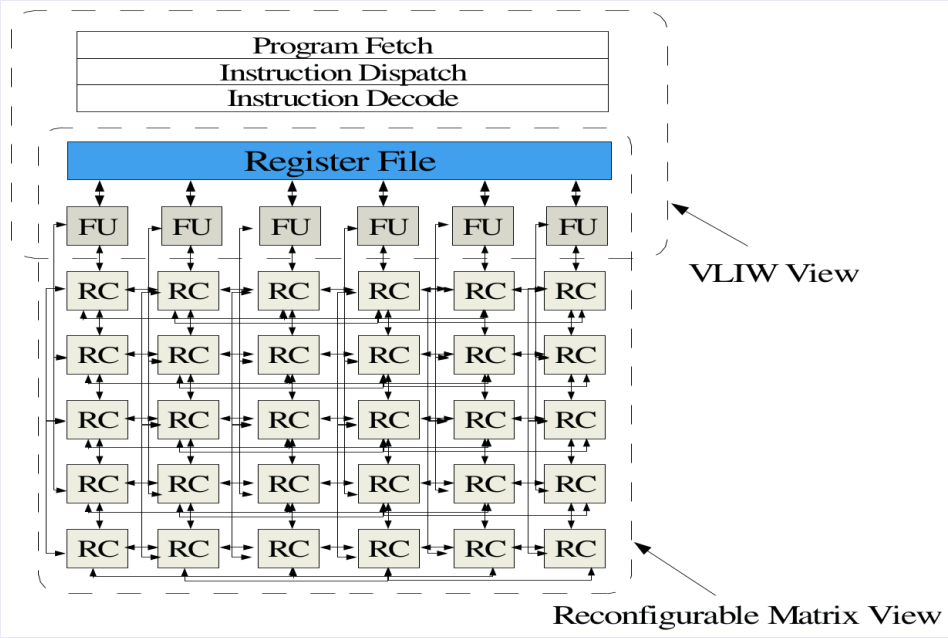
Illustration of a simple CGRA taken from [48], showing the mesh topology (a), the internal architecture of the Reconfigurable Cell, RC (b), and an example of the configuration register (c).

[48] A. Podobas, K. Sano, and S. Matsuoka. A survey on coarse-grained reconfigurable architectures from a performance perspective. *IEEE Access*, 2020.

Three decades of CGRA

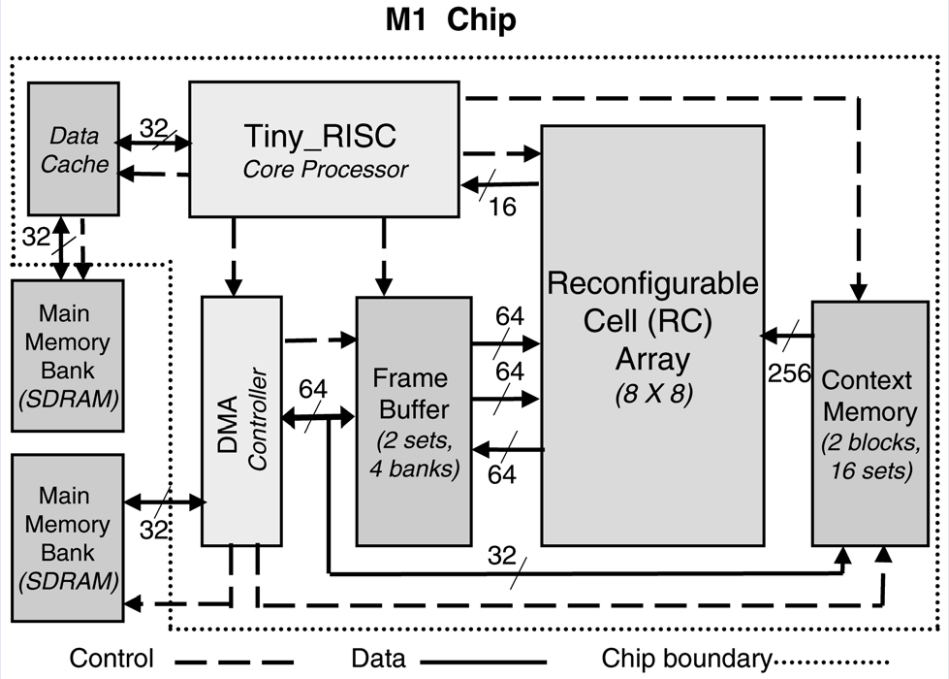
Coupling with a host processor

Tightly coupled



ADRES [42]

Loosely coupled



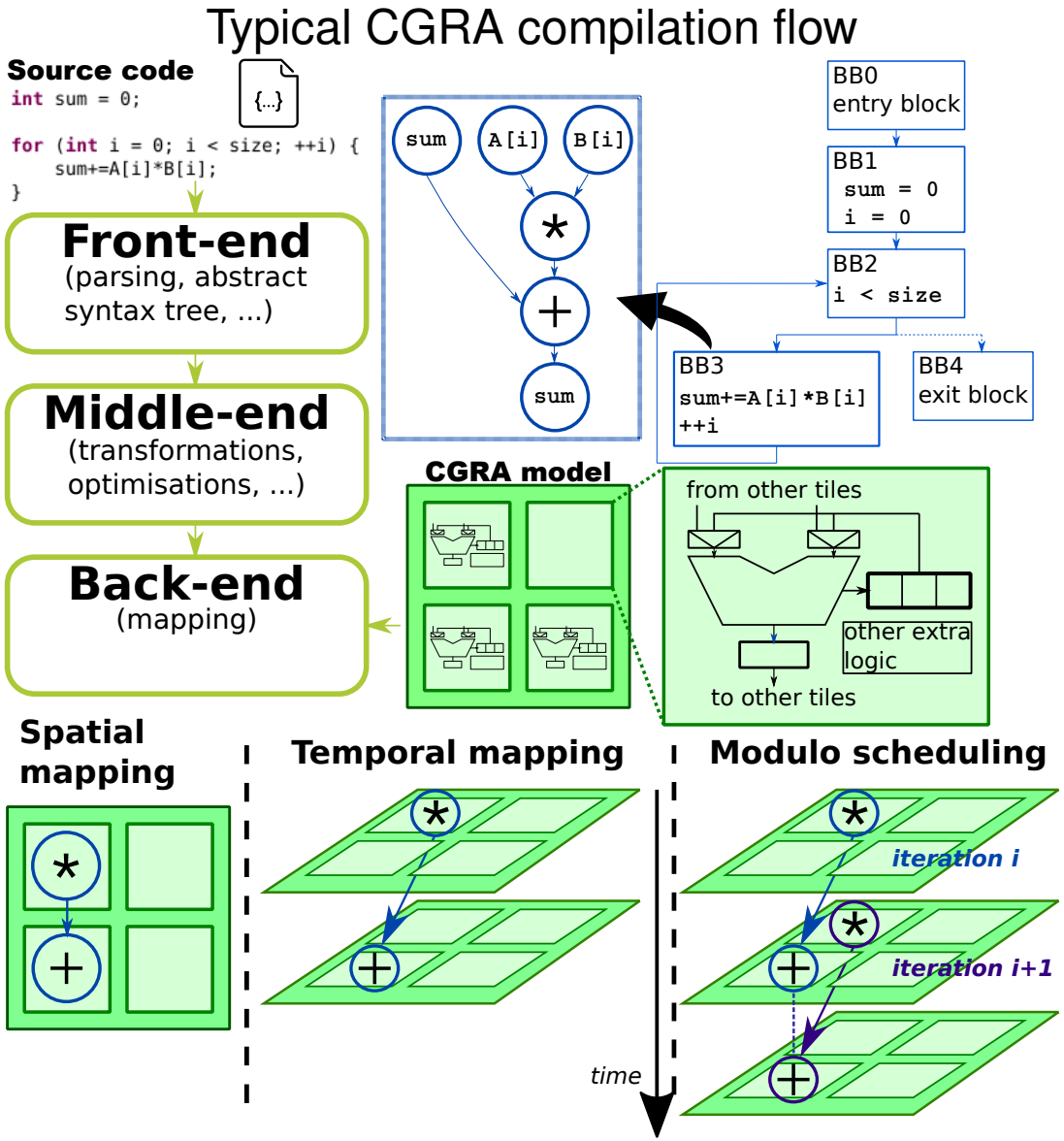
MorphoSys [53]

[42] Mei et al. ADRES: An architecture with tightly coupled vliw processor and coarse-grained reconfigurable matrix. *FPL*, 2003

[53] Singh et al. Morphosys: an integrated reconfigurable system for data-parallel and computation-intensive applications. *IEEE Transactions on Computers*, 2000.

Three decades of CGRA

CGRA mapping



Three decades of CGRA

CGRA mapping

CGRA mapping problem formulation

Bind in place and schedule in time operations of the application on the cells of the CGRA, in a short time, while guaranteeing the dependencies, such that the application executes as fast as possible

CGRA mapping problem

- Solve 2 NP-complete problems: scheduling and binding
  - + register allocation
- Mapping might fail!

	Approximate methods			Exact methods	
	Heuristics	Meta-heuristics		ILP/B&B	CSP
		Population-based	local search		
Spatial mapping	[30, 62, 37]	GA [34]	SA [58, 23]	ILP [12, 45, 62]	
Temporal mapping	[59, 7, 36, 65, 46, 18, 24, 10]		SA [40]	ILP [9] B&B [32]	CP [49] SAT [43] SMT [20]
Binding	[61, 31, 27, 47, 17, 26]	QEA [35]	SA [21, 30, 52]	ILP [25, 35]	
Scheduling	[17, 26, 35, 27, 6, 65, 52, 5]			ILP [25, 44]	

A review of binding and scheduling techniques for automated spatial and temporal mapping of applications on CGRAs.

Three decades of CGRA

CGRA mapping

Mapping if-then-else (ITE) constructs

1. Full predication [3]
2. Partial predication [11]
3. Dual-issue single execution [28, 33, 63]
4. Direct CDFG mapping [14]

Three decades of CGRA

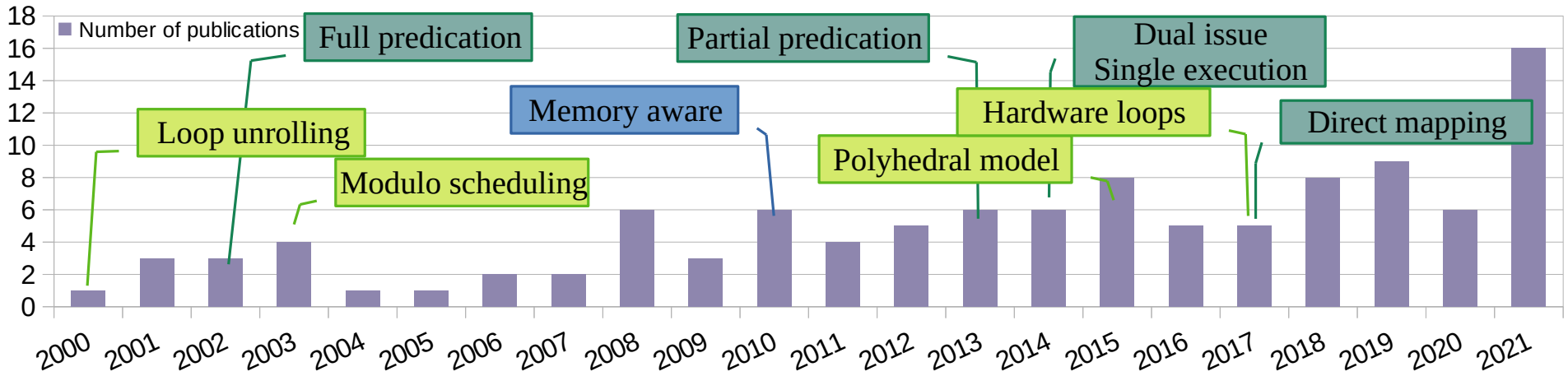
CGRA mapping

Mapping loops

1. Modulo scheduling
   - Modulo routing resource graph (MRRG) [41, 33]
   - Graph-based approaches [18, 46]
   - ILP
2. Direct CDFG mapping [14]
3. Hardware loops [4, 54, 57]

Three decades of CGRA

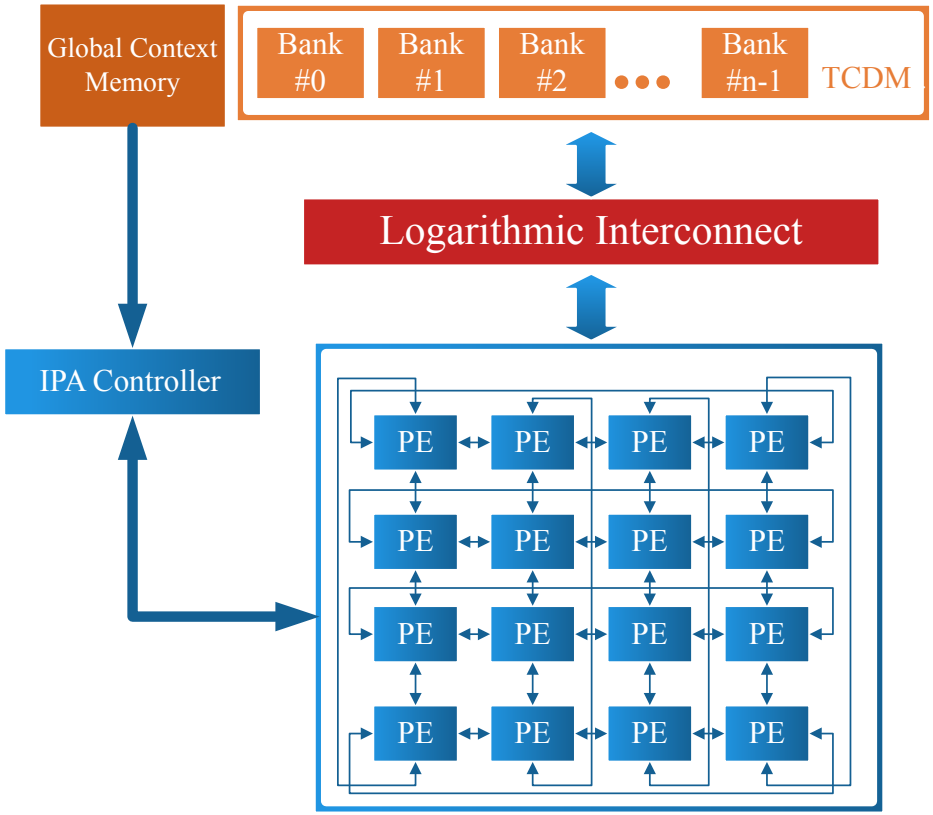
Timeline



Integrated Programmable-Array (IPA)

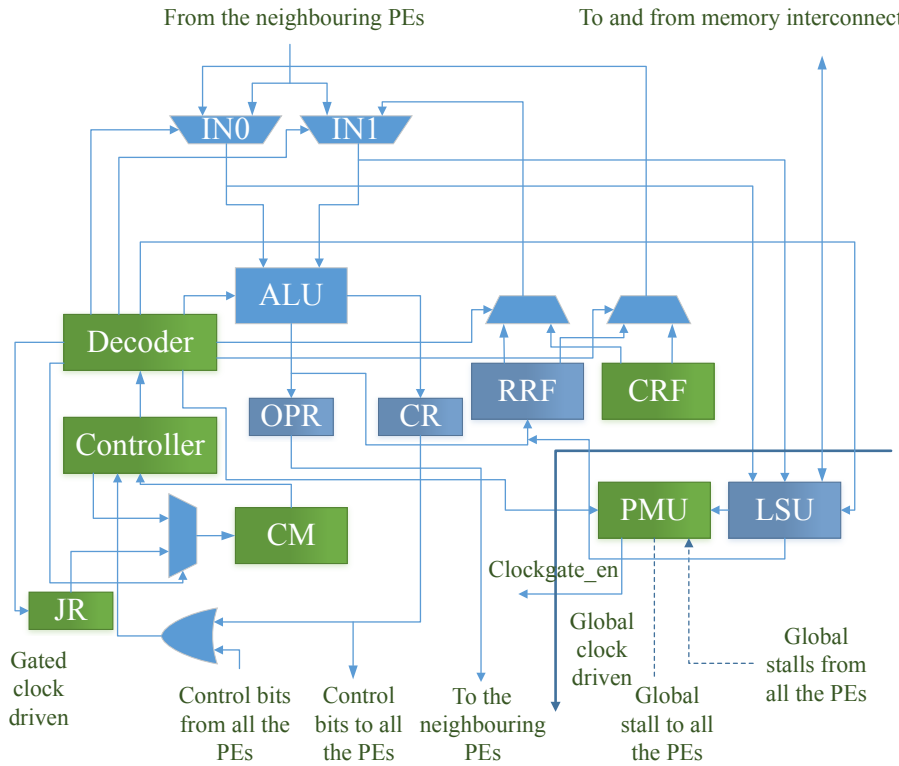
Integrated Programmable Array (IPA)

Integration with data on-chip memory



TCDM: Tightly Coupled Data Memory
PE: Processing Element

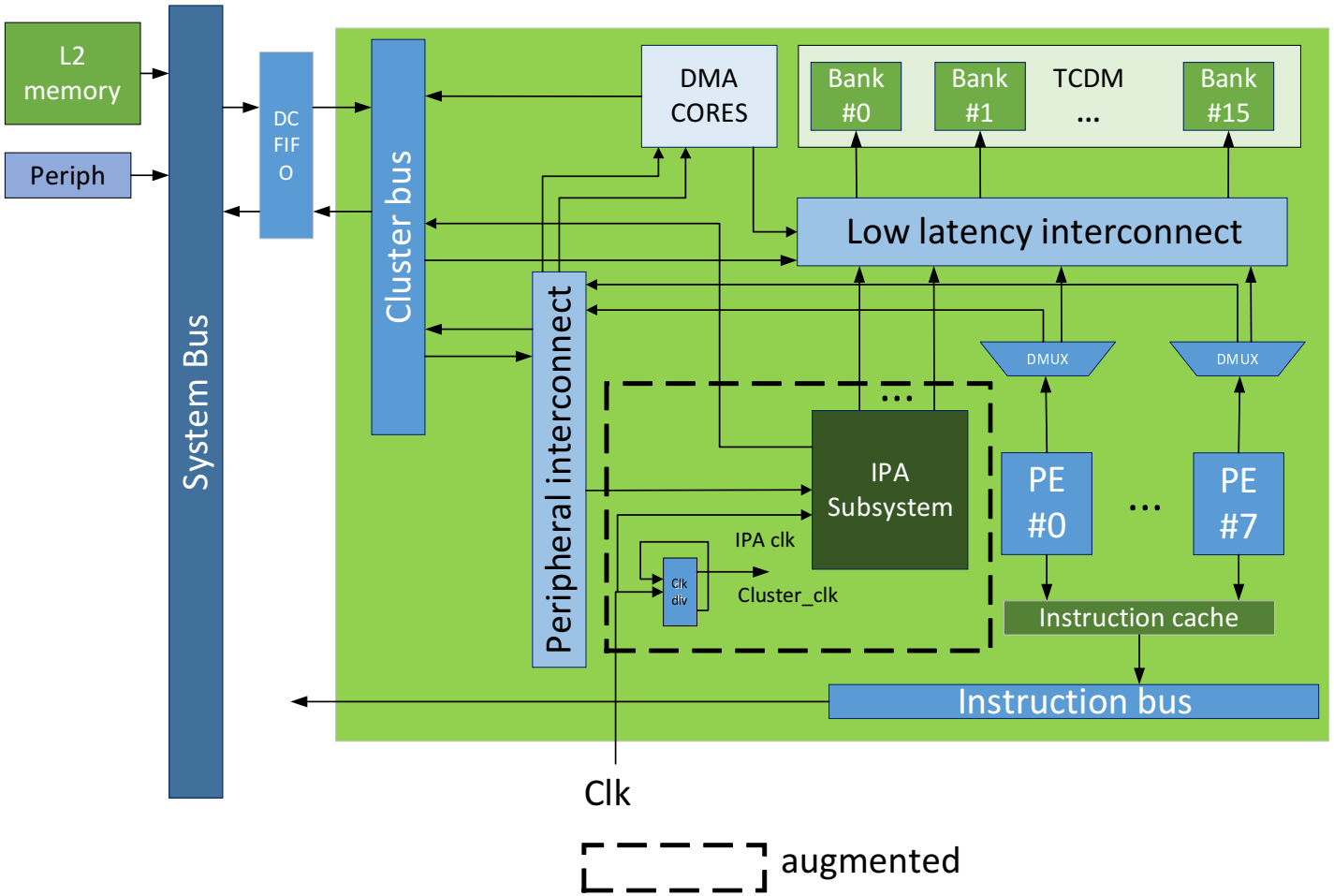
Inside a Processing Element



PMU: Power Management Unit
RRF: *Regular* Register file
CRF: Constant Register File
CM: Context Memory
OPR: Output Register
CR: Control Register

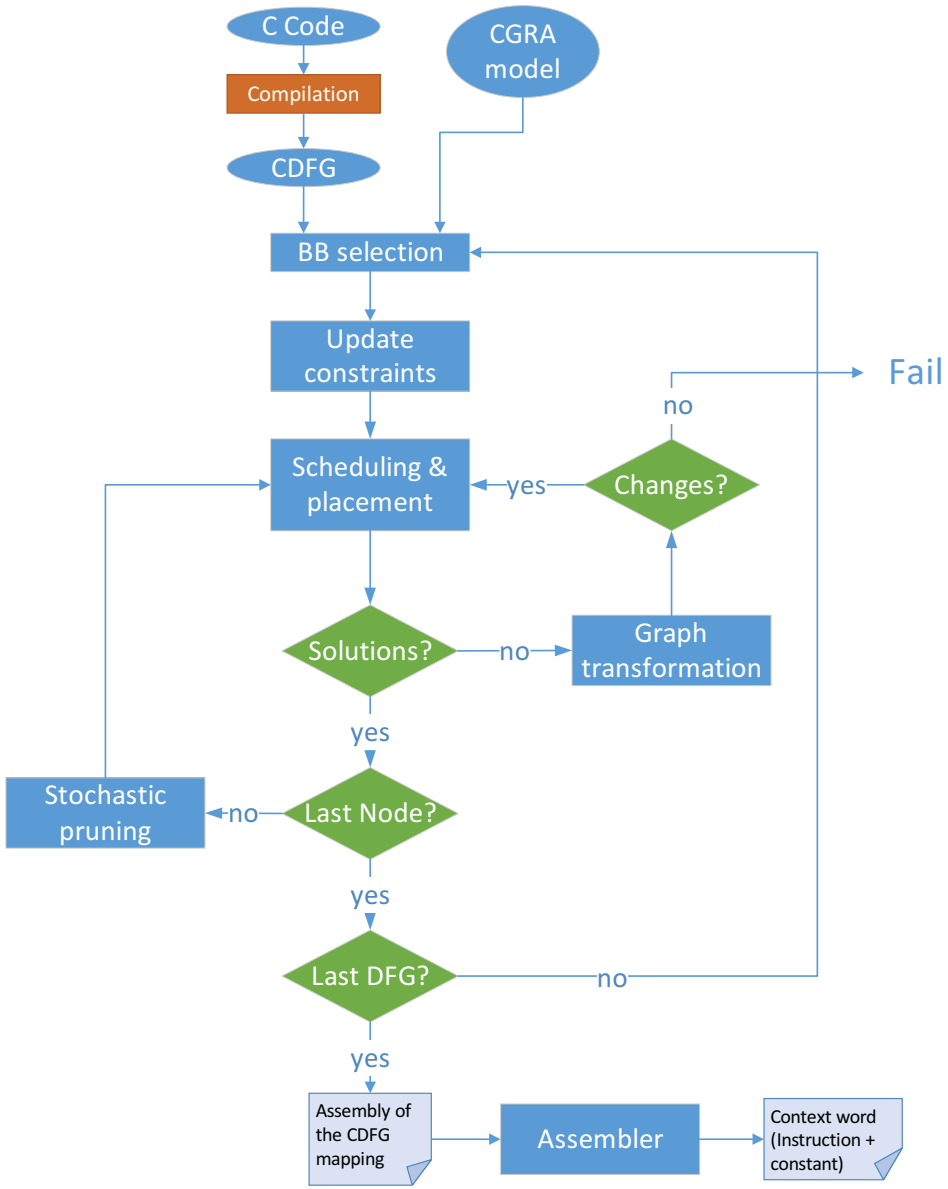
Integrated Programmable-Array (IPA)

Integration in a PULP cluster



Integrated Programmable-Array (IPA)

Compilation flow



Compilation method

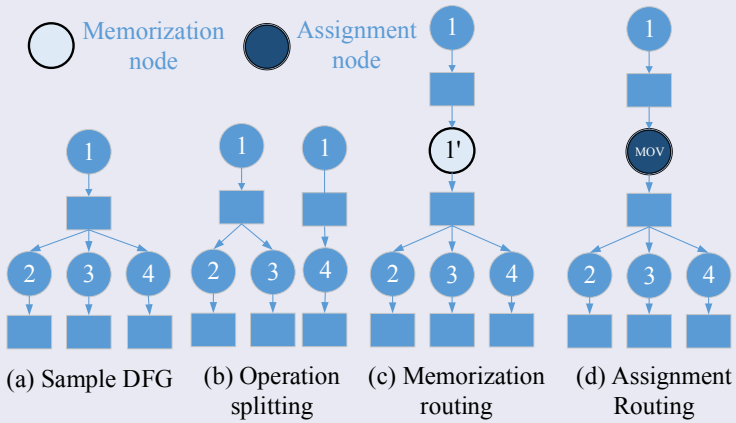
- Except array inputs and outputs, all the scalar variables are placed in the register files of the PEs
- Modified Forward traversal of CDFG to minimize the number of constraints
- Introduce routing to reach the correct variable, while mapping the basic blocks

Compilation steps

DFG mapping

- Backward traversal of operation nodes
- List scheduling based on priority (fanout)
- Partial Levi's algorithm to find common subgraphs
- Graph transformations
- Stochastic pruning
  - Keep a minimum number of partial mappings to find a complete mapping
  - Keep a maximum number of partial mappings to manage scalability

Graph transformations



Integrated Programmable-Array (IPA)

Experimental Setup

Technology and tools

- STMicroelectronics 28 nm UTBB FD-SOI
- Synopsys design compiler 2014.09-SP4
- Synopsys PrimePower 2013.12-SP3
- Questa Sim-64 10.5c

CGRA

- 4×4 array with 16 PEs
- 20×32-bit (Instructions), a 32×8-bit RRF, and 32×16-bit CRF
- 100 MHz
- clock gating

Integrated Programmable-Array (IPA)

Results

Overall instructions executed and energy consumption in IPA vs CPU [16]

Kernels		FIR	MatM (16×16)	Convolution	SepFilter	NonSepFilter	FFT	DC Filter
IPA	**Configuration cycles**	71	88	88	90	98	87	145
	Execution cycles	6 071	11 940	56 241	827 685	1 852 382	8 076	4 748
	Total number of instructions executed	44 294	110 946	531 815	7 349 843	17 486 486	76 310	28 868
	Active PEs/cycle (%)	46.1	58.5	59.2	55.5	59	59.7	39.5
	Energy (μJ)	0.022	0.043	0.202	2.98	6.669	0.032	0.017
	Energy (μJ) in non-clock-gated IPA	0.047	0.077	0.479	7.152	11.704	0.063	0.045
CPU	**Execution cycles**	37 677	96 256	616 805	5 982 730	9 084 101	164 480	50 085
	Energy (μJ)	0.132	0.337	2.159	20.94	31.794	0.576	0.175
	Speed-up	6.21x	8.06x	10.97x	7.23x	**4.9x**	**20.3x**	10.55x
	Energy-gain	6x	7.84x	10.69x	7.03x	**4.77x**	**18x**	10.29x

[16] Satyajit Das et al. *An energy-efficient integrated programmable array accelerator and compilation flow for near-sensor ultralow power processing*, IEEE TCAD, 2019.

Integrated Programmable-Array (IPA)

Results

Performance evaluation in execution time (ns) for different configurations in the heterogeneous platform [15]

Kernels	Data size (KB)	Single-core (ns)	Multi-core (ns)	Speed-up in multi-core (x)	IPA (ns)	Speed-up in IPA (x)
MatMul	8	3,358,740	435,180	7.72	432,630	7.76
Conv	8	9,733,380	1,520,840	6.4	1,494,860	6.51
FFT	1	767,640	142,720	5.38	94,510	8.12
FIR	0.84	182,500	33,460	5.45	33,410	5.46
Sep Filter	10	39,870,420	6,404,160	6.23	6,334,700	6.29
Sobel Filter	10	117,024,880	40,894,260	2.86	28,865,890	4.05
GCD	0.01	2,951,160	2,951,160	1	61,1300	4.83
Cordic	0.06	9,000	7,000	1.29	3,610	2.49
Manh Dist	8	244,640	164,640	1.49	70,300	3.48

[15] Satyajit Das et al. *A heterogeneous cluster with reconfigurable accelerator for energy efficient near-sensor data analytics*, ISCAS, 2018.

Integrated Programmable-Array (IPA)

Results

Energy consumption evaluation in μ J for different configurations in the heterogeneous platform [15]

Kernels	Single-core	Multi-core	IPA	
			Energy	of Active PEs/cycle
MatMul	1.247	0.313	0.208	58.5
Convolution	2.876	1.095	0.658	59.2
FFT	0.292	0.087	0.042	59.7
FIR	0.08	0.026	0.026	46.1
Separable filter	16.663	4.611	4.28	55.5
Sobel Filter	51.491	29.444	12.701	51.2
GCD	1.151	1.151	0.257	6.25
Cordic	0.004	0.003	0.001	50
ManhDistance	0.1	0.095	0.03	48.5

[15] Satyajit Das et al. *A heterogeneous cluster with reconfigurable accelerator for energy efficient near-sensor data analytics*, ISCAS, 2018.

Integrated Programmable-Array (IPA)

Comparison with state of the art architectures

	Ultra-low-power CGRAs			High-performance CGRAs			
	ULP-SRP [34]	**CMA [55]**	**IPA [17]**	**HyCube [33]**	**Revel [75]**	**SGMF [71]**	**SNAFU**
Fabric size	3×3	8×10	4×4	4×4	5×5	8×8 + 32 mem	N×N (6×6 in SNAFU-ARCH)
NoC	Neighbors only	Neighbors only	Neighbors only	Static, bufferless, multi-hop	Static & dynamic NoCs (2×)	Dynamic routing	Static, bufferless, multi-hop
PE assignment	Static	Static	Static	Static	Static *or* dynamic	Dynamic	Static
Time-share PEs?	Yes	Yes	Yes	Yes	Yes	Yes	No
PE firing	Static	Static	Static	Static	Static *or* dynamic	Dynamic	Dynamic
Heterogeneous PEs?	No	No	No	No	Yes	Yes	Yes
Buffering (approx.)	—	—	188 B / PE	272 B / PE	≈1 KB / PE	≫1 KB / PE	40 B / PE
Power	22 mW	11 mW	3–5 mW	15–70 mW	160 mW	20 W	<1 mW
MOPS/mW (approx.)	30–100	100–200	140	60–90	60	60	305

Table I: Architectural comparison of SNAFU to several prior CGRAs.

Taken from [23]

[23] Gobieski et al. Snafu: An ultra-low-power, energy-minimal cgra-generation framework and architecture. *ISCA*, 2021

Integrated Programmable-Array (IPA)

IPA features

- Architectural support
  - PMU: Power Management Unit
  - CRF: Constant Register File
  - Global synchronization
  - ISA-based configurations (20/21-bits)
- Compiler
  - Direct CDFG mapping (register allocation approach)
  - Backward traversal of operation nodes
  - List scheduling based on priority (fanout)
  - Partial Levi's algorithm to find common subgraphs
  - Dynamic Graph transformations
  - Stochastic pruning

Summary

IPA: Integrated Programmable Array

- Ultra-low power domain
- Integer operations
- CDFG support

TRANSPIRE: transprecision and SIMD support

- Floating-point operations
- Multi-cycle operators

Perspectives

CGRA

- Still ever promising approach?
- New momentum
  - Xilinx AI engine
  - Reconfigurable Dataflow Architecture/Accelerator (RDA)

Embedded systems

- Small grids (4x4, 5x5, 6x6)
- Temporal mapping
- (Ultra) Low Power

HPC systems

- (Very) Large grids (100s to 1000s of cells)
- Spatial mapping
- HPC: High Power Consuming

Perspectives

CGRAs for AI

Artificial Intelligence (AI) applications

- Xilinx AI-engine [22]
- Reconfigurable Dataflow Architecture [50]
- Reconfigurable Dataflow Accelerator [64]

Scalability challenge

AI for CGRAs

- Machine learning to optimize the mapping [38]
- Single model: functional + non functional contraints

CGRA + emerging memory technologies and organisations

- MRAM, FeRAM, ReRAM, PCM, ...
- Computing in/near memory

Open-source frameworks

- DSAGEN [58]
- OpenCGRA [55]
- CGRA-ME [1]
- CCF

THANK YOU

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