# Adaptation of a solid-state-Marx modulator for electroactive polymer

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***Abstract*— Electroactive polymers show promising characteristic such as lightness, compactness, flexibility and large displacements making them a candidate for application in cardiac assist devices. This revives the need for quasi- square wave voltage supply switching between $0$ and several kilo-Volts, that must be efficient, to limit the heat dissipation, and compact in order to be implanted. The high access resistance, associated to compliant electrodes, represents an additional difficulty. Here, a solid-state Marx modulator is adapted to cope with electroactive polymer characteristics, taking advantage of an efficient energy transfer over a sequential multistep charge/discharge process. To ensure compactness, efficiency as well as the needs of an implanted device, a wireless magnetic field based communication, and power transfer system has been implemented. This work demonstrates the benefit of this design through simulations, and experimental validation on a cardiac assist device. At a voltage of $7$ kV, an efficiency of up to $88\%$ has been achieved over a complete charge/discharge cycle.**

## I. Introduction

Recent trends in electroactive polymers pose new challenges to the accompanying power electronics. In a dielectric elastomer actuator (DEA), a hyperelastic material is sandwiched between two compliant electrodes. When a voltage is applied, the electrostatic force squeezes the film reducing its thickness, while expanding its area. DEAs show a high-energy conversion density (i.e. up to $1\,\mathrm{J\,cm^{-3}}$), with an electromechanical response reaching $100\,\%$ deformation [1]. Thanks to their unique characteristics and their softness, they have been used to augment the role of the aorta and bring up to $5\%$ of cardiac assistance [2]. Unfortunately, the amplifier used in [2] is falling short of the portability need. Indeed, only a compact (i.e. low volume), and efficient converter coping with the following challenges will unlock the full DEAs' potentialities:

- a typical DEA, cyclically switches from $0$ to $7$ kV and vice-versa. Thence, because it consumes only $120$ mW in average, mastering the parasitic capacitance losses in the converter is a key challenge;
- as only $20\,\%$ of the energy transferred during the capacitor charge process is converted to the mechanical side [3], the remaining energy need to be recovered in order to improve the overall efficiency;
- the charge/discharge current must be constant in order to minimize the energy dissipated within the relatively high access resistance associated to electrodes flexibility [4], [5].

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The main focus of this work is on showing the benefits of using a solid-state-Marx modulator coupled with a last generation DEA in the framework of biomedical applications. That is why, rather than the converter efficiency for a fixed output voltage, we study the overall efficiency of the converter-DEA chain (mechanical output over the energy supply to the converter) over a full charge/discharge cycle.

In addition, we shall present a design where the converter powering is wireless, a rather relevant issue to improve the functionality of a biomedical implant in order to avoid batteries replacement surgery, and the risk of infections it entails. Lastly, we shall address inrush currents avoidance, a major issue to improve the carbon based DEAs' electrodes lifespan.

DEA supplies hitherto have been designed based on the half-bridge, the flyback and the multilevel converter. Half-bridge bidirectional converters [6] and bidirectional flyback [7], both based on a $4.5$ kV stacked MOSFETs, have been demonstrated up to $16$ kV and $7.5$ kV respectively. However, in case of low-power devices, the inductance, and switches parasitic capacitance losses are drastically reducing the overall efficiency, down to about $15\%$ [8], [9], [6]. Besides, the design of the inductors [8], [7], [6] mostly lead to a bulky element with a volume up to $20$ times the one of the DEA. Moreover, overcoming the limit of the switch with stacked MOSFETs in order to fit the low parasitic capacitance and low current leakage entails a pretty relevant volume increase [6], [7].

Another major shortcoming of the flyback is the sharp and pulsatile output current, falling short of the DEAs' need for a nearly constant current. Tackling this issue by improving the current profile with a filtering capacitance entails a further increase in terms of volume, and of the amount of energy that needs to be transferred back and forth. Within the context of low power and high voltage DEAs, the parasitic capacitances represent a major hindering towards the realization of a compact and efficient design, limiting the half-bridge, and flyback suitability .

Modular multilevel DC-DC converters overcome the semiconductors high-voltage limitations. High voltage output (above $10$ kV) with an overall efficiency estimated around $50\%$ have been successfully used in the kilowatts range, where the energy required by the isolated driving circuit becomes negligible [10], [11]. The solid-state Marx modulator ($S^2M^2$) represents an alternative multi-level method [12], [13]. In this case, the levels are linked in series, each having the energy stored in the level-capacitor that is charged only when levels are switched in parallel (rather than by supplied with an isolated DC-DC converter). $S^2M^2$s are

commonly adapted in many applications, however at the best of our knowledge, no study has been devoted to their use for charging/discharging DEAs. Perhaps this is due to the two following issues that may represent a hindrance to their use for low power DEA: first, the commonly used single high-voltage steps, can entail pretty high inrush currents drastically lowering the efficiency (30% at best), or damaging, even destroying the DEAs; second, the isolated driving circuit is complex, bulky and energy consuming. Nonetheless, the energy sent back by the DEA at the discharge, that is most of the energy transferred, can be recovered recharging the level-capacitors, and the cyclic DEA's working allows to complete the level capacitor recharge with a single and compact diode, two pretty relevant advantages over all the above cited method indeed.

In this work, a solid-state Marx generator, shown in Fig. 1, is adapted, to supply a low power (120 mW), and high voltage DEA, reaching an overall efficiency of 88%, and a voltage up to 12.5 kV. In order to cope with the two aforementioned issues, we present a twofold adaptation. First, we get rid of the single voltage step by delaying the activation/deactivation of each stage, making the charge/discharge process a sequence of successive steps. This is a way to get close to a low-loss constant-current charge/discharge process limiting, at the same time, the losses in the parasitic capacitance. Second, the implementation we propose, uses a single magnetic field to supply and command the levels (i.e. a wireless powering, and control system) improving the compactness, and reducing the energy consumption of the isolated driving circuit.

The paper is organized as follows: the next two sections, II and III, are devoted to the two adaptation strategies mentioned above implemented on a 24 levels modified Marx generator. In section IV numerical and experimental results on the prototype demonstrate the benefit of our architecture in terms of efficiency and compactness. The last section assesses different sources of losses and the role of the level capacitance, pinpointing design guidelines to improve the device efficiency.

In this study, the complex electromechanical model of the cardiac assist DEA in Fig. 1 is mimicked by the linear elements depicted in Fig. 2, with an access resistance $R_a = 22$ kΩ, a capacitance $C_{DEA} = 4.7$ nF. The resistance $R_p = 200$ MΩ emulates the energy converted by the cardiac assist device [2]. Eventually, the modified Marx generator is validated on a real DEA.

## II. Adapted Marx generator: from single to multistep charging and discharging

A solid-state Marx modulator is made of $N$ levels. As shown in Fig. 2, each level $k$, with $k = 1, 2, 3...N$, is composed by a capacitor $C_k$, a diode $D_k$, and two MOSFETs (i.e. the high side and low side transistors $HS_k$ and $LS_k$ respectively). When the $LS_k$ are on and the $HS_k$ are off, the capacitors are connected in parallel. In the opposite configuration, the capacitors are connected in series.

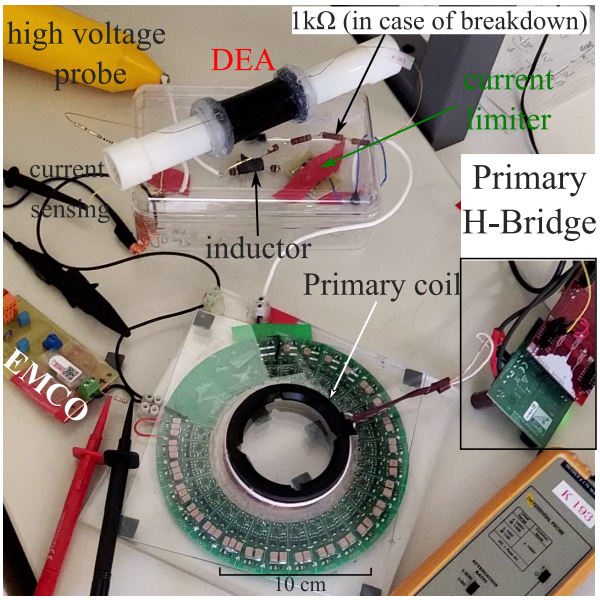


Fig. 1: Adapted Marx modulator connected to the DEA jointly with the current limiter, the inductor, an additional 1 kΩ resistance to limit the current in case of breakdown, a 560 Ω for current sensing, a high voltage probe, a high voltage source producing $V_1$ (EMCO), and the primary coil with its H-Bridge.

When levels are in parallel, their level-capacitors are charged through the diode and the current source generator connected to $V_1$. When they are all in series, a high voltage is achieved and the energy available is limited. Nonetheless, the cyclic working principle of the DEA offers the opportunity to recharge the capacitors after each cycle.

The cardiac assist cycle with a period $t_p$ of one second, consists of four stages:

1) the DEA stays at zero voltage during the diastole (i.e. half a second);
2) a fast (i.e. 50 ms) DEA charge;
3) the DEA is kept at high voltage during the systole (i.e. half a second);
4) a fast discharge (i.e. 50 ms);

thence, the converter must follow the same sequence.

**Stage 1** - The DEA stays at zero voltage, all the $LS_k$ MOSFETs are on, while all the $HS_k$ are off (frame ① in Fig. 3). The level-capacitors $C_k$ (k = 1, 2...,N) complete their recharge from the current source $I_s$, and through the diodes $D_k$ (k = 1, 2...,N).

**Stage 2** - It starts at time $t = t_{up}$ when all the $LS_k$ MOSFETs are turned off. Afterwards, the $LS_k$ MOSFETs are sequentially turned on, $HS_1$ at time $t = t_{up} + t_s$, $HS_k$ at $t = t_{up} + kt_s$ (frames ②, and ②′ in Fig. 3 show the levels at $t = t_{up} + t_s$, and $t = t_{up} + 2t_s$ respectively), up to $HS_N$ that is turned on at time $t = t_{up} + Nt_s$. This makes the process of connecting in series the level capacitors $C_k$ a sequence of $N$ voltage steps $V_i$ (see Fig. 3), each lasting a time $t_s$. Thence, the total charge at time $t_{up} + kt_s$ is:

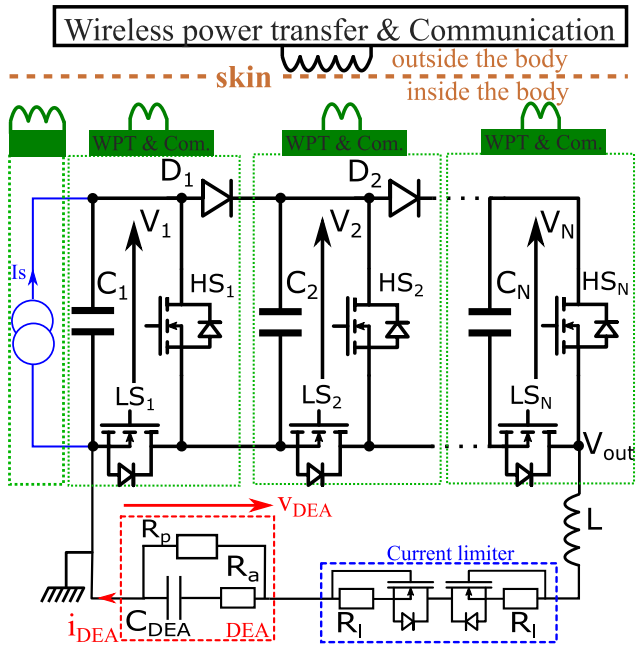


Fig. 2: The modified solid-state Marx generator, each level $k$, with $k = 1, 2, ...N$, can be charged up to a tension $V_k$. The level $k$ is composed by the MOSFETs $HS_k$ and $LS_k$, the diode $D_k$ and the capacitor $C_k$. In green the wireless power transfer (WPT) and its integrated communication (Com) used to supply and drive the MOSFETs, in blue the current limiter, in red the DEA and the generator in blue supplies the first stage $V_1$.

$$V_{out}(t_{up} + kt_s) = \sum_{i=1}^{k} V_i(t_{up} + kt_s). \quad (1)$$

**Stage 3** - The DEA is kept at high voltage and all the $HS_k$ MOSFETs stay on (frame ③ in Fig. 3). Because of the energy converted by the DEA, $V_{DEA} = V_{max}$ just after the charge, and goes down to $V_{DEA} = V_{min}$ just before the discharge. This voltage drop $\Delta V_{DEA} = V_{max} - V_{min}$, is kept as small as possible through an additional charge transfer from the level capacitors towards the DEA, taking place all along the stage 3.

**Stage 4** - The discharge of the DEA starts at time $t = t_{down}$, where all the $HS_k$ MOSFETs are off; at time $t = t_{down} + t_s$ the MOSFET $LS_N$ is set on, $LS_{N-1}$ is set on at $t = t_{down} + 2t_s$, $LS_{N-k+1}$ is set on at $t = t_{down} + kt_s$, till reaching time $t = t_{down} + Nt_s$ where $LS_1$ goes on, and the full discharge has been carried out (frames ④, and ④′ in Fig. 3 show the configuration at $t = t_{down} + t_s$, and $t = t_{down} + 2t_s$ respectively). Similarly to the charge process, the discharge takes place through a series of voltage steps $V_i$ with an output voltage at time $t = t_{down} + kt_s$ given by the following expression:

$$V_{out}(t_{down} + kt_s) = \sum_{i=1}^{N+1-k} V_i(t_{down} + kt_s). \quad (2)$$

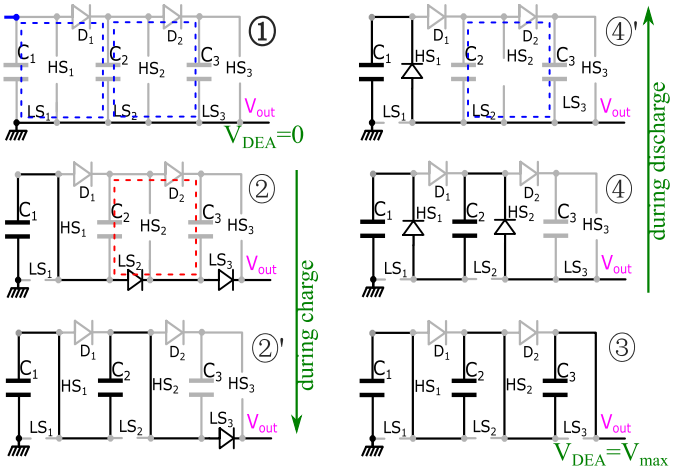


Fig. 3: Evolution of the structure where the frame number shows the different stages and with $N = 3$. ②, shows stage 2 at time $t = t_{up} + t_s$, and ②′ at time $t = t_{up} + 2t_s$. ④ shows the discharge stage at time $t = t_{down} + t_s$, and ④′ at time $t = t_{down} + 2t_s$. MOSFETs body diode are represented only when they are relevant. The dashed rectangles highlight different recharge mechanism of the level capacitor and are discussed later.

In the standard Marx generator, the $N$ stages are switched at the same time, resulting in a unique voltage step. On the contrary, in our adapted Marx generator, the overall tension change is split into a sequence of minor steps, each delayed of $t_s$ with respect to the previous one. The delay decouples the current response in order to reduce the inrush current and the Joule losses in the access resistance $R_a$. Moreover, because the load (i.e the DEA) behaves as a capacitor, during the DEA-charge the level-capacitors $C_k$ are only partially discharged. Consequently, during the DEA-discharge, the level-capacitor voltages are partially restored. This energy recovering is a key feature to take advantage of, in order to achieve a higher efficiency.

During charge (discharge), each time a level $HS_k$ ($LS_k$) is activated, a current peak is produced. This current can be an issue for the DEA, and must be kept below a threshold of about 1 mA. This has been achieved through a depletion MOSFET-based current limiter (BSP135 from Infineon with $R_l = 820\ \Omega$) connected in series with the load, as shown in Fig. 2. The step voltage reduction that arises from the adapted Marx generator, makes possible the use of a current limiter which withstand only a fraction of the voltage applied to the DEA, the $V_{DS}$ breakdown being 600 V.

## III. Adapted Marx generator: a low power and compact implementation

In the previous section, we presented the general principle of the modified $S^2M^2$ jointly with some key advantages of the proposed principle. Here we shall focus on the details of the 24 levels prototype emphasizing its design compactness, as well as the reduced consumption of its electronic components, two features of the utmost relevance to get the device

suitable to be used as a biomedical implant.

Since the 24 levels are at different voltage potentials, the control signal and the power of each level need to be insulated. Indeed, the use of optical or magnetic isolators for each level would be dramatically volume and energy consuming (i.e. few milliwatts per level) for an implanted low-power device. In order to keep them low, the magnetic field of the wireless power transfer (WPT), used to supply the implanted device, has been used, at the same time, to control the signal and the energy of the levels.

In what follows the adopted design is presented in detail and a general view of the implementation is shown in Fig. 4.

A full-bridge at the top of Fig. 4 produces a 1 MHz square wave which is switched on/off to provide an amplitude-modulated voltage. The resulting triangular current (i.e. 2 A amplitude) is injected in a two-turns primary coil (black coils in Fig. 4), made of Litz wire, that couples with the 24 single-loop, 80 $\mu$m diameter, polyurethane enameled, secondary coils (green in the Figure). The secondary coils are stacked and encapsulated in silicone (Sylgard 184 from Dow - Fig. S1 S2 in the supplementary). About 2 cm separate the primary from the secondary coils allowing to carry out the energy, and communication keeping the former outside the body, while the latter are implanted under the skin.

A compact but unregulated DC-HVDC converter (A06P-5 from EMCO) provides the energy of the first level (Fig. 4). The converter is active only when all the level-capacitors are in parallel (i.e. between $t_{down}$ and $t_{up}$), and it has been experimentally checked that, when active, it behaves as a constant current source.

The levels are then disposed circularly with the coils inserted in the middle, as shown in Fig. 5.

On each level, the Schottky diode, $R_{dem}$ and $C_{dem}$, demodulate the binary amplitude-shift keying, while the asynchronous-receiver module of the microcontroller $\mu C$ (ATtiny 406 from Microchip) decodes the frames. The 0b01010101, and 0b01010111 trigger the charge and discharge processes, respectively. The second Schottky diode, and $C_{dec}$, provide the energy to supply the $\mu C$. The field on the primary coil is directly adjusted to get a 5 V supply.

The $\mu C$ allows a pretty compact design. Within a volume $3\times3\times0.9$ mm$^3$, it decodes the frame, and directly drives the MOSFET thanks to its 5 V output, to the 100 mA sink/source current per pin group, and to the low gate voltage threshold of the transistors (i.e 1.9 V). It is worth noting that the use of a single and small MOSFET (BSS225 from Infineon) is made possible thanks to the step voltage reduction provided by the architecture. The maximum voltage on a level is limited by the MOSFET breakdown voltage 600 V, which gives the opportunity to reach 12.5 kV as checked experimentally.

In addition, the $HS_k$ and the $LS_{k+1}$ have their source terminal at the same potential (colored background in Fig. 4), allowing to drive them with the same $\mu C$. The level-capacitors, $C_k$, are made of several (up to three) 1 $\mu$F 2020 X7R multilayer ceramic capacitors in parallel (from Knowles Syfer). They provide a high energy-density with a minimum current leak, but they have a time dependent

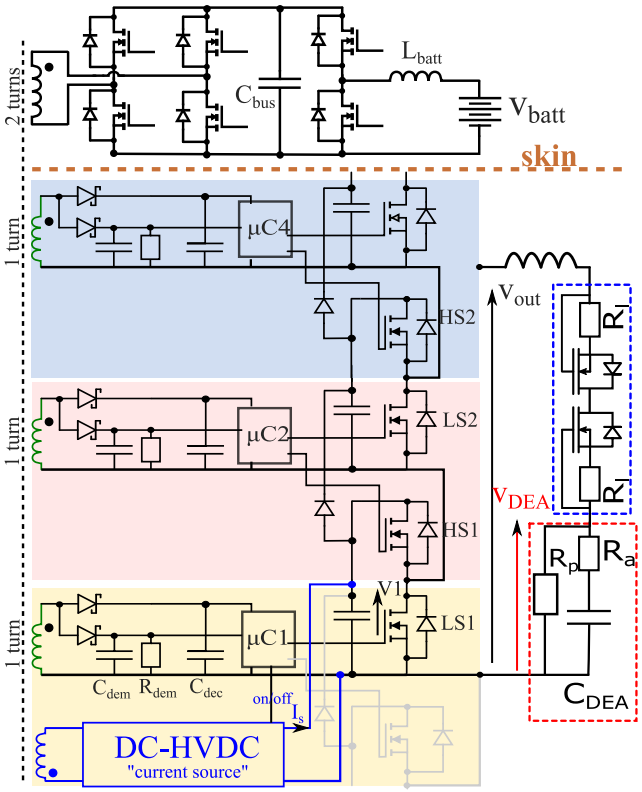


Fig. 4: Schematic of the circuit used to implement the 24 levels $S^2M^2$. At the top, the circuit used to drive the emitting coil is represented. All the components laying below the orange dashed line are part of the implanted device. Three levels are sketched; the background color is used to highlight components driven by the same $\mu C$. The red dashed box contains the DEA, while the current limiter lies within the blue dashed box. The blue DC-HVDC, at the bottom, represents the voltage input of the modified Marx generator.

and non-linear behavior. The effective capacitance is reduced down to 0.4 $\mu$F (at 300 V) with an equivalent leakage resistance of 3 G$\Omega$ (after 60 s). The effective level-capacitors are organized in the following way: $C_k = 1.2$ $\mu$F for $k \in [1,7]$, $C_k = 0.8$ $\mu$F for $k \in [8,19]$, and $C_k = 0.4$ $\mu$F for $k \in [20,24]$.

## IV. Experimental and Numerical Results

In this section, the measurements performed on the prototype presented in this work are compared with numerical simulations of the adopted setup. The working conditions have been chosen to fit the DEA's applications of interest here (i.e. biomedical implants). Hence: $t_{up} = 0.2$ s, $t_{down} = 0.7$ s, $t_s = 2$ ms, the current limiter is set at 1.1 mA and $V_1 \approx 320$ V. The resistance mimicking the DEA is a voltage probe (Cal Test CT4026 ) with $R_p = 200$ M$\Omega$ and $C = 4.7$ nF of plastic capacitor (30 kV Styroflex capacitor). The 50 mH inductor $L$ allows a zero current switching and still leads to a $RLC$ aperiodic current response. The current and voltage in the supply are measured with a digital multimeter (keysight 34465A), while the current and voltage

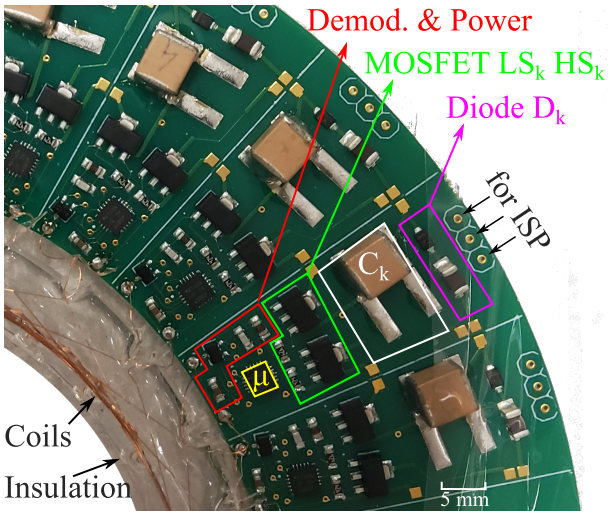


Fig. 5: Picture showing 5 of the 24 levels, corresponding to an angular sector of 12°, of the modified Marx generator presented in Section III. The inner and outer diameter are 10 cm and 17 cm respectively. On one level (sector) the relevant components of the circuit are highlighted, namely: the rectifier for demodulation and the power (cyan), the microcontroller to decode and drive the MOSFETs $LS_k$ and $HS_k$ (green), the capacitor $C_k$ and the diode $D_k$ (white), and the Schottky diode to demodulate the binary amplitude-shift keying (red). The three pins (black) situated on the outer diameter are used for the in-situ programming of the $\mu C$.

in the DEA are measured with an oscilloscope (Lecroy HDO4000). Simulations are carried out with Simscape Electrical from Matlab Simulink using the parameters from the component data sheets, or measuring them directly when the nominal value are not available. The simulation file, all the components reference and components measurement are provided in the supplementary materials.

The charge/discharge voltage, and currents along a full cycle are shown in Fig. 6, while Fig. 7 shows a zoom, from the $5^{th}$ up to the $9^{th}$ step of the charge process allowing to better appreciate its structure. Each $k$ voltage step represents the connection of the level capacitor $C_k$. For instance, focusing on the $6^{th}$ charge step starting at time $t = 0.212$ s, the voltage $V_{out}$ (blue lines) is passing from 1628 V to 1948 V which corresponds to the level-capacitor voltage $V_6 = 320$ V. Over the same step the current (red lines), when the limiter is active, is at its limit 1.1 mA (i.e. plateau from 0.212 s to $\approx 0.213$ s) and the DEA is charged through a linear voltage increase (blue lines). Then at 0.214 s, the $7^{th}$ step follows, showing a similar response, and so on until all level-capacitors get switched from parallel to series. The current spike in the experimental measurements, apparent in Fig. 7 at the starting point of the plateau, are induced by the switching and by parasitic elements. After a damped oscillation, the current gets back to the plateau constant value (see inset in Fig. 7). Once achieved, the full DEA charge, at $t = 0.25$ s, $V_{DEA} = V_{max}$. Up to $t = 0.7$ s,

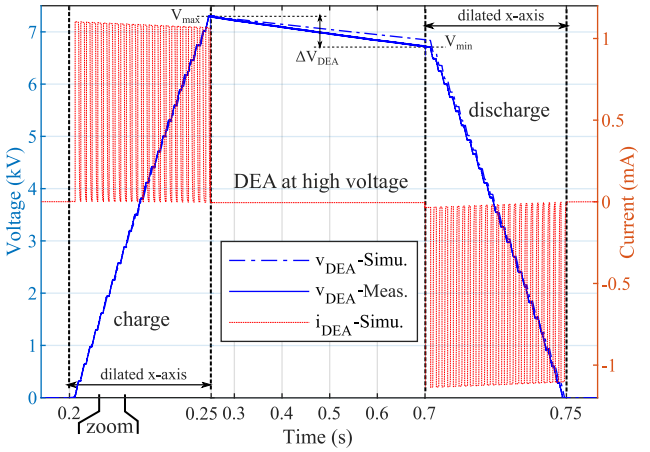


Fig. 6: DEA's voltage $V_{DEA}$, and current $i_{DEA}$ along a cycle. Continuous, and dashed lines show the measured, and simulated data respectively. The $x$-axis has been dilated in correspondence to the charge, and discharge processes in order to better appreciate their multistep structure.

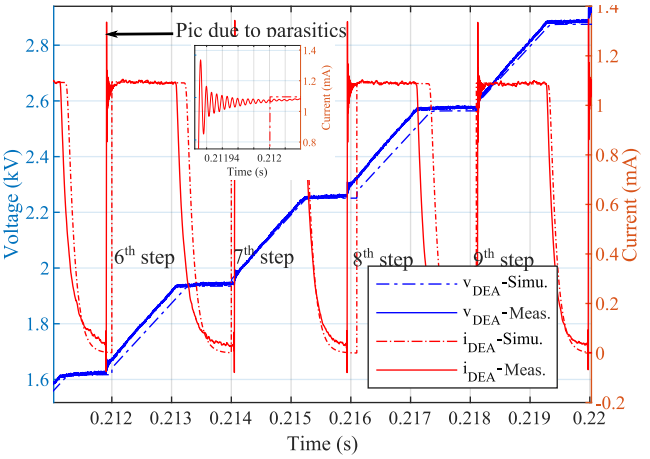


Fig. 7: Main frame: zoom from the $5^{th}$ up to the $9^{th}$ step along the charge process of Fig. 6. Inset: zoom showing the damped oscillations that follow the current peaks due to parasitic elements.

a small voltage drop $\Delta V_{DEA}$ takes place. This is due to the energy conversion in the DEA (viz. $R_p$ in the present setup), and to current leakages in the components ($C_k$, $LS_k$, $D_k$). At $t = 0.7$ s, where $V_{DEA} = V_{min}$ the discharge process takes place showing a pattern similar to the one of the charge, reversed.

These results offer the opportunity to appreciate the main advantages of the proposed setup, in terms of overall efficiency. Let us consider the energy converted by the DEA (i.e. dissipated in $R_p$) as measured (simulated) $E_{DEA} = 119.1$ mJ (121.5 mJ), over the energy transferred by the current source, $E_{in} = 134.4$ mJ (137.4 mJ). Defining the charge-discharge efficiency as follows:

$$\eta = \frac{\int_0^{t_p} \frac{V_{DEA}(t)^2}{R_p} dt}{\int_0^{t_p} V_1(t) I_s(t) dt} \tag{3}$$

we get 88.7% (88.4%) efficiency, corresponding to $E_{loss} = 15.2$ mJ (15.9 mJ) losses over a full cycle. A rather satisfying result considering that, in a similar case (i.e. charge/discharge of low-power, high voltage DEAs) the reported efficiency has been of the order of 15% [7].

Simulations and experiments are in pretty good agreement in term of signal as well as in term of efficiency. Minor discrepancies are related to a slight delay $t_s$ mismatch, and to the component values dispersion in the experimental setup.

## V. Losses and DEA voltage drop

In this section to provide design guidelines, we identify and model the cause of the energy losses and of the DEA voltage drop $\Delta V_{DEA}$, both relevant characteristics for DEAs. Thereafter, supported by numerical simulation, we illustrate the important role of the level capacitance characteristic, value and distribution.

### A. Losses analysis

First of all the 0.8 mW (with 333 kHz clock and 5 V) consumption per stage due to the $\mu C$, are not taken into account in the overall efficiency, Eq. (3). Indeed, these losses are directly supplied by the external magnetic field, thence they are related to the wireless powering of the modulator, an issue we shall address elsewhere. Nonetheless, it is worth noting that these losses can be easily reduced of two orders of magnitude through an advanced energy management mode of the $\mu C$.

The three main mechanism driving the energy loss per cycle are: the losses associated with current leakages $E_{leak}$, the losses taking place in the level diodes $E_D$ and the losses associated with charge transfer between level capacitors $E_J$. In the following sub-subsection each are modeled as a function of the number of level $N$, the level capacitance $C_k$, and of the DEA voltage, $V_{max}$ and $V_{min}$ and they are estimated for the adopted setup. The total loss per cycle extrapolated in this section $E_{tot} = 14.8$ mJ, is in good agreement with the the measured (simulated) value 15.2 mJ (15.9 mJ), confirming the pertinence of our loss analysis.

Here, the reduced number of low voltage switching of the adapted Marx generator makes the losses related to the parasitic capacitance negligible, a fairly relevant improvement over some of the previously reported works on powering low power and high voltage DEAs [6], [7].

*1) Current leakage losses:* the energy losses associated with current leakages $E_{leak}$ are related to a static dissipation taking place in high voltage components (i.e. $D_k$, $LS_k$, $HS_k$ and $C_k$). The components used within the presented setup have been selected for their low leakage properties. Here, leakage losses over a cycle, $E_{leak} \approx 1.5$ mJ, are dominated by the level-capacitors,

$$E_{leak} \approx \frac{\sum_{k=1}^{N} C_k}{2\tau_C} \left( \frac{V_{max} + V_{min}}{N} \right)^2 t_p. \qquad (4)$$

where $\tau_C = 1200$ s is the self-discharge time (3 G$\Omega$ $\times$ 0.4 $\mu F$).

*2) Losses in the diode:* To maintain the device cycle, the current source (i.e. the energy input) compensates the energy transferred to the DEA and the losses. When the DEA is at maximum voltage, only $C_1$ is connected to the current source. To avoid an abrupt voltage increasing in $C_1$ due to its low capacitance, and the additional losses due to the consequent huge voltage difference between $C_1$ and $C_2$ once connected, the current source is active only when all the capacitances are in parallel (i.e. when $V_{DEA} = 0$). When the current source is active $I_S \approx 0.95$ mA, the current in the diodes represents an additional source of losses. Assuming that all capacitors are recharged with the same energy, only a fraction $(N + 1 - k)/N$ of the total current pass through the $k^{th}$ diode inducing the following overall losses:

$$E_D \approx \sum_{k=1}^{N-1} \frac{(N+1-k)}{2N} I_s V_D = \frac{(N-1)(N+2)}{4N} I_s V_D, \qquad (5)$$

with a diode voltage $V_D = 0.6$ V these losses are $E_D = 3.4$ mJ over a half cycle.

*3) Losses due to the charge transfer between capacitors:* the loss associated with the connection between a capacitor $C_1$ at voltage $v_1(0)$ to a capacitor $C_2$ at voltage $v_2(0)$ represents a sort of elementary brick of the multistep charge/discharge process proposed here. The final voltage of the two connected capacitors worked out from the voltages balance, and the charge conservation writes:

$$v = \frac{C_1 v_1(0) + C_2 v_2(0)}{C_1 + C_2}. \qquad (6)$$

Expression (6) allows extrapolating the losses due to charge transfer $E_J$ as the difference between the energy stored before connecting the capacitors, and after reaching equilibrium, without getting into the detail of the involved dissipating processes (a resistance, a diode, or a current limiter). This gives:

$$E_J = \frac{1}{2} C_{eq} \left( v_1(0) - v_2(0) \right)^2, \qquad (7)$$

where $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$. Using Eq. (7) to estimate the losses taking place during the successive capacitor connections within the charge, and the discharge processes, we get $E_J^{ch} = 5.4$ mJ, and $E_J^{dis} = 4.5$ mJ respectively.

To pinpoint the relevant benefit of the multistep charge/discharge protocol proposed here, let us assume $C_{eq} = C_{DEA}$, a pretty reasonable approximation as $(\sum_{k=1}^{N} 1/C_k)^{-1} \gg C_{DEA}$. Thence the charge losses are,

$$E_J^{ch} \approx \frac{1}{2} C_{DEA} \sum_{k=1}^{N} V_k^2 = \frac{1}{2} C_{DEA} \frac{V_{max}^2}{N}, \qquad (8)$$

where the $1/N$ loss reduction makes apparent the benefit of the multistep modified $S^2M^2$ charge. Indeed, a single step charge would give: $E_J^{ch} = \frac{1}{2} C_{DEA} V_{max}^2$. A similar expression can be obtained for the discharge by replacing $V_{max}$ with $V_{min}$. In addition, it is worth noting that the use of the current limiter preserves the overall value of the

Joule losses, displacing the dissipation from $R_a$ to the current limiter in order to avoid DEA damaging, and improving its lifespan.

### *B. Voltage drop on the DEA*

So far, the DEA voltage is just mentioned as the sum of the level capacitor voltages, as described by Eq. (1). Now it can be of some interest to link $V_{DEA}$ along the charge/discharge, and during the energy conversion, with the voltage evolution (drop) on a single level capacitor, $V_k(t)$. Here, we separate the voltage drop associated with the DEA charge $\Delta V_k^{ch}$, and the further drop $\Delta V_k$ associated with the energy conversion in the DEA. As an example, the voltage on the first level capacitance is shown in Fig. 8. After a voltage increase, when the current source is active, lasting till $t = 0.2$ s, the level voltage undergoes a steep drop (i.e. between 0.2 s and 0.25 s) $\Delta V_k^{ch}$ associated with the DEA charge, a slower one (i.e. between $t = 0.25$ s and $t = 0.7$ s) $\Delta V_k$ associated with the DEA energy conversion, a fast increase due to the charge transferred back from $C_{DEA}$ (i.e. between 0.7 s and 0.75 s), a short drop due to charge re-circulation, and eventually a recharge from the current source.

Besides, the coupling between the level capacitance and the DEA, $V_k(t)$ depends on its position in the charge/discharge sequence as the level $k$ sees $(N + 1 - k)$ charge transfers. This can be better appreciated considering the following expression:

$$\Delta V_k^{ch} \approx \frac{C_{DEA} V_1 (N + 1 - k)}{C_k}, \tag{9}$$

where the dependence of the voltage drop associated with the charge on $k$ and on $C_k$ is made apparent. On the other hand, assuming the charge leakages on the level capacitors to be negligible, the drop due to the energy conversion writes:

$$\Delta V_k \approx \int_{0.25}^{0.7} \frac{V_{DEA}(t)}{C_k R_p} dt. \tag{10}$$

Eq. (9) and (10) make clear that different strategies can be adopted regarding the distribution of $C_k$ values. For instance, when the total capacitance is fixed, a distribution $\propto \sqrt{N + 1 - k}$ (we shall refer as the square root distribution) would maximize $V_{max}$. On the other hand, a uniform $C_k$ distribution would minimize $\Delta V_{DEA}$, keeping $V_{DEA}$ nearly constant during the conversion process.

In the prototype presented here, different number of capacitor in parallel per level have been tuned in order to approach a square root distribution, and to maximize $V_{max}$.

### *C. Optimization of the level-capacitance*

The studies of the losses, and of the voltage drop, show that the level-capacitors role, in the proposed architecture, is twofold. On the one hand, large capacitor values are needed to keep, the charge transfer losses $E_J^{ch}$ and $E_J^{dis}$ and the voltage drop, low. On the other, small capacitor values would limit the current leakage loss. In addition, the $C_k$ distribution play a minor but subtle role in the charge re-circulation, eventually affecting the diode losses $E_D$.

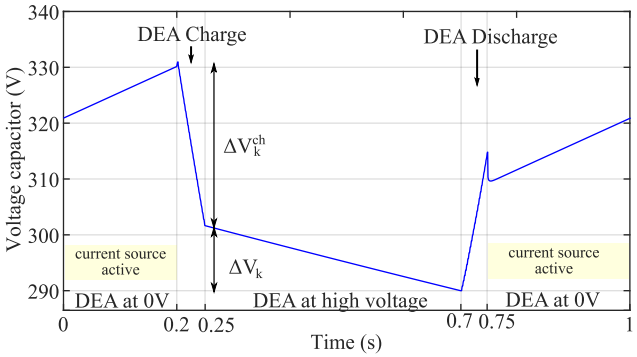


Fig. 8: Voltage $V_1$ of the level-capacitor $C_1$ along a full cycle. For $t \leq 0.2$ s the current source $I_s$ is charging the capacitor; from $t = 0.2$ s to 0.25 s the $\Delta V_k^{ch}$ voltage drop is due to the charge transferred to $C_{DEA}$; from $t = 0.25$ s to 0.7 s a further drop $\Delta V_k$ is associated with the energy converted by the DEA; at $t = 0.7$ s the voltage increases due to the charge transferred back from $C_{DEA}$; a short drop at $t = 0.75$ s is due the charge re-circulation, afterwords the capacitance gets again under charge from $I_s$.

In this section we use the numerical simulations, which have fitted pretty well the experimental results of the presented setup, as a tool to investigate the device overall efficiency, and the DEA's voltage drop $\Delta V_{DEA}$. Fig. 9 shows Simscape results performed on our 24 stages modified $S^2M^2$ as a function of the total level capacitance, using a uniform (continuous line) and a square root (dashed line) $C_k$ distribution. Increasing the total level capacitance up to about 15 $\mu$F induces a pretty steep $\Delta V_{DEA}$ reduction, and decreases the voltage variation per level (a consequence of Eq. (10) and (9)). At the same time, the overall efficiency increases, due to a reduction of the charge transfer losses (i.e. Eq. (7)). Hereafter, as soon as the equivalent capacitance in the charge transfer is dominated by $C_{DEA}$, the reduction of the charge transfer losses is less effective, whilst the increasing current leakages (i.e. Eq. (4)) lead to a diminish in the overall efficiency.

The uniform distribution lowers the voltage drop, as expected, and slightly improves the efficiency because the level capacitor at level $k + 1$ has always a voltage higher than the level $k$, avoiding charge re-circulation and the related losses when they are in parallel. In this trade off, our experimental choice of level-capacitance values provides an overall efficiency close to the maximum with a moderate voltage drop.

The number of stages plays also a key role, because of its relationship with the the device volume on the one hand, and with its efficiency, on the other.

When the number of stages is increased of a factor $\alpha$ (i.e. $\alpha N$), the level capacitor values increase by $\alpha C_k$ in order to compensate the voltage drop (sum of the Eq. (9)). The resulting stored energy does not change (i.e $\alpha N(\alpha C_k)(V_k/\alpha)^2$ is not related to $\alpha$). However, the energy is stored at a different voltage, possibly leading to different capacitor

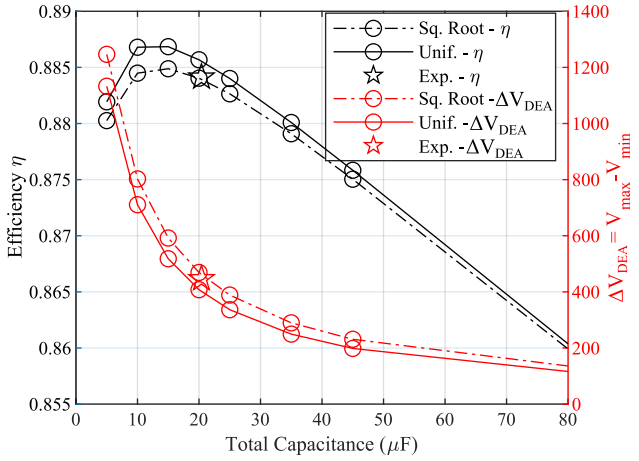


Fig. 9: Estimation of the overall efficiency (black) and DEA's voltage drop (red) from numerical simulations as a function of the total effective capacitance, using a uniform and a square root $C_k$ distribution. The star shaped points represent the values measured on the experimental setup presented in this work (i.e. square root $C_k$ distribution).

technologies and self-discharge time. The resulting losses in the DEA charge/discharge transfer reduction ($E_J^{ch/dis}/\alpha$) is balanced by losses in the diode increase ($\alpha E_D$) as recharging the last levels becomes more difficult. Assuming the same capacitance self-discharge time, the leakage in the capacitor $E_{leak}$ does not depend on the number of levels.

## VI. Conclusion

A multilevel Marx generator has been adapted as an efficient, and low volume way to supply a low power DEA at voltage up to 12.5 kV. The main advantages of the proposed principle have been discussed, and a 24 level experimental demonstrator charging a DEA up to 7 kV is presented and fully characterized. The proposed setup reaches an excellent overall efficiency, up to 88% . Furthermore, the device has been designed to limit its volume, and to be powered and controlled with a wireless component. The beyond state-of-the-art efficiency, the limited volume, and the wireless control/power design all make the presented setup a possible candidate for implanted cardiac assist devices with a pretty high technology readiness level. Indeed, the benefits of the multilevel architecture are threefold: they reduce the voltage stress on the individual levels, allowing a rather relevant size reduction of the components; they reduce the current stress in the DEA; they significantly improve the efficiency.

In addition to the proof of the concept, analytical modeling and simulations allow highlighting the key features of the proposed design. On the one hand, the total volume of capacitance balances the charge efficiency and the voltage drop with the losses due to leakage current. On the other, the number of levels is very effective to reduce the huge losses due to the charge transfer $E_J^{ch+dis}$. However, the number of levels is limited by the losses in the diode $E_D$. Energy density and self discharge of the level capacitors are critical and need to be chosen with care to reduce the volume and to improve the efficiency.

Eventually, the experimental test on a real DEA works in accordance to the RC model, as apparent in the video available in the supplementary materials.

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