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# Further Analysis of Laser-induced IR-drop

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**Abstract**—Studies on laser induced IR-drop are recent and still not much covered. Since laser-induced IR-drop can amplify the well-known effects of induced photoelectric currents in ICs, this work aims to present important characteristics of such effect. Understanding the characteristics and effects of laser induced IR-drop in ICs allows the elaboration of more accurate simulation models, and consequently helps in the design of countermeasures that mitigate the effects of laser illumination. Simulations and experiments were performed in order to understand the relationship of the laser pulse width and the decoupling capacitance of the power supply network with the induced IR-drop. The results showed that the maximum variation of the supply voltage depends on the laser pulse duration, and on other circuit characteristics, such as RLC parameters of the supply network. It was possible to observe by simulations and experiments that, for the proposed circuit, the maximum variation of the supply voltage occurred for a laser pulse greater than or equal to 1  $\mu$ s. Regarding the decoupling capacitance variation, the results showed that for a decoupling capacitor up to 100 pF, the IR-drop becomes even more relevant with a variation up to 97% of VDD.

**Index Terms**—Laser fault injection, IR-drop, Electrical simulation.

## I. INTRODUCTION

Electronic devices are continuously improved in order to reduce their dimensions [1] and still be robust to failures [2]. Among the different causes of failure to which an electronic device is subject, there are random failures caused by environment disturbances (e.g. by intense solar activity) [3] and intentional failures, caused for a specific purpose (e.g. laser attacks aimed at acquiring sensitive information) [4]. The study of the different effects to which these devices are exposed is then important to maintain their proper functioning even when operating in extreme environments or under malicious attacks.

Within the context of malicious attacks, fault injection attacks (FIA) have become a common way to defeat the security mechanisms of embedded devices. There is a large and constantly growing number of known techniques for injecting faults into ICs [5], [6]. Among them, one can find techniques to disrupt the clock signal [7], to induce sudden variations of the supply voltage [8] or of the bulk biasing [9], and to inject parasitic currents using powerful electromagnetic disturbances [10] or intense light flashes [5].

The efficiency of optical attacks was first demonstrated using a camera flash [11]. However, for better accuracy and control, focusable sources of ionizing radiations are preferable,

for example laser sources. These sources allow to control the injected faults with precision thanks to their high spatial and temporal resolutions, as highlighted in [11], which reported in the early 2000s the use of laser to induce a type of fault, called bit-flip in the literature, in an SRAM cell. After this pioneering work, the need to design circuits robust to laser fault injection (LFI) has gained visibility in the scientific community. Consequently, it started the development of models and methodologies that would allow researchers to simulate the effects of laser attacks on ICs. Although LFI simulations can be performed at different abstraction levels of design flows (transistor level, gate level, RTL level, and even software level), low abstraction levels provide the highest accuracy.

When a laser illuminates an IC, it generates a parasitic (photoelectric) current [12]. This current generates an undesired transient voltage that propagates through the logic toward the input of a register (e.g., D-type Flip Flops) and, if it is still present when the next rising clock edge occurs, a bit may be inverted, producing a soft error (SE) [13]. At the electrical level, a current source, with a double exponential-shaped current profile, can efficiently model the photocurrent generated at a PN junction by the effects of laser illumination [14], [15]. By adding this current source according to the cell illuminated by the laser beam, it is then possible to perform an electrical level simulation with satisfactory precision.

However, considering only the effect of a single induced electric current may be imprecise for recent technologies. Indeed, with increasing transistor density, laser illumination does not affect a single transistor (or CMOS gate) but several of them simultaneously. In this case, a laser shot also induces a current that flows from VDD to GND causing a temporary drop in supply voltage (IR-drop) known by designers to be a source of timing failures. As the induced IR-drop may be of significant amplitude and duration [16], [17], it has to be taken into account while performing LFI simulation.

Consequently, more complex circuit simulations are needed to ensure a good representation of the real effects of laser illumination. A previous study showed, for example, that the joint effects of the photoelectric currents and of the related IR-drop can only be accurately simulated at low abstraction levels (taking into account the layout topology to better represent the physical phenomenon) in the scope of a whole system [18].

A methodology that allows LFI simulation at the electrical level in large-scale circuits by using standard CAD tools was presented in [18] as well as an enhanced electrical fault model

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that takes laser-induced IR-drop into account.

This study extends the simulations and experiments regarding the effects of IR-drop during LFI by presenting its correlation and relevance for different pulse durations and capacitance intrinsic to the supply network of ICs.

## II. STATE OF THE ART OF LASER SHOT EFFECTS ON ICs

### A. Effect of a Laser Shot at Transistor Level

Transient electrical currents induced in ICs can cause malfunctions. As seen in previous studies, these electrical currents can be generated, for example by exposure to ionizing radiation or even by laser beams passing through the device [12]. Laser pulses are composed of photons which are absorbed by the material to generate electron-hole pairs. When these charges are generated near the PN junction regions, where strong electric fields are present, electric currents are induced in the device [13]. The transient electric current that is induced has characteristics that depend on the laser power and the location of the spot, as well as the device technology and circuit supply voltages. Early studies of the effects of laser illumination on ICs were conducted in order to simulate the effects of ionizing particles, since both effects are similar [19].

Fig. 1 shows in simplified way how an electric current is induced by the passage of a laser beam in a PN junction. When a laser beam passes through a sensitive region of the MOSFET, an ionization path is created. Therefore, the production of free charge carriers in the MOSFET occurs. When these charges are generated close to an active region (PN junction), where there is a strong vertical electric field, they are collected immediately and generate a transient electrical current. This phenomenon is illustrated in Fig. 1.

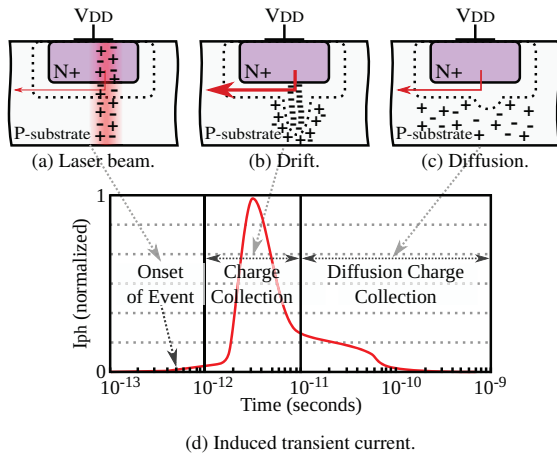


Fig. 1. Photoelectric effect of a laser beam through a PN junction [12], [13].

Fig. 1(a) illustrates the generation of charges through the trajectory of a laser beam that crosses a reverse biased PN junction.

Fig. 1(b) depicts the temporary funnel-shaped distortion of the depletion region along the laser path, promoting an electric current pulse that lasts a few picoseconds.

Fig. 1(c) presents the step where the charge funnel disappears, at this point the diffusion current component dominates the collection process until all excess charges have been collected by the electric field.

The photoelectric effect described above then generates a transient current through a reverse biased PN junction, but this does not necessarily mean that there is a fault in the electronic device. For a fault to eventually occur, it may depend on variables such as the amplitude of the transient current (photoelectric current,  $I_{Ph}$ ), the location in the circuit of the component exposed to the laser beam and the input data.

### B. Effect of a Laser Shot at Gate Level

To understand the effects of a laser shot at gate level, the case of laser illumination of a CMOS inverter will be considered. Fig. 2 shows the electrical currents that can be induced depending on the input signal.

Assuming that the input of the inverter is equal to the logical value '0', and consequently the output is equal to '1' (Fig. 2(a)), and assuming also the circuit in stationary condition, the equivalent output capacitance ( $C_{Load}$ ) (i.e., the sum of all gate capacitance of cells connected to this output) is fully charged. In this case, the drain of the NMOS transistor is the most laser-sensitive location in the inverter, because there is at that moment a reverse biased PN junction (between the drain and the  $P_{substrate}$ ). By illuminating this region with laser beams, an induced electric current ( $I_{Ph}$ ) flows from the drain of the NMOS to the  $P_{substrate}$  biasing contact (at GND). Similar reasoning can be made when the inverter input is high (Fig. 2(b)). In that case, the susceptible part of the inverter is the drain of the PMOS transistor. In Fig. 2(a) (resp. Fig. 2(b)), a part of the induced photocurrent ( $I_{Ph}$ ) discharges (resp. charges) the inverter output capacitance. As a result the inverter output switches to low voltage (resp. high voltage), thus a so-called voltage transient occurs.

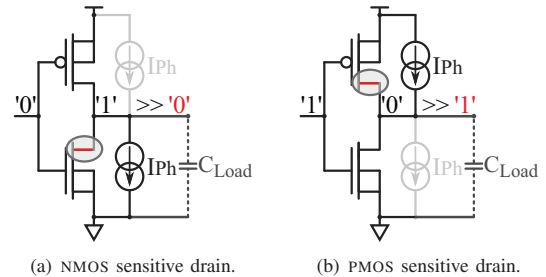


Fig. 2. Electrical model of laser-induced transient currents applied to a CMOS inverter.

Another important parameter when considering the effects of a laser shot, is the beam diameter. A good approximation for the beam considers a Gaussian radial profile, where the spot diameter is 86.5% of its maximum value [20].

The authors in [21] show a model which the induced electric current is spatially distributed as a Gaussian profile, has a peak amplitude ( $I_{Ph\_peak}$ ) and follows the empirical equation (1):

$$I_{Ph\_peak} = (a \times V + b) \times \alpha_{gauss(x,y)} \times Pulse_w \times S \quad (1)$$

where  $V$  is the reverse-biased voltage of the exposed PN junction,  $a$  and  $b$  are constants that depend on the laser power.  $\alpha_{gauss(x,y)}$  is a term related to the Gaussian distribution of the laser beam amplitude in space,  $Pulse_w$  is the laser pulse duration and  $S$  is the area of the PN junction. More details about each parameter can be seen in [21].

Fig. 3 shows a three-dimensional view relating the intensity of the laser beam to coordinates in  $x, y$ .

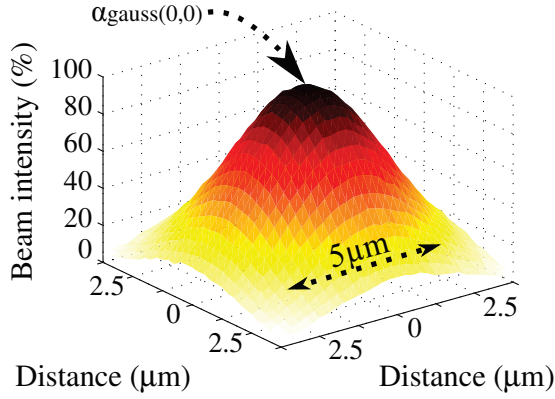


Fig. 3. Three-dimensional view of a laser beam in terms of intensity per area. 100% of laser beam intensity represents the epicenter of the laser spot.

### C. Effect of a Laser Shot at Circuit Level

As seen above, laser shots can generate electrical currents ( $I_{Ph}$ ) in certain locations of the circuit. The duration of this current depends on the injection time. If the duration is large enough and the inverter in Fig. 2 is part of a combinational logic block, the output capacitance of the circuit can be discharged to the point where the voltage drops below the threshold voltage of the next logic block, thus causing a logic fault.

Fig. 4 illustrates a Soft-Error (SE) induced in a Data-type Flip-Flop (DFF). It can be seen that if a transient voltage arrives at the input of the memory cell at the time of data writing, this disturbance can propagate through the circuit for the next clock cycle and affect the operation of the circuit.

### D. IR-Drops During Laser Fault-Injection

In order to improve the existing models, which for recent technologies lack accuracy by only considering currents induced to the drain regions sensitive to laser shots, a new model that also takes into account a current flowing from VDD to GND has been proposed. This current is induced in the reversed biased  $P_{sub-Nwell}$  junction and can have significant effects on a circuit by inducing a supply voltage drop [18], [22]. Fig.

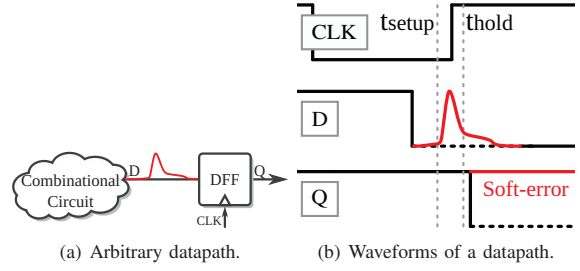


Fig. 4. Propagation of a transient voltage through the combinational circuit causing a soft-error (in red).

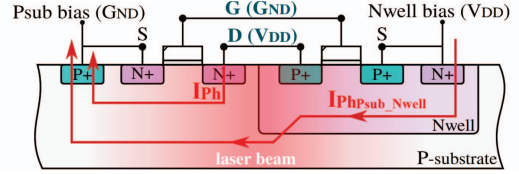


Fig. 5. Laser-induced current components. Cross-section of a CMOS inverter.

5 (cross-section of a CMOS inverter) illustrates this additional current, called  $I_{PhPsub\_Nwell}$ .

Fig. 6 presents the proposed model for a CMOS inverter that takes into account the  $I_{PhPsub\_Nwell}$  current. Although this current does not cause direct interference in the inverter output, it does cause disturbances in the circuit power supply network. Furthermore, thinking about larger circuits, as neighboring cells are subject to similar transient currents, their effects add up and can propagate to separate cells via the power distribution network (PDN).

However, this proposed model is not useful if the power supply grid is considered as ideal. For the application of the model, it is necessary to model the power-grid as well. In [18] the methodology applied in this work, which is based on an Electromigration / IR-drop (EMIR) CAD tool, is detailed.

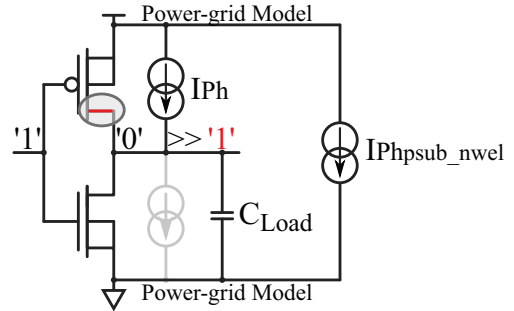


Fig. 6. Proposed laser induced transient fault model applied to an inverter with input biased at VDD to take into account the supply voltage drop/bounce induced by the  $I_{PhPsub\_Nwell}$  parasitic current.

In Fig. 6, the current sources have a double exponential profile. The currents have a peak amplitude defined by eq. (1). The  $S$  parameter (i.e. the area of the considered PN junction)

used to model  $I_{Ph}$  and  $I_{PhPsubNwell}$  are respectively, the PMOS drain area and the  $Nwell$  area (see Fig. 5). As a result, because PMOS drain area is significantly smaller than the area of  $Nwell$ ,  $I_{PhPsubNwell}$  is bigger than  $I_{Ph}$  [18], [22].

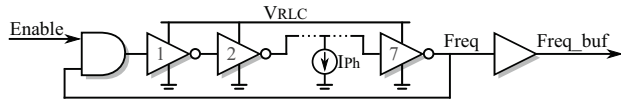
Since the power grid is resistive and capacitive, when adding  $I_{PhPsubNwell}$  currents flowing from VDD to GND, VDD drops and GND bounces occur. This induces voltage oscillations in the PDN that can cause timing errors (timing constraint violations) or even data disruptions leading to erroneous sampling values by DFFs.

### III. IMPORTANCE OF IR-DROPS DURING LASER FAULT-INJECTION

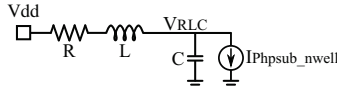
#### A. Methodology for Experimental and Simulation Analysis

To perform a comparative study between the classical model and the model proposed, both models were implemented in a ring oscillator (RO). In order to evaluate the performance of each model, the RO was also implemented in an FPGA. It was considered the cases where the laser illuminates directly the RO's standard cells and where the laser illuminates regions near the RO (i.e. without direct laser illumination of its logic gates).

The RO was chosen as study case because it presents a frequency variation proportional to the variation of the supply voltage [23], [24]. This characteristic makes it interesting to use to experimentally verify supply voltage drops just by observing the oscillation of its frequency [25]. Fig. 7 shows the schematics used for the electrical simulations of the effects studied.



(a) RO block diagram including the IR-Drop contribution (non-ideal VDD) for a given power-grid model.



(b) Lumped elements of a series RLC network +  $I_{PhPsubNwell}$  current component in parallel.

Fig. 7. Electrical model of laser-induced transient currents applied to a ring oscillator.

Fig. 7(a) describes the RO, which was designed using CMOS 65 nm technology. It features an AND2 gate, a BUFFER gate, and seven inverters. Its nominal oscillation frequency is equal to 148 MHz. Fig. 7(b) shows a lumped model of an RLC network. This model includes the decoupling effect of the power grid as well as its inductance and resistance. Therefore, it takes laser-induced IR-drops into account during electrical simulations by setting  $I_{PhPsubNwell} > 0$ .

#### B. Simulation and Experimental Results

The simulations performed in [18] illustrated the importance of taking into account the effects of laser-induced IR-drops.

When considering the case of direct illumination of the RO with an infrared laser, the classical model indicated a drop of the circuit frequency from 148 MHz to about 100 MHz. The enhanced model, which takes into account the  $I_{PhPsubNwell}$  current, showed a drop of the frequency to zero. Further, experiments show results consistent with the enhanced model, with the circuit frequency being forced to zero by the effects of the  $I_{Ph}$  and  $I_{PhPsubNwell}$  currents combined.

When analyzing the effects of laser shots near the RO, the enhanced model show again a high level of correlation with the experimental data. Fig. 8 shows the location of the RO with respect to the laser shot for this experiment.

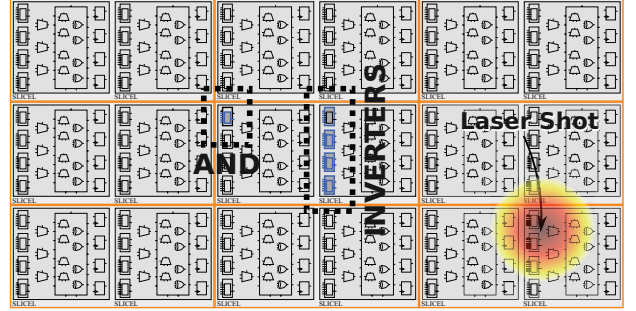


Fig. 8. Position of the RO and the laser shot, when the RO is not directly illuminated.

The classical model shows no effect on RO operation as it disregards the  $I_{PhPsubNwell}$  current.  $I_{Ph}$  being equal to zero reflects in no PN junction sensitive to laser shots being illuminated. The enhanced model show similar variations to the experimental results in RO frequency (resp. in RO supply voltage). Figure 9 presents the simulation and experimental data for such a case with a 5  $\mu$ s pulse, showing a good correlation between the two.

### IV. IMPORTANT CHARACTERISTICS OF LASER INDUCED IR-DROPS

In this section, the influence of laser pulse duration and RLC parameters on the characteristics of laser induced IR-drops is discussed.

#### A. Influence of the Pulse Duration on Laser Induced IR-Drops

To analyze the effect of laser pulse duration, three laser shots with duration equal 100 ns, 1  $\mu$ s and 5  $\mu$ s were applied to the target embedding the RO. These shots were obtained using a laser diode source with 1064 nm wavelength (infrared range) and using a power equal to 1.04 W (considering 57.84% of the lens coefficient transmission). The laser spot size was set at 5  $\mu$ m. The output frequency of the RO was measured during the experiments.

Fig. 10 shows the applied pulses and the related evolutions of the oscillation frequency of the RO. One can observe on this figure that for short pulses the amplitude of the frequency drop, and thus the one of the IR-drop, is lower than for long pulses. This could be explained by the role of decoupling



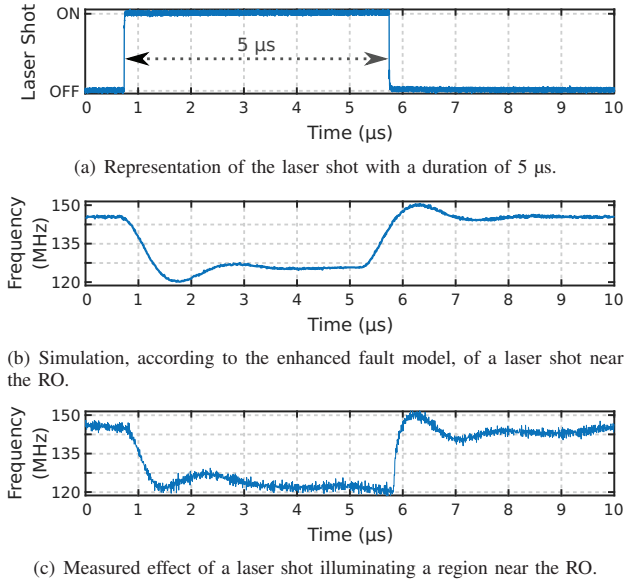


Fig. 9. Effect on the RO oscillation frequency of a laser shot illuminating a region close to it.

capacitors that are able to provide enough charges to the PDN to counterbalance for short pulses of the induced IR-drop. For longer pulses however, the charge stored in the decoupling capacitance is not sufficient to counterbalance the laser induced IR-drop, thus the frequency settles to a constant value after approximately 1 μs.

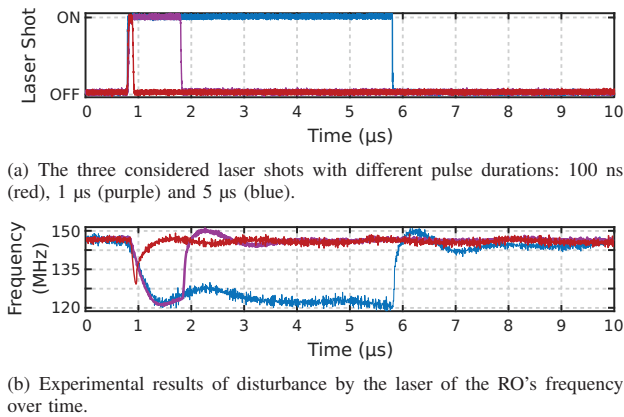


Fig. 10. Experimental results: maximum drop in frequency for different pulse durations.

Fig. 11 presents the results of simulations performed with the enhanced model (Fig. 7) for the different laser pulse durations.

Comparing Fig. 10 and Fig. 11, it can be seen that the simulation results with the enhanced model are very similar to the experimental ones. The classical model works well for simulations with laser pulses of duration on the order of ps, having effects similar to those of ionizing radiation,

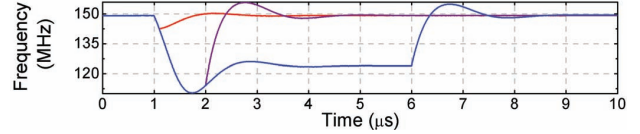


Fig. 11. Simulation results of the RO frequency drop for different laser pulse durations.

but can present significant inaccuracy with longer pulses. As can be seen in Figs. 10 and 11, for pulse duration shorter than 100 ns, variations in circuit supply voltages can be negligible depending on the IC. However, laser fault injection can have a significantly longer pulse duration, and in such cases the induced  $I_{Ph_{Psub\_Nwell}}$  current passing through the power supply networks becomes very relevant to the operation of the circuit. This highlights the importance of using an improved model that considers such effects.

Such simulations allow predicting the minimum pulse duration that will cause an attenuation of the induced IR-drop depending on the technology, circuit size and amount of decoupling capacitors.

### B. Influence of RLC Parameters on the Laser Induced IR-Drops

In order to evaluate the influence of the circuit RLC parameters on the laser induced IR-drop, simulations using the model shown in Fig. 6 and 7 were performed. For these simulations, different values for the network capacitance ( $C$ ) were used (Fig. 7(b)). The frequency of the RO was then observed during 10 μs for each value of  $C$ .

Fig. 12 depicts the different RO frequency variation curves obtained for the network capacitances of 8 nF, 2 nF, 1 nF, 250 pF and 100 pF, with a laser pulse duration of 5 μs.

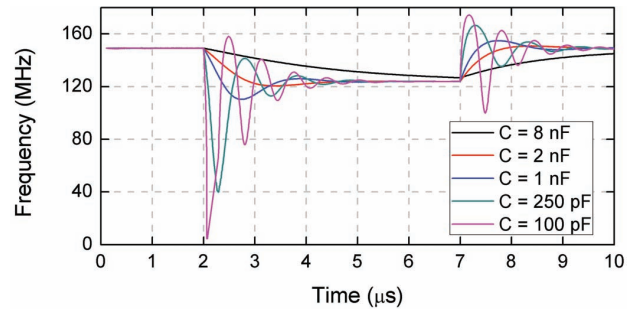


Fig. 12. Simulation results of the RO frequency drop for different network capacitances.

By analyzing the curves in Fig. 12 it is possible to see the direct impact of the internal and external capacitances connected to the circuit. For the simulation with  $C$  equal to 100 pF there was a maximum drop in the frequency of the RO (and therefore its supply voltage) of about 97%, reducing it to practically zero. On the other hand, for a  $C$  of 2 nF, the maximum frequency drop of the RO was about 18%. This

operation is similar to that of a low-pass filter, allowing the supply voltages to be less affected by the  $I_{PhP_{sub,Nwell}}$  current for higher values of  $C$  [26]. As can be seen from the equation (2) [26]:

$$f_c = \frac{1}{2\pi RC} \quad (2)$$

for higher values of  $C$ , the result is a lower cutoff frequency ( $f_c$ , or critical frequency). In other words, for higher values of  $C$ , longer laser pulse durations are needed to have relevant effects on the supply voltages.

These results are important, since the design can be modified, based on this observation, to harden sensitive parts of the circuit. An alternative, for example, would be to add decap cells if the design allows (taking into account the overhead area caused by the addition of capacitors), in order to mitigate laser-induced IR-drop, which can amplify the effects of induced photoelectric current in electronic circuits and increase the incidence of faults.

## V. CONCLUSION

This paper presents new evidence and relevant points about the importance of taking into account laser induced IR-drop effects in ICs. Through a review of previous work and subsequent studies on the characteristics of such effects, it is reasonable to state that by using models that do not take into account laser induced IR-drop, transient faults may be underestimated or not correctly predicted.

The studies on the correlation of laser pulse duration and induced IR-drop have helped to clarify why previous models worked well for effects simulating ionizing radiation, but not for the effects of laser shots in general. It was observed that for pulses on the order of 100 ns or longer, which can easily be obtained from laser sources, IR-drop effects should not be neglected. Simulation and experimental results on the RO have shown a drop of about 20% in the supply voltage for pulses in the order of 1  $\mu$ s. The studies involving the correlation of the capacitance of the power supply network with the laser induced IR-Drop in a given electronic circuit show how important these effects can become depending on the design. Through the results obtained it was observed that the lower the parasitic and decoupling capacitance of the circuit, the more susceptible it is to laser fault injection. In the most critical case considered, with a capacitance  $C$  of 100 pF, the supply voltage had a 97% decrease.

The improved model and the simulations demonstrated in this work confirm that the laser induced IR-drop is a strong contributor to the fault injection process. These same models and simulations can help in the design of laser-hardened ICs, allowing to identify areas to be protected or to design electronic circuits that mitigate the effects of laser induced IR-drop through their known characteristics.

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