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Innovative Nanocomposites for Low Power Phase-Change Memory: GeTe/C Multilayers

Damien Térébénec,* Nicolas Bernier, Niccolo Castellani, Mathieu Bernard, Jean-Baptiste Jager, Martina Tomelleri, Jessy Paterson, Marie-Claire Cyrille, Nguyen-Phuong Tran, Valentina M. Giordano, Françoise Hippert, and Pierre Noé*

Innovative nanocomposites consisting of $[(\text{GeTe})_{4\text{ nm}}/\text{C}_{1\text{ nm}}]_{10}$ multilayers (MLs) deposited by magnetron sputtering are integrated in phase-change memory (PCM) test devices with a “wall structure.” Scanning transmission electron microscopy (STEM) shows that an ML structure, with crystallized GeTe layers, is kept after integration in as-fabricated devices and also after an additional annealing of the devices at 425 °C. The programming current (RESET current) required to reach the high resistance state of $[(\text{GeTe})_{4\text{ nm}}/\text{C}_{1\text{ nm}}]_{10}$ ML devices decreases by 45% after annealing at 425 °C. The reduction in RESET current is 55% and the reduction in drift coefficient is about 40% in ML devices annealed at 425 °C compared to similar devices incorporating $\text{Ge}_2\text{Sb}_2\text{Te}_5$. STEM imaging, coupled with nano-beam electron diffraction and electron energy loss spectroscopy, of ML devices in the high resistance state shows that the RESET current reduction after annealing is correlated to a reduction of the amorphized volume.

changed by application of electrical pulses that locally heat the active volume of the phase-change material by Joule effect. The active volume is successively programmed from the crystalline to the amorphous state or vice versa during the successive SET/RESET operations. A limitation of PCM is the high energy required by the RESET operation, which involves local melting of the phase-change material followed by quenching of the liquid phase to the amorphous state. Thus, an intense research effort aims at reducing the heat loss occurring during the RESET operation. The optimization of memory architecture engineering and the reduction in the size of memory devices have enabled a significant reduction in the energy required to switch the phase-change material between

1. Introduction

Phase-change memory (PCM) is widely recognized as one of the most promising next-generation nonvolatile memory technology for storage class memory applications and neuromorphic computing.^[1] In a PCM cell, information is stored at the nanoscale by using two distinct resistive states of a phase-change material such as a Ge–Sb–Te alloy. The high resistance state (RESET state) corresponds to the amorphous state, while the low resistance (SET state) corresponds to the polycrystalline state of the phase-change material. The state of the memory is reversibly

the two phases.^[2,3] Another approach to reduce the power consumption of a PCM is to reduce the thermal conductivity of the polycrystalline phase-change material thin film that surrounds the active volume of the PCM cell. To this end, doping of archetypical phase-change materials, such as GeTe or $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST), with a light element (C, N, O), has attracted much interest. Carbon-doped GeTe or GST alloys have better data retention and a lower RESET current than undoped alloys.^[4–6] During the crystallization process, C atoms migrate to GeTe/GST grain boundaries, which limits crystallite growth and decreases the thermal conductivity.^[5,6] However, C segregation cannot be controlled,

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resulting in cell-to-cell performance variability and compromising the integration of C-doped alloys in PCM cells at smaller technology nodes. In this context, deposition of multilayers (MLs) where thin layers of a phase-change material are separated by a spacer material seems a promising approach. In addition, an ML structure should allow to reduce the lattice thermal conductivity, through phonon scattering at the interfaces.^[7] In this work, carbon and GeTe nanocomposites consisting of GeTe/C MLs are deposited by magnetron sputtering at room temperature and integrated in PCM test vehicle devices. The thickness of the deposited amorphous GeTe layers is 4 nm and that of the amorphous C layers is 1 nm. The number of GeTe and C layers is set to 10. We show that such GeTe/C MLs enable to control the nanostructure of the phase-change material in devices and that the RESET current is then significantly reduced compared to similar devices incorporating the reference Ge₂Sb₂Te₅ alloy. The GeTe/C MLs deposited by sputtering are amorphous. Then, during final integration steps in our PCM test vehicle devices, the ML is submitted to a thermal budget of about 300 °C for 15 min. The term “as-fabricated” will be used later to describe these devices. After fabrication, some devices were further annealed at 425 °C for 15 min. These conditions were chosen

for two main reasons: first, to approach the maximum thermal budget of the back-end integration of industrial PCM devices, while preventing damage to the PCM in our test vehicles devices, and secondly, to crystallize the slight Ge excess (see later). A GeTe/C ML structure, with crystallized GeTe layers, is kept after integration and also annealing at 425 °C. A recent study has reported the deposition by sputtering of Ge₂Sb₂Te₅/C MLs (thickness of the deposited Ge₂Sb₂Te₅ layers between 6 and 9 nm and thickness of the deposited C layer of 0.5 nm).^[8] Such MLs integrated in devices were found to exhibit improved programming performances with respect to the Ge₂Sb₂Te₅ devices, which was ascribed to the formation of nanometer-scale C clusters from the deposited ML structure.

2. Results

A scanning transmission electron microscopy (STEM) image in the high-angle annular dark-field (HAADF) mode (**Figure 1a**) of a [(GeTe)_{4 nm}/C_{1 nm}]₁₀ ML in the pristine state of an as-fabricated PCM device shows a periodic ML structure, as confirmed by the intensity profile shown in **Figure 1c**. The interfaces

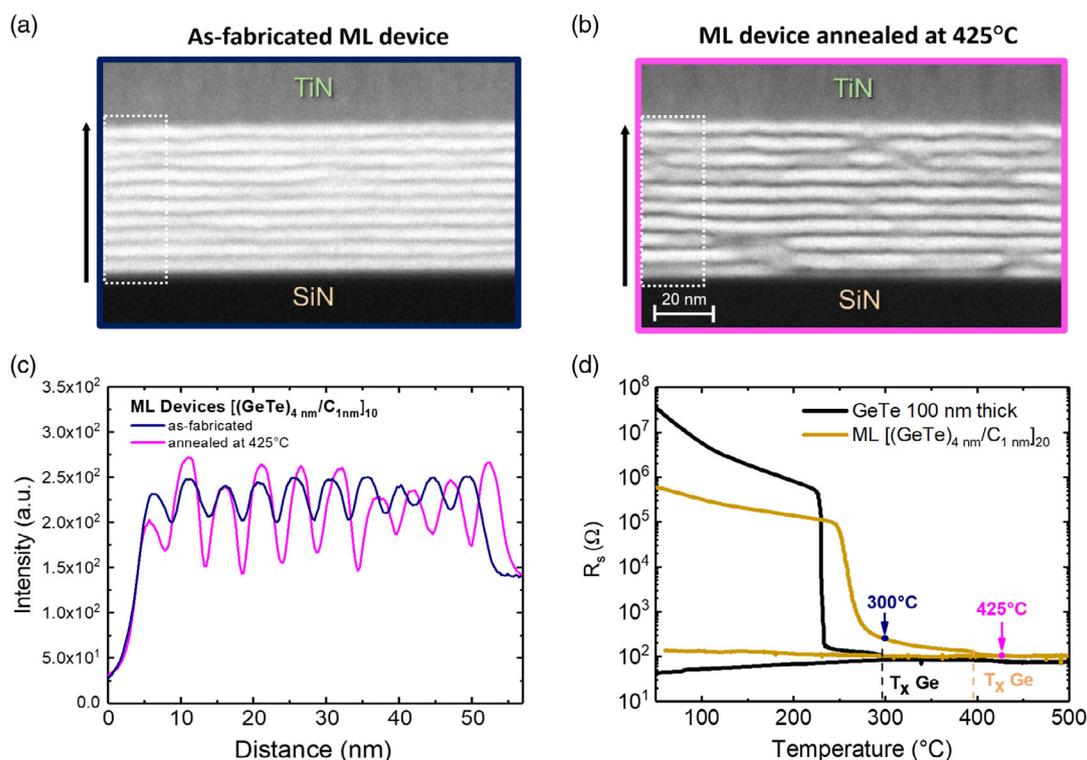


Figure 1. High-angle annular dark-field scanning transmission electron microscope (HAADF-STEM) images of [(GeTe)_{4 nm}/C_{1 nm}]₁₀ multilayers (MLs) integrated in a) an as-fabricated memory device (annealed at 300 °C for 15 min during fabrication) and b) a device further annealed at 425 °C for 15 min. As the devices were previously programmed in the high resistance (RESET) state following the procedure described in the text, the images were acquired away from the heater to study the pristine state of the ML. For each device, the displayed area is on the left side of the image in **Figure 3**, which shows the whole device. The bright layers correspond to the GeTe layers and the dark ones to the C layers. The bottom layer under the ML is a dielectric SiN layer and the top layer is the TiN electrode. c) Intensity profiles integrated in the white dashed frames shown in (a) and (b) along the direction indicated by a black arrow (a) and (b). d) Sheet resistance as a function of temperature of a [(GeTe)_{4 nm}/C_{1 nm}]₂₀ film and of a 100 nm thick GeTe film for comparison. The initially amorphous films (deposited at room temperature) were heated and cooled by using a ramp of 10 °C min⁻¹. A slight drop in resistance (indicated by a dashed line) is observed after GeTe crystallization in both films. It corresponds to the crystallization of the excess of germanium. The arrows indicate the annealing temperatures of as-fabricated (blue arrow) and annealed (pink arrow) ML devices.

between the bright GeTe layers and the dark C layers are almost flat. In the HAADF mode, the contrast is mainly the result of the Z differences between the chemical elements, with an intensity $I \sim Z^{1.7}$, and thus brighter areas correspond to heavier atoms.^[9] The GeTe layers in the as-fabricated device are crystalline, as evidenced by nano-beam electron diffraction (NBED, see later). An X-Ray diffraction pattern measured on a [(GeTe)_{4 nm}/C_{1 nm}]₂₀ reference film previously annealed at 300 °C for 15 min (Figure S1, Supporting Information) shows the diffraction peaks of the rhombohedral α -GeTe phase.^[10] This result was expected from temperature-resolved sheet resistance measurements of a [(GeTe)_{4 nm}/C_{1 nm}]₂₀ reference film showing a drop in resistance at ≈ 258 °C upon heating (Figure 1d). By comparison, the crystallization of a 100 nm thick GeTe film, deposited in the same sputtering conditions as the GeTe layers in the ML, occurs at ≈ 230 °C. The slight increase in T_x , from ≈ 230 °C for the 100 nm thick GeTe film to ≈ 258 °C for 4 nm thick GeTe layers in the [(GeTe)_{4 nm}/C_{1 nm}]₂₀ ML film, can be explained by a scaling effect. Indeed, decreasing the thickness of GeTe films under 20 nm is known to result in an increase of the crystallization temperature, as shown in ref. [11] and references therein. This increase in T_x is due to the stress gradient exerted by the capping layer onto the PCM layer, which delays its crystallization in the case of very thin films. In the present case of 4 nm thick GeTe layers in the GeTe/C ML, the stress exerted by the 1 nm thick C layers on the GeTe layers is expected to be quite low compared to that induced by thicker and harder SiN layers in ref. [11] leading to only a slight increase in T_x . Note that similar thickness effects on T_x have been reported in Ge₂Sb₂Te₅/C MLs.^[8] These results show that a well-defined and regular ML structure, with crystallized GeTe layers alternating with amorphous C layers is retained in PCM devices at the end of the integration process.

An HAADF-STEM image of a pristine [(GeTe)_{4 nm}/C_{1 nm}]₁₀ ML in a device annealed at 425 °C (Figure 1b) shows that the overall ML structure is still present but localized defects, absent in the as-fabricated device, have appeared. A local disappearance of a GeTe layer, accompanied by the junction of the lower and upper dark C layers over a lateral length of a few nanometers, is observed in several places of the ML in the annealed device. This observation suggests that annealing at 425 °C has promoted the diffusion of C and possibly of Ge excess atoms (see later) at the GeTe grain boundaries. In addition, the contrast between the bright GeTe and the dark C layers is stronger in the case of the device annealed at 425 °C in Figure 1b than in the case of the as-fabricated device in Figure 1a. A comparison between intensity profiles (Figure 1c) allows to quantify this difference. The intensity profile of the annealed device was integrated in an area of the HAADF-STEM image in Figure 1b where almost no defects are detected. To account for the difference in foil thickness, the intensity profiles of the as-fabricated and annealed devices are normalized so that the total integrated intensity is similar for both samples. The average contrast between GeTe and C layers increases by a factor ≈ 2 after annealing at 425 °C. One difference between MLs, in as-fabricated and annealed devices, is the presence of crystallized Ge after annealing at 425 °C, as explained hereafter. The measured Ge/Te ratio in the GeTe layers in the ML is found slightly larger than 1 (Table S1, Supporting Information), as usually the case for GeTe films deposited by

sputtering of a stoichiometric GeTe target,^[12] whereas the crystalline GeTe phase is slightly deficient in Ge.^[13] In GeTe films, amorphous Ge precipitates are formed during the crystallization of GeTe and they crystallize upon heating to a higher temperature.^[14] The crystallization of excess Ge, marked by a small drop in resistance (Figure 1d and S2, Supporting Information), occurs at ≈ 297 °C in the GeTe film and at ≈ 395 °C in the [(GeTe)_{4 nm}/C_{1 nm}]₂₀ reference film. An X-Ray diffraction pattern measured on a [(GeTe)_{4 nm}/C_{1 nm}]₂₀ film annealed at 425 °C clearly shows weak intensity diffraction peaks of the cubic Ge phase coexisting with the diffraction peaks of the rhombohedral α -GeTe phase (Figure S3, Supporting Information). In the as-fabricated devices, some of the excess Ge atoms rejected during the crystallization of the GeTe phase may have diffused preferentially to the C layers since the formation of Ge—C bonds is favorable, as previously shown in case of amorphous C-doped GeTe films.^[15] For annealing temperatures above 395 °C, the crystallization of Ge should lead to diffusion of the Ge atoms out of the C layers to finally form isolated Ge crystallites and pure C layers. This explains the difference in contrast between the HAADF-STEM images of MLs in the as-fabricated and annealed devices. Another difference between intensity profiles of the two devices can be observed in Figure 1c. The total thickness of the ML increases by about 3 nm after annealing at 425 °C. The increase in the total thickness must be correlated to an increase in the average size of GeTe crystallites in the direction perpendicular to the layers when the annealing temperature increases, observed by X-Ray diffraction on a [(GeTe)_{4 nm}/C_{1 nm}]₂₀ ML.

The electrical characteristics of [(GeTe)_{4 nm}/C_{1 nm}]₁₀ ML memory devices were measured by following the test procedure described in Experimental Section. The median R - I (Resistance of the memory cell as a function of the current flowing through the memory cell during the programming pulse) curves shown in Figure 2a were obtained from measurements on 26 as-fabricated devices and 20 devices annealed at 425 °C for the first RESET operation, that is, the switching from the pristine SET state to the RESET state. The individual R - I curves are shown in Figure S4, Supporting Information. In the pristine state, where the ML is entirely crystallized, the median resistance of the devices is low (3.1 k Ω for as-fabricated devices and 4.5 k Ω for devices annealed at 425 °C). Given the dispersion of device resistances, no significant change in initial resistance is detected between the two types of devices. However, annealing the ML devices after fabrication has a huge impact on their electrical performances. The melting current I_{melting} , which is the current at which the memory cell resistance starts to increase from its initial value, decreases by 36% (from 0.70 to 0.45 mA) after annealing at 425 °C and the RESET current I_{RESET} , at which the memory cell resistance reaches a high-resistance plateau, decreases by 46% (from 1.40 to 0.75 mA). In addition, the median resistance of memory cells in the RESET state of devices annealed at 425 °C (≈ 4 M Ω) is one order of magnitude higher than that of as-fabricated devices (≈ 250 k Ω). The electrical characteristics of ML devices were compared to those of similar memory devices incorporating a 50 nm thick layer of the archetypical phase-change material Ge₂Sb₂Te₅. The median R - I curve obtained on 15 Ge₂Sb₂Te₅ devices for switching from the SET state to the RESET state is shown in Figure 2a. The transition from the SET state to the RESET state is steeper in the case

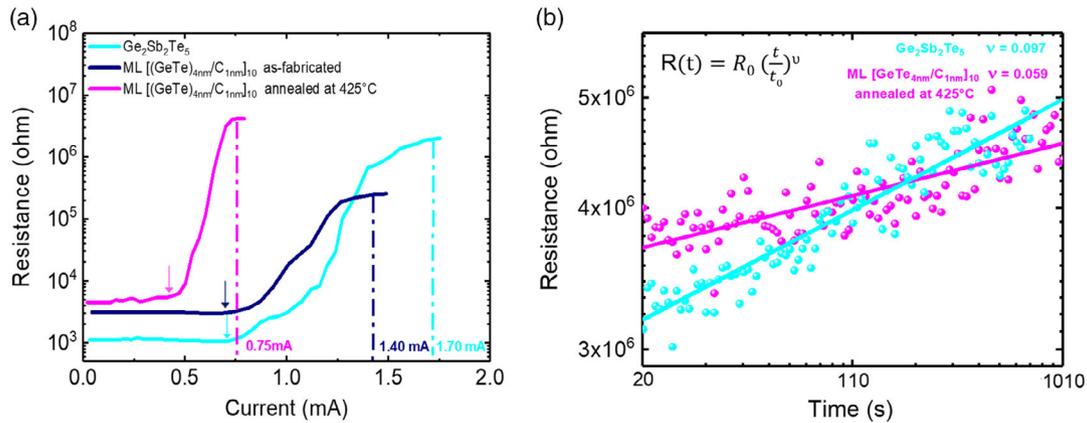


Figure 2. a) Median R – I curves for the first RESET operation for 26 as-fabricated $[(\text{GeTe})_{4\text{ nm}}/\text{C}_{1\text{ nm}}]_{10}$ ML devices and 20 ML devices annealed at 425 °C for 15 min, compared to median R – I curves for 15 $\text{Ge}_2\text{Sb}_2\text{Te}_5$ devices with the same memory cell architecture. The median RESET currents are indicated by dashed-dotted lines and the median melting currents by arrows. b) Resistance as a function of time for a $[(\text{GeTe})_{4\text{ nm}}/\text{C}_{1\text{ nm}}]_{10}$ ML device annealed at 425 °C and a $\text{Ge}_2\text{Sb}_2\text{Te}_5$ device in the RESET state. The origin of time is taken at the end of the RESET operation. The solid lines are fits of the data for $20 \leq t \leq 1000$ s by $R(t) = R_0 \left(\frac{t}{t_0}\right)^\nu$, where $R(t)$ is the resistance at time t and R_0 is the resistance at time t_0 .

of the $[(\text{GeTe})_{4\text{ nm}}/\text{C}_{1\text{ nm}}]_{10}$ ML devices annealed at 425 °C than in as-fabricated $[(\text{GeTe})_{4\text{ nm}}/\text{C}_{1\text{ nm}}]_{10}$ ML and $\text{Ge}_2\text{Sb}_2\text{Te}_5$ devices. The median RESET current in annealed $[(\text{GeTe})_{4\text{ nm}}/\text{C}_{1\text{ nm}}]_{10}$ ML devices (≈ 0.75 mA) is reduced by $\approx 55\%$ with respect to its value in $\text{Ge}_2\text{Sb}_2\text{Te}_5$ devices (≈ 1.70 mA). This is a promising result. From literature data, the RESET current of GeTe and $\text{Ge}_2\text{Sb}_2\text{Te}_5$ devices is similar and doping GeTe with C reduces the RESET current by $\approx 30\%$ for a C content of 10 at%.^[4] In addition, the resistance window is almost the same in ML devices annealed at 425 °C and $\text{Ge}_2\text{Sb}_2\text{Te}_5$ devices, in contrast with C-doped GeTe or $\text{Ge}_2\text{Sb}_2\text{Te}_5$ devices for which a reduction in the resistance window of up to more than a factor of 3 is observed.^[5,6] Note that $[(\text{GeTe})_{4\text{ nm}}/\text{C}_{1\text{ nm}}]_{10}$ has similar performance as the so-called “interfacial Phase-Change Memories” (iPCM) in terms of RESET current reduction.^[16,17] Thus, ML devices annealed at 425 °C show promising properties in terms of I_{RESET} reduction for the development of high-density PCMs.

To further increase the density of information in PCM, encoding multiple resistance levels in the same memory point, that is, “multi-level storage” is currently being studied.^[18] In PCM, the resistance of the amorphous state increases with time (drift phenomenon). The drift of a PCM cell must be as low as possible to ensure the reliability of the multilevel cell (MLC) technology. The resistance drift is ascribed to a structural relaxation of the amorphous phase with aging but its precise origin in amorphous chalcogenide phase-change materials is still debated.^[19–21] The drift phenomenon is usually described by an empirical power law $R(t) = R_0 \left(\frac{t}{t_0}\right)^\nu$, where $R(t)$ is the resistance at time t , R_0 is the resistance at time t_0 , and ν the drift exponent.^[22] To investigate the drift of $[(\text{GeTe})_{4\text{ nm}}/\text{C}_{1\text{ nm}}]_{10}$ devices annealed at 425 °C, the $R(t)$ curves of 6 ML devices were measured after the RESET operation. One curve is shown in Figure 2b. For $20 \leq t \leq 1000$ s, the measured $R(t)$ curves can be fitted by a power law. This is not the case for the time interval (0–20 s), which corresponds to an incubation period.^[23] The drift coefficient ν shows an appreciable dispersion from one memory device to another, ν varies from

0.038 to 0.122, with an average value equal to 0.059 and a standard deviation of ± 0.029 . These values are lower than some literature values for melt-quenched $\text{Ge}_2\text{Sb}_2\text{Te}_5$. However, the ν values reported in the literature vary significantly, as shown in ref. [23,24] and references therein. Thus, we also measured the resistance drift in the RESET state for 6 $\text{Ge}_2\text{Sb}_2\text{Te}_5$ devices with the same memory cell architecture as the ML devices. The obtained ν values vary from 0.067 to 0.144, with an average value equal to 0.097 and a standard deviation of ± 0.025 . The drift coefficient measured in $[(\text{GeTe})_{4\text{ nm}}/\text{C}_{1\text{ nm}}]_{10}$ devices is thus smaller than in $\text{Ge}_2\text{Sb}_2\text{Te}_5$ devices with the same architecture. This result is also in good agreement with the observation of ref. [8] in which a drift coefficient as low as 0.06 was obtained for their single $\text{Ge}_2\text{Sb}_2\text{Te}_5$ 6 nm/ $\text{C}_{0.5\text{ nm}}$ ML device to be compared with 0.17 for their $\text{Ge}_2\text{Sb}_2\text{Te}_5$ device.

To understand the origin of the difference in I_{RESET} between as-fabricated $[(\text{GeTe})_{4\text{ nm}}/\text{C}_{1\text{ nm}}]_{10}$ ML devices and ML devices annealed at 425 °C, as well as the low drift value of the devices annealed at 425 °C, HAADF-STEM images of memory devices, previously switched from the initial state to the RESET state by same the procedure used for R – I measurements in Figure 2a, were acquired (Figure 3). In addition, electron energy loss spectroscopy (EELS) maps of C, Ge, and Te acquired in an area located above the heater are shown in Figure 3. For the as-fabricated device (Figure 3a), the HAADF-STEM image shows that the structure of the ML is strongly affected by the RESET operation over almost the entire thickness of the ML and over a lateral extension of ≈ 80 – 100 nm centered on the heater. In this area, the C and GeTe layers are curved. In some places, the C layers are absent and thicker GeTe layers (thickness 8 to 10 nm) are observed. The EELS maps confirm these observations and in addition show a depletion in C in a small area above the heater (lateral extension of ≈ 70 nm and height of 8 nm). Ge enrichment is detected in an even smaller area. The HAADF-STEM image of an ML device annealed at 425 °C (Figure 3b) reveals striking differences from that of the as-fabricated ML device. The area centered

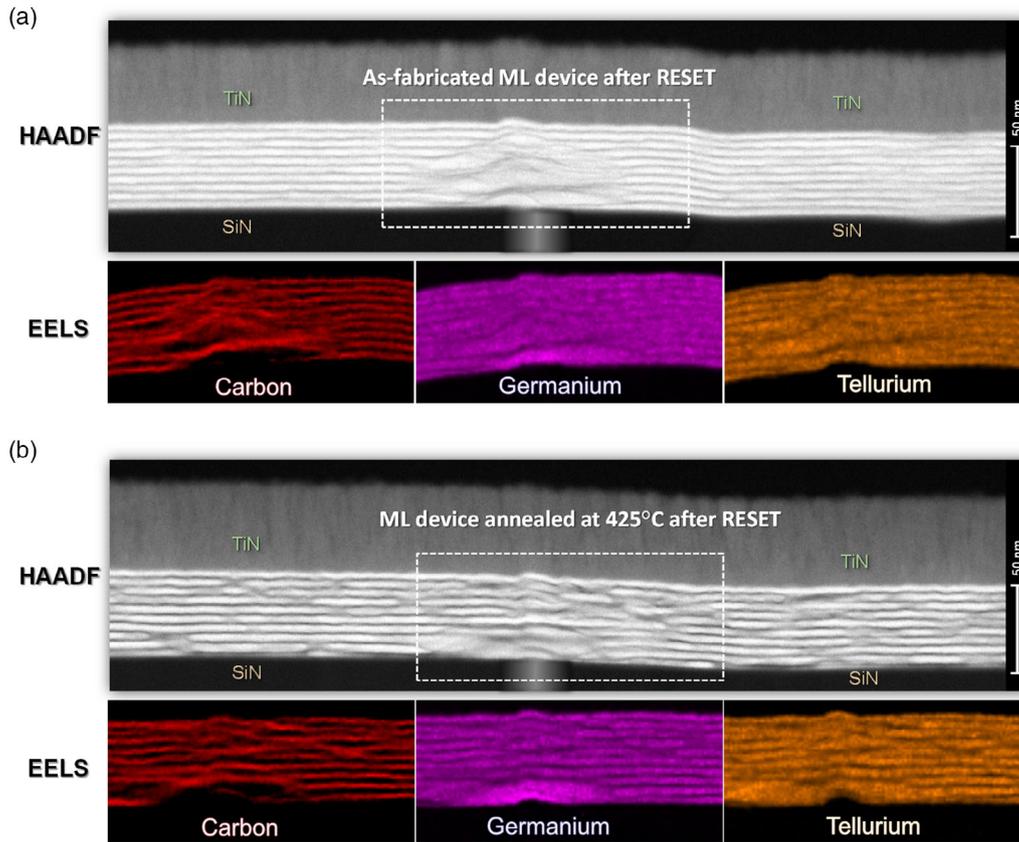


Figure 3. HAADF-STEM images and electron energy loss spectroscopy (EELS) maps of a $[(\text{GeTe})_{4 \text{ nm}}/\text{C}_{1 \text{ nm}}]_{10}$ ML device in a) the as-fabricated state and of b) an ML device annealed at 425 °C. The devices were previously programmed in the RESET state following the procedure described in the Experimental Section. The EELS maps are acquired in the dashed white frames (shown in the HAADF-STEM images) located above the heater that is schematically represented by a gray rectangle.

on the heater in which the structure of the ML is affected by the RESET operation is much smaller. GeTe layers separated by C layers are still observed in the upper part of the ML above the heater, with the same nanostructure as in the left and right parts of the HAADF-STEM image showing the pristine state of the ML annealed at 425 °C. The EELS maps highlight that only the first two layers of GeTe and C above the heater are affected by the RESET operation and over a 70 nm lateral extension centered on the heater with a vertical height of 8–9 nm. This area is enriched in Ge, depleted in C and surrounded by a C shell. Furthermore, outside the area affected by the RESET operation, the Ge EELS map shows alternating light and dark layers, where the dark layers correspond to the C layers in the C EELS map. In the case of the as-fabricated device, the contrast is much lower, suggesting the presence of Ge atoms in the C layers, in agreement with the interpretation of the HAADF STEM image given before.

NBED mapping was performed to distinguish crystalline areas from amorphous areas (Figure 4). A custom Python script based on template matching was written to locate the diffraction spots and then extract their intensities. Displayed intensities are finally normalized to one with respect to the maximum value in the map. The resulting Python-processed NBED maps thus exhibit an intensity contrast related to the crystalline phase content in

each pixel. Note that the relation is not strictly proportional as the diffracted intensity depends on the crystal orientation as well. A purple pixel corresponds to an amorphous area, or possibly an area containing only nanocrystals, while a yellow/green pixel corresponds to a crystalline area. For each device, the contour of the amorphous areas extracted from the script was drawn on the HAADF-STEM image to show the entire amorphous area after the RESET operation. The sizes and shapes of the amorphous area are very different in the two devices. The height of the amorphous area reaches ≈ 30 nm in the case of the as-fabricated device, to be compared to only ≈ 8 nm in the device annealed at 425 °C. The lateral size is almost the same in the two devices, of the order of 80–100 nm. Note that a change in the electrical resistivity of the amorphous state likely occurred between the two ML structures, since a smaller amorphous dome produces a higher resistance, in the ML device annealed at 425 °C compared to the as-fabricated device. The presence of carbon inside the amorphous dome, observed in the as-fabricated device, could explain a lower electrical resistivity of the amorphous phase since amorphous carbon is more conductive than the amorphous GeTe phase. Although the ML structure disappeared in the amorphous region after a single RESET operation in the 425 °C annealed ML, the reduction in programming current appears

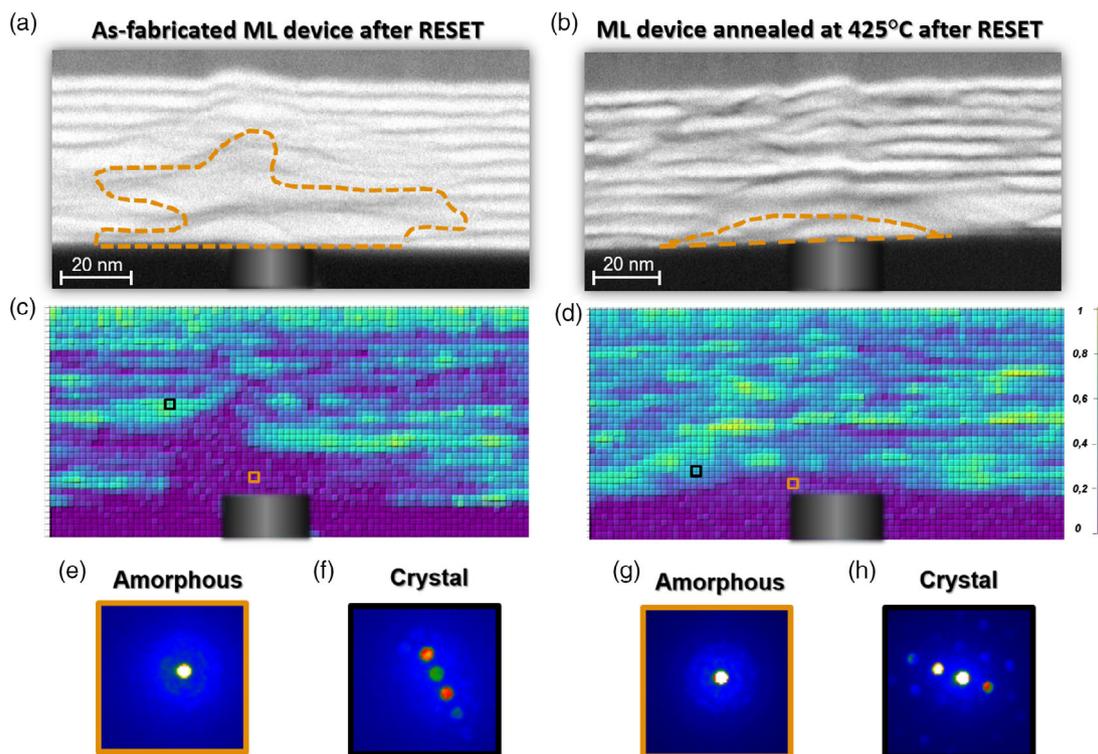


Figure 4. a,b) HAADF-STEM images coupled with c,d) nano-beam electron diffraction (NBED) mapping of as-fabricated and annealed $[(\text{GeTe})_{4\text{ nm}}/\text{C}_{1\text{ nm}}]_{10}$ ML devices programmed in the RESET state. The heater is schematically represented by a gray rectangle. The intensity scale of the NBED maps (color bar given on the right side) is related to the crystalline phase content in each pixel. The mapping is processed by a custom Python™ script: see text for more information. e–h): NBED patterns acquired in selected groups of 4 pixels indicated in the NBED maps. In (e) and (g), only diffuse intensity rings due to an amorphous structure are observed, while in (f) and (h) diffraction spots are observed. For each device, the contour of the amorphous area extracted from the NBED map is drawn as a dashed line in the HAADF-STEM image.

to have been preserved up to 10^6 cycles, as shown in Figure S5 of the Supporting Information. The SET-RESET programming operation could be reproduced during 10^6 successive programming cycles, with a resistance contrast of more than one order of magnitude between the resistances of the SET and RESET states. This result shows that thermal confinement is maintained by the undamaged ML structure surrounding the amorphous region.

3. Discussion

The very small amorphous area in the RESET state of the $[(\text{GeTe})_{4\text{ nm}}/\text{C}_{1\text{ nm}}]_{10}$ ML device annealed at $425\text{ }^\circ\text{C}$ shows that the heat was efficiently confined during the RESET operation. The heat confinement in the direction normal to the layers is much stronger than in as-fabricated ML devices.^[1] This observation must be correlated with the fact that ML devices annealed at $425\text{ }^\circ\text{C}$ exhibit a significantly lower melting current and RESET current than as-fabricated ML devices. For a given device architecture, I_{melting} depends on the resistance of the device when the phase-change material is crystalline (R_{SET}), the phase change being the result of the Joule power dissipated at the phase-change material/heater interface.^[1] R_{SET} corresponds to the sum of the resistance of the phase-change material, the resistance of the

heater and all contact resistances.^[1] I_{melting} also depends on the melting temperature T_m of the phase-change material and on the thermal conductivity of the memory cell and hence of the crystalline state K_{th} , because in PCM devices a significant part of the heat is lost during programming by thermal dissipation in the phase-change material and thus away from the active region.^[1,3] As mentioned earlier, no significant change in R_{SET} is detected between as-fabricated ML devices and devices annealed at $425\text{ }^\circ\text{C}$. Thus, only a decrease in the K_{th} of the crystalline ML film can explain the reduction of I_{melting} . The thermal conductivity K_{th} of the ML is the sum of an electronic contribution ($K_{\text{th}}^{\text{electronic}}$), proportional to the electrical conductivity σ , and a contribution due to atomic vibrations ($K_{\text{th}}^{\text{phonon}}$). The latter is expected to depend on the nature and thickness of the layers and on their interfaces. In addition, in an ML structure, one can expect differences between the in-plane and out-of-plane electronic and phonon contributions ($K_{\text{th}}^{\text{electronic}}$ and $K_{\text{th}}^{\text{phonon}}$). No change in σ is expected in out-of-plane direction, since as-fabricated devices and devices annealed at $425\text{ }^\circ\text{C}$ have similar R_{SET} values. In the in-plane direction, a small increase of σ is observed in Figure 1d when the annealing temperature increases from 300 to $425\text{ }^\circ\text{C}$. Therefore, only a decrease in $K_{\text{th}}^{\text{phonon}}$ could be at origin of a decrease of K_{th} , and hence a decrease of I_{melting} in ML devices annealed at $425\text{ }^\circ\text{C}$ with respect to as-fabricated devices. One way to decrease $K_{\text{th}}^{\text{phonon}}$ is to reduce the mean free

path of phonons through introduction of scattering centers with a density close to their mean free path.^[25–27] Phonons with wavelengths comparable to the nanostructure length scale will be scattered by interfaces and more generally heterogeneities at the nanometer or sub-nanometer scales.^[28] X-Ray diffraction experiments (through a determination of the diffractive coherent domain (DCD) by using the Scherrer's law) show only a minor change (about 15% increase) in lateral crystallite size when the annealing temperature is increased from 300 to 425 °C. This result excludes a significant increase in the number of grain boundaries between as-fabricated ML devices and devices annealed at 425 °C. Then, the most probable origin of the decrease of K_{th}^{phonon} must be related to a change in the structure and/or the nature of interfaces between the GeTe and C layers induced by annealing at 425 °C. Indeed, the contrast between GeTe and C layers in the devices is significantly increased after annealing at 425 °C, as evidenced earlier (Figure 1c and 3). These changes in contrast are attributed to the presence of Ge atoms in the C layers in the as-fabricated device but not in the device annealed at 425 °C. As Ge diffusion out of the C layers increases the mass density difference between the GeTe and C layers, it is expected that the differences in vibrational modes between the two layers increase, which increases phonon scattering and reduces K_{th}^{phonon} in the out-of-plane direction.

In summary, a decrease of the thermal conductivity (K_{th}) of the ML due to a reduction of phonon thermal conductivity (K_{th}^{phonon}) resulting from an enhanced out-of-plane phonon scattering seems to be the most plausible explanation of the decrease of $I_{melting}$ in ML devices annealed at 425 °C with respect to as-fabricated devices. Thanks to a better heat confinement, the ML devices annealed at 425 °C exhibit an amorphized volume that is three times smaller than that observed in the as-fabricated ML devices (Figure 4). This decrease of the melted volume is consistent with the reduction of I_{RESET} required to reach the RESET state. Finally, one must note that for a given material, the drift coefficient measured in a memory device depends also on the volume of the amorphous dome above the heater.^[29,30] Thus, the small size of the amorphized region in the ML devices annealed at 425 °C (Figure 4b) could explain their low drift coefficient. However, to achieve multilevel storage in ML devices annealed at 425 °C, the applied current density must be finely controlled because the transition from the SET state to the RESET state is very abrupt (Figure 2a).

4. Conclusion

In conclusion, phase-change nanocomposites consisting in [(GeTe)_{4 nm}/C_{1 nm}]₁₀ MLs are promising candidates for low-power PCM thanks to their unique and controllable nanostructure. Indeed, a significant decrease of about 55% of the RESET current compared with the well-known Ge₂Sb₂Te₅ alloy can be achieved in ML-based PCM devices. The origin of these performance improvements over standard polycrystalline phase-change thin films seems to be the result of a decrease in out-of-plane lattice thermal conductivity in the ML due to increased phonon scattering, resulting from a high density of GeTe/C interfaces, since the two materials have very different vibrational properties. In addition, the resistance drift of the RESET state is significantly smaller in ML devices than in

Ge₂Sb₂Te₅ devices opening further opportunities for use of ML in multilevel cell devices. In the future, data retention and endurance of ML devices need to be investigated and will be the subject of future studies. Finally, all the features shown before in ML memory devices are promising to develop the next generation of PCM, as well as using the concept of nanocomposites for a wide range of applications requiring to master the thermal conductivity, for instance in thermoelectric devices.

5. Experimental Section

Sample Preparation: Amorphous [(GeTe)_{4 nm}/C_{1 nm}]_n ML films were deposited at room temperature by alternating magnetron sputtering of pure C and GeTe targets. In memory devices, MLs with $n = 10$ were deposited above a TiN bottom electrode (heater with an L-shape plug) surrounded by a SiN dielectric layer, and then covered by a planar upper TiN electrode. During additional steps of device fabrication, the MLs were heated at 300 °C for about 15 min. For characterization purposes, reference ML films with $n = 20$ were deposited on Si substrates, previously deoxidized by Ar sputtering, and on Si substrates covered by a 500 nm thick SiO₂ layer obtained by thermal oxidation. These films were capped in situ with a 10 nm thick SiN layer to avoid oxidation. The sheet resistance of the film deposited on SiO₂ was measured as a function of temperature by the four-point probe technique. The initially amorphous films were heated up to 500 °C at a rate of 10 °C min⁻¹ and then cooled down to room temperature at the same rate. The four probe tips were applied directly to the film surface through the 10 nm SiN layer.

STEM: Electron transparent cross-sectional foils of [(GeTe)_{4 nm}/C_{1 nm}]₁₀ MLs in memory devices were prepared by focused Ga⁺ ion beam milling. They were thinned using first a conventional operating voltage of 30 kV and then a voltage in the 5–8 kV range to reduce surface damage on each side of the foil. The final thickness of the foil was estimated to be of around 60 nm. HAADF-STEM images were acquired on a probe Cs-corrected TFS (Thermo Fisher Scientific) Titan Themis microscope operating at 200 kV. To prevent the specimen from any damage due to electron irradiation, HAADF images were obtained using a low beam current, typically below 20 pA. Nano beam electron diffraction (NBED) patterns were obtained with a second condenser aperture of 30 μm providing a convergence angle of ≈5 mrad and a spot size of ≈2 nm. STEM EELS maps of Ge, Te, and C were acquired using a Quantum Gatan Imaging Filter (GIF) in dual-EELS mode from 200 to 2100 eV with a dispersion of 0.5 eV per channel.

Electrical Characterization of PCM Devices: R – I characteristics of PCM devices (with R the resistance of the memory cell and I the current applied during the programming pulse) were measured in pulsed mode by applying successive square programming pulses of increasing voltage with a fixed width of 300 ns. After each programming pulse, the resistance of the cell was measured at a constant voltage of 0.1 V. To limit the current flowing through the device, a resistance of 2.2 kΩ was connected in series with the PCM device. For ML devices, the R – I curves in Figure 2a correspond to the first RESET operation, from the pristine state (low resistance state [SET state]) to the RESET. The R – I curves of Ge₂Sb₂Te₅ devices in Figure 2a were measured after an initialization RESET-SET cycle to obtain reproducible memory performances.

The drift of the resistance of memory cells in the RESET state was measured as a function of time. The devices were first programmed in the RESET state by the same procedure used for R – I measurements in Figure 2a. Then, 20 s after the end of the RESET operation, the resistance of the device was measured as a function of time during 1000 s at a constant voltage of 0.2 V.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

C, GeTe, multilayers, nanocomposites, phase-change memory, STEM

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