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Elucidation of the Density of States for Polycrystalline Silicon Vertical Thin-Film Transistors

Peng Zhang¹, Emmanuel Jacques², Régis Rogel, Laurent Pichon²,
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Abstract—The polycrystalline silicon vertical thin-film transistors (TFTs) with different active layer thicknesses of 150 and 300 nm were fabricated by a five-mask process and electrically characterized. The vertical TFT with 150-nm active layer thickness shows comprehensive advantages over its counterpart with 300-nm active layer, especially with a higher I_{ON}/I_{OFF} current ratio of more than 10^6 and higher field-effect mobility, excluding the access resistance effect. The electrical parameters were analyzed by the density of states (DOS) calculation, and smaller DOS is deduced for the device with 150-nm active layer for the same energy level. The detailed elucidation of the DOS was analyzed by introducing the intrinsic mobility and the grain boundary barrier height at the flat-band state, which gives the detailed expressions for the DOS. Polycrystalline silicon lateral TFT was also introduced to verify this evaluation method.

Index Terms—Access resistance, density of states (DOS), intrinsic mobility, polycrystalline silicon, threshold voltage, vertical thin-film transistors (TFTs).

I. INTRODUCTION

POLYCRYSTALLINE silicon thin-film transistors (TFTs) have been widely adopted in industry fields for driving different types of displays, such as in E-ink electrophoretic displays (EPDs) [1], active-matrix liquid crystal displays (AMLCDs) [2], and active-matrix organic light-emitting diodes displays (AMOLEDs) [3], and also own potential applications in radio frequency identification (RFID) tags [4], X-ray detectors [5], sensors [6], and so forth. The flexible and transparent display might be the development directions for future display domains, where organic small molecular

and polymer TFTs own the advantage of flexibility and IGZO TFTs own the advantage of transparency. However, for the mainstream displays, the polycrystalline silicon TFTs show certain advantages over organic TFTs and IGZO TFTs, such as high ambient stability and bias stress stability, as well as high field-effect mobility and mature industrial production line, which is required especially for high-resolution displays. In addition, for these display applications, one objective focuses on the improvement of the driving current with reduced power consumption. The main approach of obtaining larger driving current lies in the improvement of field-effect mobility by well controlling the polycrystalline silicon morphology, such as adopting excimer laser annealing (ELA) [7] of the predeposited amorphous Si layer, or by other methods such as using metal-induced lateral crystallization (MLC) method [8]; however, the two crystallization methods own disadvantages. In previous work, solid-phase crystallization (SPC) method has been adopted in our group with a processing temperature of 600 °C that supports the processing on specific glass substrates, such as on Corning 1737 glass substrates, while the field-effect mobility exceeds $100 \text{ cm}^2/\text{V} \cdot \text{s}$ with a current ratio exceeding 10^7 , indicating high-quality polycrystalline silicon active layer [9].

From another aspect, the driving current can also be amplified with higher channel width/length ratio, and considering the high aperture ratio requirement for higher luminance, short-channel length is preferred. From our previous work, 3-D vertical TFTs based on SPC polycrystalline silicon active layers have been proposed, with the aim of improving current ratio by introducing an insulating barrier layer between source and drain, and thus suppress the large source–drain overlapping area [10], [11]. In addition, the vertical configuration also enables high flexibility since the channel direction is perpendicular to the substrate surface. However, from previous work, even adopting the polycrystalline silicon active layer crystallized by SPC, the field-effect mobility of the vertical TFT is approximately one order lower than their lateral counterpart, which is supposed to be due to the etched rough sidewall and the small grain size of the polycrystalline silicon film grown vertically on the rough sidewall, where the growth kinetics may be different from the lateral growth [11]. In addition, further enhancement of current ratio is preferred for realizing high-resolution displays.

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In this article, optimized vertical TFTs are proposed by involving an insulating layer between source and drain, and the electrical characteristics are simply analyzed. Elucidation of the low field-effect mobility is also proposed based on the density of states (DOS) analysis. In order to verify this special DOS method, a different method adopting threshold voltage calculation is proposed, verifying the accuracy of the DOS expression. In addition, polycrystalline silicon lateral TFT was also introduced to further verify the accuracy of this evaluation method.

II. DEVICE FABRICATION

The fabrication of the polycrystalline silicon vertical TFTs was carried out as follows. Monocrystalline silicon wafers were initially employed as the substrates to guarantee the endurance of high processing temperature of 600 °C. The substrates were cleaned by a standard RCA cleaning step, following by a deposition step of a thick SiO₂ layer by atmospheric pressure chemical vapor deposition (APCVD) step at 420 °C, in order to prevent the penetration of the impurities from the substrates. Thereafter, four layers were deposited in sequence, which are an n-type heavily doped polycrystalline silicon layer, a 200-nm Si₃N₄ layer, a 1- μ m undoped polycrystalline silicon layer, and finally another n-type heavily doped polycrystalline silicon layer, and all depositions were carried out by low-pressure chemical vapor deposition (LPCVD) method. The combined barrier layers of the 1- μ m undoped polycrystalline silicon layer and the 200-nm Si₃N₄ layer are used between heavily doped polycrystalline silicon layers to facilitate better etching profile as well as to guarantee a sufficient channel length, in order to avoid serious short-channel effects.

Prior to the patterning step, the adjustments of the etching parameters were carried out, and due to the etching selectivity between Si₃N₄ and polycrystalline silicon, the reactive ion etching (RIE) procedure adopts a high power of 50 W, a gas flow of 10 sccm, and a low pressure of 1 mTorr, in order that the physical bombard dominates over the chemical erosion in the RIE process. This enables to form continuous steep sidewalls, as shown in Fig. 1(a), even with certain relief at the Si₃N₄ layer. Fig. 1(b) shows the fabrication procedure of the five-mask process. The first etching step aims to form sidewalls, and then, a second partial etching until reaching the bottom polycrystalline silicon layer was carried out with the aid of a laser interferometer, in order to discriminate source and drain. After that, the undoped polycrystalline silicon active layer was deposited by LPCVD with different thicknesses of 150 and 300 nm and then patterned by a third mask. Afterward, a second RCA cleaning step should be carried out prior to the deposition of gate oxide layer, in order to eliminate most defects at the active layer/gate oxide layer interface. After that, a 70-nm-thick-gate oxide layer is deposited by APCVD, with the fourth mask employed to form source and drain contact holes. Finally, a thick aluminum layer was deposited by thermal evaporation and patterned by the fifth mask and a wet etching step is carried out. Fig. 1(c) shows the 3-D configuration of the two-tooth vertical TFT, and there are four parallel channels at the sidewalls. Fig. 1(d) shows a four-tooth device configuration, where there are eight sidewalls

(channels), and source and drain are well discriminated. All the electrical characterizations were carried out by an Agilent B1500 semiconductor parameters analyzer.

III. RESULTS AND DISCUSSION

The transfer characteristics for the vertical TFTs with different active layer thicknesses of 150 and 300 nm are shown in Fig. 2(a), with a low drain–source voltage of 10 mV, in order to suppress the short-channel effects and reduce power consumption. For the device with higher active layer thickness, the ON-current is approximately 6.7×10^{-6} A, and the OFF-current is approximately 3.8×10^{-11} A, leading to a current ratio of 6.7×10^{-6} A/ 3.8×10^{-11} A in the order of 10^5 . In contrast, when reducing the active layer thickness to 150 nm, the ON-current increases to approximately 9.7×10^{-6} A, while the OFF-current reduces to 4.5×10^{-12} A, leading to a current ratio in the order of 10^6 . The increase of the OFF-current for higher active layer thickness is mainly due to the reduced resistivity of the polycrystalline silicon layer that the larger active layer thickness enables more leakage paths at the flat-band condition (i.e., for the V_{GS} value that approximately corresponds to the lowest current) [12]. In contrast, for the device with low active layer thickness, the higher ON-current is obtained. When the V_{gs} value is smaller than -10 V, the device with a 150-nm active layer shows larger leakage current, which may be due to the thermal (field) emission through the grain boundaries, or with Poole–Frenkel effect [13]. Therefore, higher crystalline quality can be indicated in the device with 150-nm active layer, which increases the leakage current at V_{gs} less than -10 V. In order to demonstrate the effect of the access resistance, a simple extraction method is adopted

$$R_{\text{total}} = \frac{V_{ds}}{I_{ds}} = R_{\text{acc}} + \frac{L}{WC_{\text{ox}}\mu_{\text{FE}}} \frac{1}{V_{gs} - V_{\text{th}}} \quad (1)$$

where R_{acc} is the access resistance, L/W is the channel length/width ratio of $1.2/80 \mu\text{m}$, C_{ox} is the gate capacitance per unit area, μ_{FE} is the field-effect mobility, and V_{th} is the threshold voltage. Prior to the extraction of access resistance, the electrical parameters of the vertical TFTs were obtained and listed in Table I. The access resistance is then calculated, as shown in Fig. 2(b). The channel resistance of the 300-nm active layer is higher than its 150-nm active layer counterpart. For the device with 150-nm active layer, the access resistance is about 500 Ω , which is comparable to the channel resistance at the largest V_{gs} ; however, the access resistance is still not dominant in the total resistance, especially at a lower V_{gs} . Note that, this evaluation method is rather simple, and the accuracy of the access resistance needs to be further verified. In order to prove the effect of the access resistance, the accurate threshold voltage that suppressed the access resistance is proposed by a secondary derivative method, and the accurate threshold voltage is shown as the peak of the secondary derivative curve [14]. From the secondary derivative method, as shown in Fig. 2(c) and (d), the threshold voltages are shown to be 1.7 and 3.1 V, respectively, which is close to the values from the extrapolation method (-0.19 and 0.44 V). Note that, even for 300-nm active layer with smaller

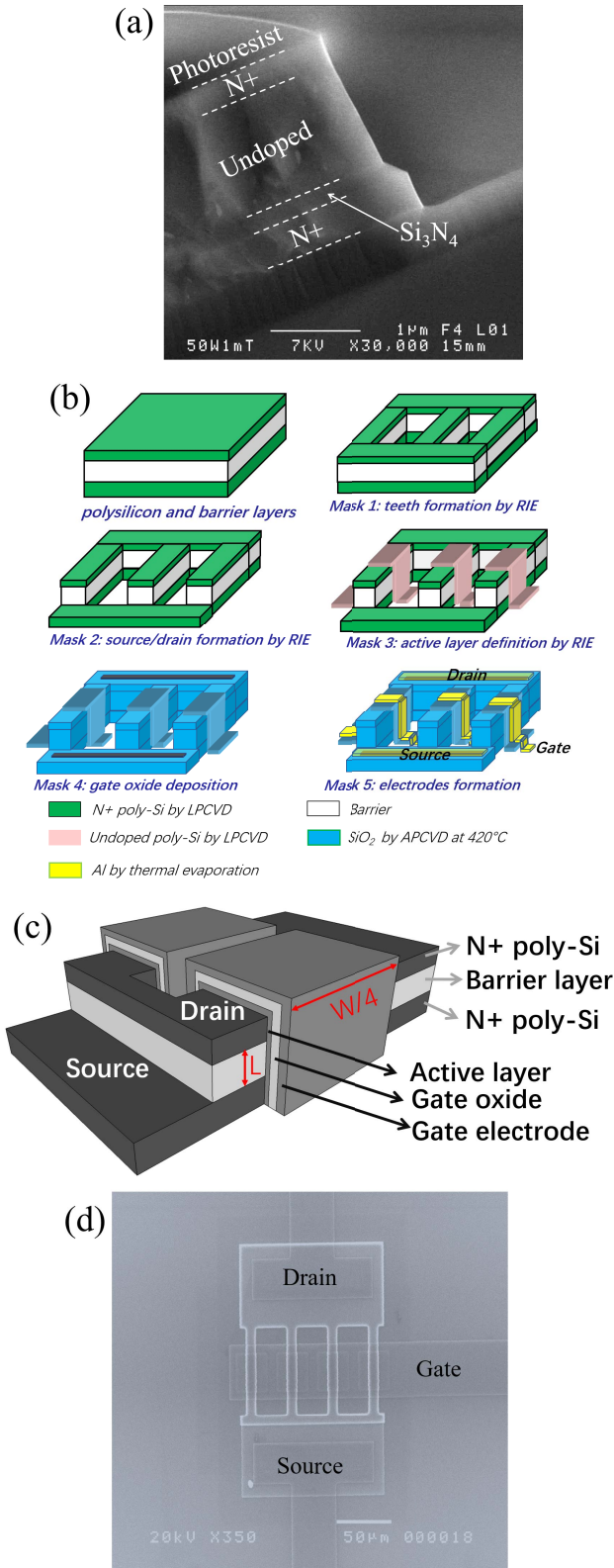


Fig. 1. (a) SEM image of vertical sidewall incorporating Si_3N_4 barrier layer, (b) five-mask fabrication process of the vertical TFT, (c) three-dimensional configuration of a two-tooth vertical TFT, and (d) SEM image of a four-tooth vertical TFT, where eight channels were formed at the sidewalls.

access resistance, the threshold voltage from the secondary derivative method shows a bit difference from the value from the extrapolation method. Therefore, the access resistance

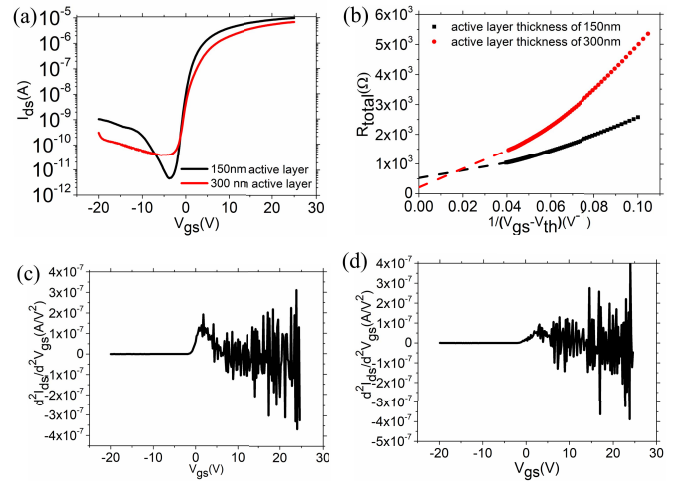


Fig. 2. (a) Transfer characteristics of vertical TFTs based on different active layer thicknesses of 150 and 300 nm, (b) access resistance deductions for the two types of vertical TFTs, the access resistances can be negligible, (c) accurate threshold voltage of 1.7 V for 150-nm active layer thickness, and (d) accurate threshold voltage of 3.1 V for 300-nm active layer thickness.

TABLE I
 ELECTRICAL PARAMETERS DEDUCED FROM TRANSFER CHARACTERISTICS WITH A LOW DRAIN–SOURCE VOLTAGE OF 10 mV

| Active layer thickness (nm) | V_{th} (V) | g_m (μS) | SS (V/dec) | μ_{FE} ($\text{cm}^2/\text{V}\cdot\text{s}$) |
|-----------------------------|--------------|-------------------------|------------|--|
| 150 nm | -0.19 | 0.48 | 0.77 | 14.5 |
| 300 nm | 0.44 | 0.34 | 1.3 | 10.4 |

effect can be negligible, especially at a lower V_{gs} . Indeed, the higher field-effect mobility and the lower subthreshold slope indicate the lower bulk and interface trap densities for the device with 150-nm active layer thickness. Therefore, the access resistance does not play an important role in the total resistance, indicating the appropriate usage of DOS to analyze the electrical performance.

The DOS calculation is based on Suzuki’s theory [15], where the DOS can be calculated following the three formulas:

$$N_{\text{DOS}}(E_F + q\psi_s) = \frac{\epsilon_{\text{Si}}}{2q^2} \frac{\partial^2}{\partial \Psi_s^2} \left[\frac{d\Psi(x)}{dx} \Big|_{x=0} \right]^2 \quad (2)$$

$$\frac{d\Psi(x)}{dx} \Big|_{x=0} = -\frac{\epsilon_{\text{OX}}}{\epsilon_{\text{Si}}} \cdot \frac{V_{\text{GS}} - V_{\text{FB}} - \psi_s}{d_{\text{OX}}} \quad (3)$$

$$d\psi_s = \frac{dG}{G_0} \frac{\epsilon_{\text{OX}}}{\epsilon_{\text{Si}}} \frac{d}{d_{\text{OX}}} \frac{V_{\text{GS}} - V_{\text{FB}} - \psi_s}{\exp\left(\frac{q\psi_s}{kT}\right) - 1} \quad (4)$$

Fig. 3 shows the calculated DOS for the vertical TFTs with different active layer thicknesses of 150 and 300 nm, respectively. The channel thickness is fixed at 10 nm [16]. From the DOS calculation, the tail states are demonstrated, a maximum DOS of approximately $10^{23} \text{ eV}^{-1} \cdot \text{cm}^{-3}$ is obtained for both vertical TFTs. In addition, the closer of the Fermi level to the conduction band due to the band bending indicates higher field-effect mobility of the vertical TFT with 150-nm active layer thickness, being due to that more carriers were closer to the mobility edge that separates the localized states and the delocalized states, which indicates the better crystalline quality of the channel for the 150-nm active layer. In addition, the

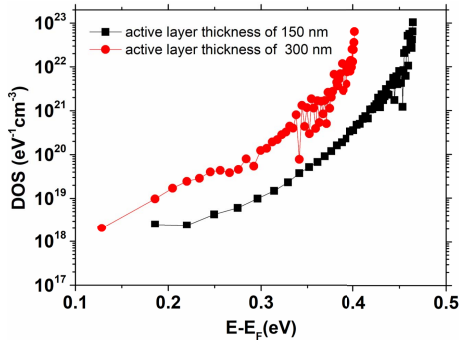


Fig. 3. DOS calculation from the surface potential for the two types of vertical TFTs.

interface trap density should also be low considering a lower subthreshold slope, for the vertical TFT with 150-nm active layer thickness.

From the typical model, the unit-area DOS can also be expressed as [17]

$$\text{DOS} = \frac{N_t}{k_B T_0} \exp\left(\frac{E - E_C}{k_B T_0}\right). \quad (5)$$

It demonstrates the unit-area density of tail states that follows the exponential relationship with the energy level, which can be related to the bulk DOS by dividing by the channel thickness. N_t is the trap density per unit area and T_0 is the characteristic temperature. Therefore, for the device with an active layer thickness of 150 nm, the relationships can be deduced from fitting the DOS of 150-nm device in Fig. 3 with (5) as

$$k_B T_0 = 0.0254 \quad (6)$$

$$\log_{10} N_t - 17.07 \times (E_C - E_F) = 6.27. \quad (7)$$

In contrast, for the device with a higher active layer thickness of 300 nm, the relationships can also be shown by fitting the DOS of 300 nm device in Fig. 3 as

$$k_B T_0 = 0.0344 \quad (8)$$

$$\log_{10} N_t - 12.6(E_C - E_F) = 8.96. \quad (9)$$

On the other hand, the $E_C - E_F$ value can also be deduced for the threshold voltage V_{th} shown as follows [17]:

$$\begin{aligned} V_{th} - V_{FB} &= \varphi \\ &= -\frac{q t_{acc} N_t}{2\pi \epsilon_{ox}} \times \left[\exp\left(-\frac{E_C - E_F}{k_B T_0}\right) \right. \\ &\quad \left. - \exp\left(-\frac{E_g/2 - q\phi_b}{k_B T_0}\right) \right] \\ &\quad \times \ln\left(\frac{2t_{ox} + t_{acc}/2}{t_{acc}/2}\right) \end{aligned} \quad (10)$$

where t_{acc} is the accumulation layer thickness with a value of approximately 10 nm for polycrystalline silicon TFT [16], t_{ox} is the gate oxide thickness with a value of 70 nm, ϵ_{ox} is the gate oxide dielectric constant, which is 3.46×10^{-13} F/cm, and V_{FB} is the flat-band voltage. For polysilicon, the bandgap E_g is approximately 1.12 eV. Therefore, the only unsolved parameter is the grain boundary barrier height Φ_b at the flat-band state, which can be solved as follows.

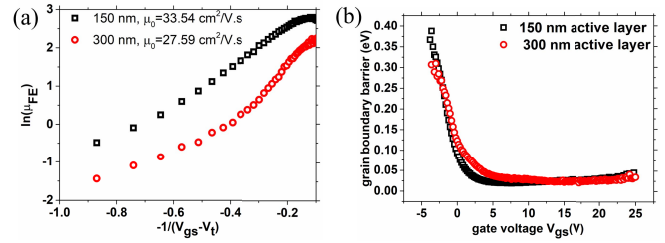


Fig. 4. (a) Deduced intrinsic mobility with $\ln(\mu_{eff}) - (-1)/(V_{gs} - V_t)$ relationship and (b) deduced grain boundary barrier relationship with gate bias, the grain boundary barrier height at the flat-band state can be obtained.

In another reference paper [18], the grain boundary barrier height Φ_b can be elucidated as follows:

$$\overline{\mu_{eff}} = \mu_0 \exp(-\Phi_b/kT) \quad (11)$$

where $\overline{\mu_{eff}}$ can be deduced from the $I-V$ characteristics as follows:

$$I_{ds} = \frac{W}{L} C_{ox} \overline{\mu_{eff}} \left(V_{gs} - V_t - \frac{1}{2} V_{ds} \right) V_{ds} \quad (12)$$

where V_t is the intrinsic threshold voltage of -1.15 V [17]. For the intrinsic mobility of μ_0 , when without considering surface scattering and the grain boundary barrier modulation parameter, it can be deduced from the $\ln(\mu_{eff}) - (-1)/(V_{gs} - V_t)$ relationship [18], as shown in Fig. 4(a). The deduced intrinsic mobility is $33.5 \text{ cm}^2/\text{V} \cdot \text{s}$ for the device with the active layer thickness of 150 nm. In contrast, this value is $27.6 \text{ cm}^2/\text{V} \cdot \text{s}$ for the device with the active layer thickness of 300 nm. Therefore, from (11) and (12), the grain boundary barrier height can be deduced at the flat-band state.

From Fig. 4(b), the grain boundary barrier heights versus the gate voltages were demonstrated. For the device with 150-nm active layer, the grain boundary barrier height is about 0.367 eV at the flat-band state, while for the device with thicker active layer, the corresponding value is about 0.30 eV at the flat-band state. Therefore, from (10), the relationship between N_t and $E_C - E_F$ can be deduced, which are

$$N_t \left[\exp\left(-\frac{E_C - E_F}{0.0254} - 5.01 \times 10^{-4}\right) \right] = -1.53 \times 10^{13} \quad (13)$$

$$N_t \left[\exp\left(-\frac{E_C - E_F}{0.0344} - 5.18 \times 10^{-4}\right) \right] = -1.86 \times 10^{13} \quad (14)$$

for the device with thin or thick active layer, respectively. Therefore, $E_C - E_F$ is deduced to be 0.602 eV for the device with 150-nm active layer, while $E_C - E_F$ equals 0.601 eV for the device with 300-nm active layer, and the nearly same $E_C - E_F$ verifies the accuracy of this evaluation method and the high reproducibility of the fabrication process. As E_F is at the middle of the bandgap, by recalculating (13) and (14) with the omitted exponential term (which is negligible), the nearly same $E_C - E_F$ can also be obtained, indicating the accuracy of the calculation. Even though the polycrystalline silicon active layer shows the intrinsic semiconductor property, the calculation process can also be adopted for the polycrystalline silicon TFTs with doped active layer.

For the device with 150-nm active layer, the grain boundary trap density N_t is approximately $3.04 \times 10^{16} \text{ cm}^{-2}$; in contrast,

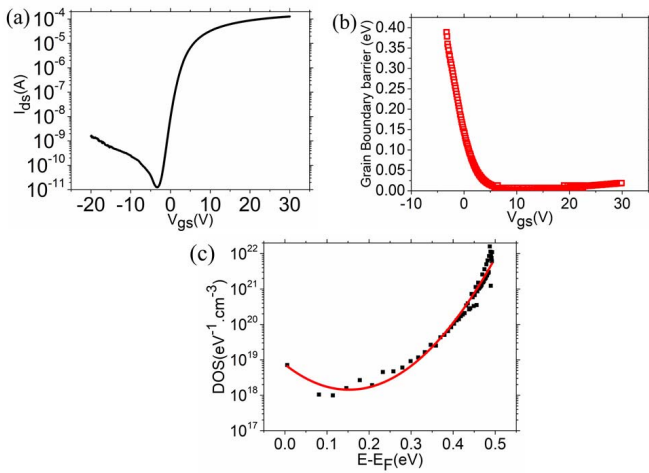


Fig. 5. (a) Transfer characteristics of the polycrystalline silicon lateral TFT, (b) grain boundary barrier height of the polycrystalline silicon lateral TFT, and (c) DOS for the polycrystalline silicon lateral TFT.

this value is about $3.61 \times 10^{16} \text{ cm}^{-2}$ for the device with 300-nm active layer. The concluded DOS can therefore be expressed as

$$\text{DOS}(\text{eV}^{-1} \cdot \text{cm}^{-3}) = 1.26 \times 10^{24} \exp(39.4(E - E_C)) \quad (15)$$

$$\text{DOS}(\text{eV}^{-1} \cdot \text{cm}^{-3}) = 1.05 \times 10^{24} \exp(29.1(E - E_C)). \quad (16)$$

For the device with 150- or 300-nm active layer, the $E - E_C$ value is from -0.352 eV to approximately -0.137 eV by considering the $E - E_F$ values ranging from 0.25 eV (corresponding to the threshold voltage) to 0.465 eV for the device with 150 nm active layer and the $E - E_C$ value is from -0.397 eV to approximately -0.199 eV by considering the $E - E_F$ values ranging from 0.204 eV (corresponding to the threshold voltage) to 0.402 eV for the device with 300-nm active layer. Obviously, the DOS for the device with 150-nm active layer is much smaller than the device with 300-nm active layer for the same $E - E_F$, and E is closer to the mobility edge for the device with 150-nm active layer, indicating better electrical characteristics for the device with 150-nm active layer.

In order to further verify the accuracy of this method, the polycrystalline silicon lateral TFT is also studied. For the lateral TFT, from Fig. 5(a), the flat-band voltage is -3.4 V , while the threshold voltage is 3.6 V . The gate oxide layer thickness is 100 nm , the channel width/length ratio is $40/20 \mu\text{m}$, and the drain-source voltage is 1 V . From Fig. 5(a) and (b), the intrinsic mobility is $128 \text{ cm}^2/\text{V} \cdot \text{s}$, and the deduced grain boundary barrier height at flat-band state is about 0.387 eV . Therefore, from (10), the trap density can be calculated to be

$$N_t \left[\exp\left(-\frac{E_c - E_F}{k_B T_0}\right) - \exp\left(-\frac{0.173}{k_B T_0}\right) \right] = -2.56 \times 10^{13}. \quad (17)$$

From the DOS calculation of Fig. 5(c), it can be deduced that

$$k_B T_0 = 0.0322 \quad (18)$$

$$\log_{10} N_t - 13.5(E_c - E_F) = 7.23. \quad (19)$$

By calculation, $N_t = 5.51 \times 10^{15} \text{ cm}^{-2}$, and $E_c - E_F$ equals 0.632 eV , which is close to the values of vertical TFT (0.601 or 0.602 eV). The nearly same $E_c - E_F$ further indicates the accuracy of this method, and the DOS of lateral TFT can be expressed as

$$\text{DOS}(\text{eV}^{-1} \cdot \text{cm}^{-3}) = 1.71 \times 10^{23} \exp(31.1(E - E_C)). \quad (20)$$

For lateral TFT, N_t is one order of magnitude lower than the values of vertical TFTs, indicating the larger field-effect mobility and better crystalline quality of lateral TFT. Nevertheless, the large channel width/length ratio of vertical TFTs also supports the high current. Note that, even with a high N_t , the polycrystalline silicon vertical TFTs show a current in the order of 10^{-5} A at a low V_{ds} of 10 mV , which is promising to drive diverse displays.

IV. CONCLUSION

Polycrystalline silicon vertical TFTs were fabricated with five-mask process and different active layer thicknesses of 150 and 300 nm . For the device with 150-nm active layer thickness, the higher ON/OFF current ratio of more than 10^6 is obtained, indicating better electrical characteristics with low DOS. The DOS is calculated, and by introducing the intrinsic mobility and the grain boundary barrier height at the flat-band state, the DOS expression can be detailedly elucidated through the threshold voltage calculation. Polycrystalline silicon lateral TFT was also introduced to further verify the accuracy of this evaluation method.

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