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Assessing the insulating properties of an ultrathin $SrTiO_3$ shell grown around GaAs nanowires with molecular beam epitaxy

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Abstract

We have studied electronic transport in undoped GaAs/$SrTiO_3$ core-shell nanowires standing on their Si substrate with two-tip scanning tunneling microscopy in ultrahigh vacuum. The resistance profile along the nanowires is proportional to the tip separation with resistances per unit length of a few GΩ/μm. Examination of the different transport pathways parallel to the nanowire growth axis reveals that the measured resistance is consistent with a conduction along the interfacial states at the GaAs{110} sidewalls or through the slightly-reduced $SrTiO_3$ shell, the 2 nm-thick $SrTiO_3$ shell being as much as resistive, despite oxygen deficient growth conditions. The origin of the shell resistivity is discussed in light of the nanowire analysis with transmission electron microscopy and Raman spectroscopy, providing good grounds for the use of $SrTiO_3$ shells as gate insulators.

Keywords: core-shell nanowire, functional oxides, heterointerface, transport properties, multiple-tip scanning tunneling microscopy

1. Introduction

In recent years, the potential of one-dimensional III-V semiconductor nanowires (NWs) grown by epitaxial methods has been demonstrated, with material quality comparable to their bulk counterpart, suitable for a large number of unique electronic [1,2] and photonic devices [3,4,5]. There is now a quest to improve the performances of these devices by combining such NWs with other materials, known for

reducing the impact of defects or providing additional functionalities. For example, covering InAs NWs with high-k dielectrics benefits to the overall performance of the field effect transistor with an increase of the electron mobility, a larger ratio between the on-state and off-state currents and a higher transconductance [6]. When III-V NWs are embedded in a ferroelectric polymer, a full depletion of the intrinsic carriers is achieved thanks to the high ferroelectric polarization field, resulting in photodetectors with enhanced performances [7,8]. Also, by transferring InP NWs that host a single InAsP quantum dot onto a piezoelectric crystal, the exciton emission of the quantum dot can be tuned based on the strain induced by the polarized crystal [9].

Among the existing functional materials, perovskite oxides are relevant as they exhibit fascinating magnetic, ferroelectric and multiferroic properties [10], and because their growth can be achieved with atomic-layer precision enabling the formation of abrupt oxide heterostructures [11,12,13]. As the quality of the interface is essential in the improvement of the device performances, such results entailed the study of heterointerfaces between oxide materials and III-V semiconductor materials. Theoretical works predicted the existence of a two-dimensional electron gas at different GaAs/oxide interfaces [14,15,16], which can be enhanced or quenched depending on the nature and the density of interfacial point defects [17]. Experimentally, molecular beam epitaxy (MBE) was used to create $SrTiO_3$/GaAs heterointerfaces or more complex heterostructures [18,19,20,21]. Although the growth parameters have been optimized to make the interface sharper, like the use of a Ti prelayer to minimize the oxidation of the GaAs(001) surface and to prevent cationic intermixing at the interface [22,23], the growth is still challenging. It has to face with significant structural differences between III-V compounds and perovskite oxides and the rapid oxidation of the crystal surface of III-V semiconductors, which leads to the formation of an amorphous interfacial layer [24]. Therefore, attempts to epitaxially grow a perovskite oxide as a shell around III-V semiconductor NWs are scarce [25] and the electronic properties of the interface are still unknown.

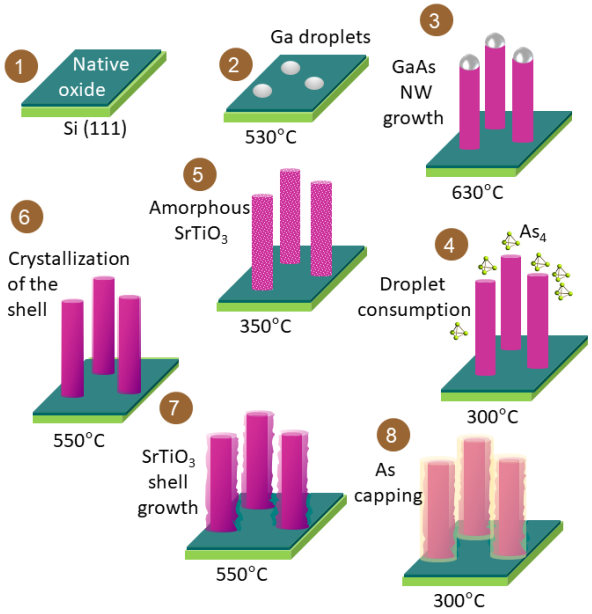

Figure 1. Schematics of the different stages for the growth of GaAs/$SrTiO_3$ core-shell nanowires.

In order to limit the unintentional oxidation of III-V surfaces, the growth conditions imply a low oxygen partial pressure during the epitaxy of the $SrTiO_3$ layer. Such conditions favor the formation of oxygen vacancies, which are known to give rise to a n-type electronic conductivity in thin $SrTiO_3$ epitaxial films [26,27]. In this work, we aim at verifying if the growth of $SrTiO_3$ shell around undoped GaAs NWs by MBE results in a similar conductivity, albeit the different growth geometry. To avoid any technological processes that could modify the NW properties during the formation of electrical contacts, electrical transport of NWs standing on their Si substrate is studied with two-tip scanning tunneling microscopy in ultrahigh vacuum (UHV). The transport measurements reveal the formation of a low contact resistance and a high NW resistance which is proportional to the NW length. While the core of the NWs is insulating, the magnitude of the measured resistance in the GΩ range is consistent with the one obtained in GaAs NWs with oxidized sidewalls. Such a result highlights a conduction along the interfacial states, which are induced by the chemical reactions occuring at the GaAs {110} sidewalls. It indicates that the $SrTiO_3$ shell is as much resistive as the interfacial pathway. To determine the origin of the shell resistance, high-resolution scanning transmission electron microscopy (STEM) and Raman spectroscopy have been performed. They show the formation of a polycrystalline shell with no detection of oxygen reduction. Such a resistive state of the shell provides an appealing path towards the development of epitaxial perovskite gate insulators around semicondutor NWs.

2. Methods

2.1. Nanowire growth

GaAs/$SrTiO_3$ NWs were grown on a *n*-doped Si(111) substrate by MBE, as described in Figure 1. Before being introduced in UHV, the epi-ready Si substrate was cleaned for 5 min in ethanol and acetone to remove surface contaminations. The substrate, covered by a 2 nm-thick native oxide layer, was outgassed in UHV for a few minutes at 200 °C and then heated up to 530 °C. At this temperature, one monolayer of Ga was deposited at a deposition rate of 1.4 Å/s to produce Ga droplets, which decompose the Si native oxide to allow the growth of self-catalyzed GaAs NWs. During the NW growth, the temperature of the sample was 630 °C and the Ga deposition rate was 2.1 Å/s in units of equivalent 2D GaAs growth rate as measured from RHEED oscillations during Ga-limited growth. The As_4 beam equivalent pressure was set at 3.3×10^{-6} Torr which

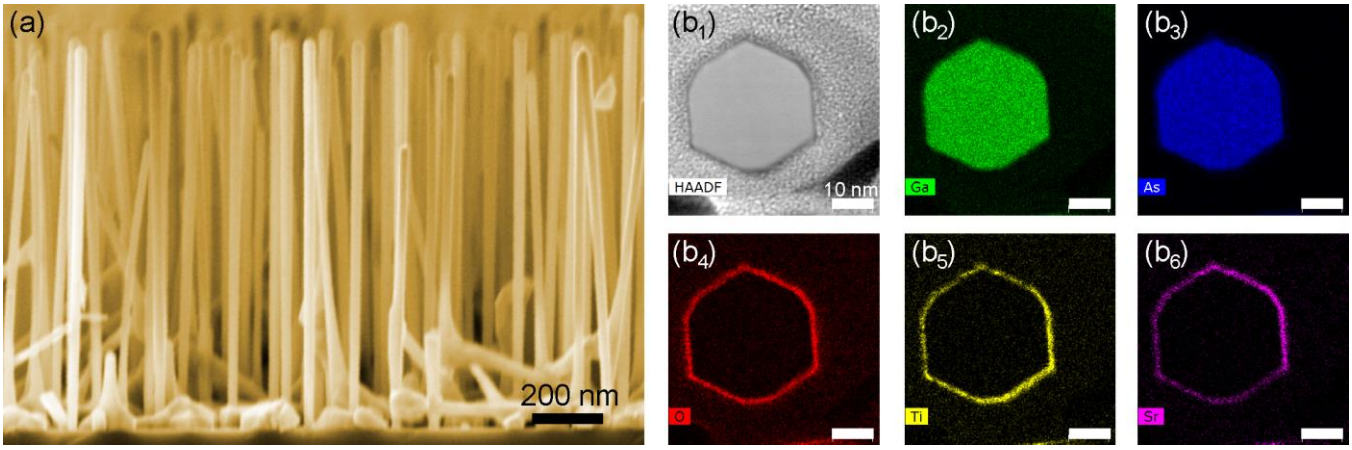

Figure 2. (a) Scanning electron microscopy image of GaAs/$SrTiO_3$ core-shell nanowires grown on a Si(111) substrate. (b) HAADF STEM image of a GaAs/$SrTiO_3$ core-shell nanowire and corresponding EDX elemental mappings for gallium, arsenic, oxygen, titanium and strontium respectively.

corresponds to a deposition rate of 3 Å/s as measured from RHEED oscillations during As-limited growth [28]. After 15 min, the Ga shutter was closed and the temperature was decreased down to room temperature under an As_4 flux in order to avoid GaAs decomposition. The sample was transferred, in UHV, to a second MBE reactor where an amorphous $SrTiO_3$ buffer layer was first grown at 350 °C under low O_2 partial pressure of 5×10^{-8} Torr. Annealing at 550 °C in UHV for 15 min led to the crystallization of the $SrTiO_3$ buffer layer, ensuring the formation of a relatively sharp interface [25]. The final step consisted in the growth of the rest of the $SrTiO_3$ shell at 550 °C under a O_2 partial pressure of 1×10^{-6} Torr. The intended thickness of the shell was limited to 2 nm, so that electrons injected from a metal contact can tunnel through this oxide layer to reach the GaAs core [29]. Finally, the GaAs/$SrTiO_3$ NWs were capped with a thin As amorphous layer to protect them from reaction with air during their transfer.

A scanning electron microscope (SEM) image of a typical sample is shown in figure 2(a). The NW average length and diameter were 1.2 μm and 60 nm respectively. In order to determine the shell thickness, the NWs were first transferred onto a silicon susbtrate, then buried under a layer of hydrogen silsesquioxane (HSQ) and thin slices, perpendicular to the NW main axis, were milled with the use of a focused ion beam machine. High angle annular darf field scanning electron microscopy (HAADF STEM) was performed concomitantly with energy dispersive X-ray (EDX) elemental mappings. Figure 2(b) clearly shows that the GaAs core is surrounded by a shell with a thickness about 2.0 nm.

2.2. Electrical characterization

The electrical resistance of the NWs was measured with a multiprobe scanning tunneling microscope (STM) working in UHV (Nanoprobe, Omicron Nanotechnology). As the use of good electrical contacts is essential to inject and extract charge carriers into the NWs, tungsten tips were prepared by an electrochemical etching in NaOH and thoroughly annealed in the UHV preparation chamber to remove the thin oxide layer covering the tips. Prior to the measurements, the As capping layer was also removed by annealing the samples at 320 °C in the preparation chamber and monitoring the As desorption with mass spectroscopy. The NWs were kept upright on the Si substrate and the STM tips were

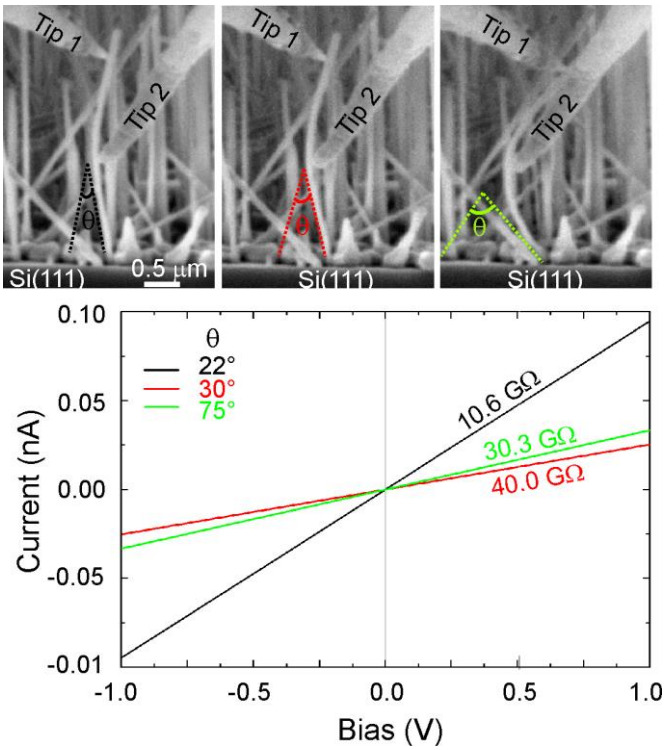

Figure 3. Sequence of SEM micrographs of two STM tips contacting a GaAs/$SrTiO_3$ core-shell nanowire with a constant tip separation of 1.6 µm and corresponding two point *I–V* measurements for three different curvatures of the nanowire.

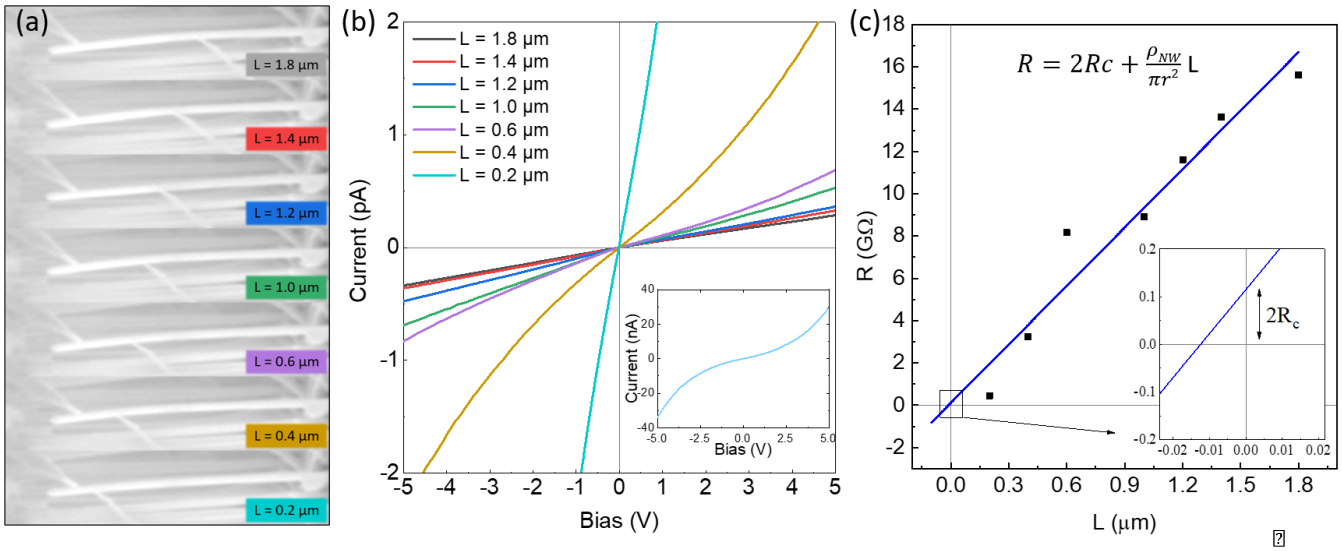

Figure 4. Sequence of SEM micrographs of two STM tips contacting a GaAs/$SrTiO_3$ core-shell nanowire with different separation. (b) Two point *I-V* measurements acquired at the different tip separations. Inset: Full range of current for the smallest tip separation of 0.2 m. (c) Resistance measured from the *I-V* characteristics as a function of the tip separation. The solid-blue line is the best-fitting curve based on the variation of the total resistance R with the contact resistance R_c the resistivity of the NW ρ_{NW}, its diameter *r* and length L. Inset: Magnified view close to zero bias to deduce the contact resistance R_c.

approached under the supervision of a SEM. The STM tips were brought into electrical contact with a NW using the distance regulation of the STM control system. A stable electric contact was achieved by further pushing down the NW in the feedback-off mode. However, great care must be taken to avoid any significant deformation of the NW, as a mechanical stress applied to a GaAs NW is known to affect its resistivity [30]. As shown in Figure 3, the same NW was electrically characterized with two STM tips, tip 2 applying increasing mechanical stress in the middle of the NW. Hence, the NW strongly bends. While the three *I–V* curves measured for three different tilts of the NW show a linear behavior, the deformation causes a substantial change of the characteristic slope. Therefore, once the first STM tip was connected to the NW, multiple *I–V* characteristics were performed with less and less pressure applied to the second connected STM tip to make sure that the NW segment between both STM tips was straight, enabling to reach a high

reproducibility in strain-free measurements of the conductance. Subsequently, the SEM and the light were turned off and the measurements of the NW resistance was performed with two STM tips and a floating substrate.

For comparison of the electrical resistance, bare GaAs NWs without the $SrTiO_3$ shell were also interconnected with conventional planar technology. The NWs were deposited on a degenerately doped Si wafer with 2000 nm of a thermally grown SiO_2 layer, where golden marks had been prepared prior the deposition with laser lithography. The marks were used to locate the NWs with a scanning electron microscope and select the appropriate ones for contact processing. After spin-coating the sample with an electron beam sensitive polymer, four 300 nm-thick Cr/Au contacts were defined along the NW using electron beam exposure. This step was followed by a thorough lift-off to get GaAs NWs with clean oxidized sidewalls.

3. Results

Figure 4 shows a sequence of *I–V* characteristics measured in a GaAs/$SrTiO_3$ NW for tip separations ranging between 0.2 and 1.8 μm, with negligible bending of the NW segment between both STM tips. The curves are fairly symmetric but deviate from a straight line at high bias, when the tip separation decreases (lower inset of figure 4(b)). While at high bias and small tip separation, the non-linear behavior reflects a space-charged-limited current [31,32], we focus on the intermediate bias range $|V| \leq 1V$, where all *I–V* are linear and can be fitted with a straight line. The slope of the line provides the total resistance, which involves the resistance of the NW and the contact resistances between the NW and the STM tips. Based on the SEM images of figure 4(a), the section of the NW is assumed to be constant along the growth axis within the range of the tip separations which were considered here. Hence, the resistance of the NW is expected to vary linearly with its length. This result is consistent with the data points shown in figure 4(c), where a best fit yields a resistance per unit length of 9 GΩ/μm. Extrapolation to zero electrode separation gives a contact resistance of ~60 MΩ, as seen in the inset of figure 4(c). This value is much smaller than the total resistance of the NW, concurring with the predominance of the NW resistance over the total resistance.

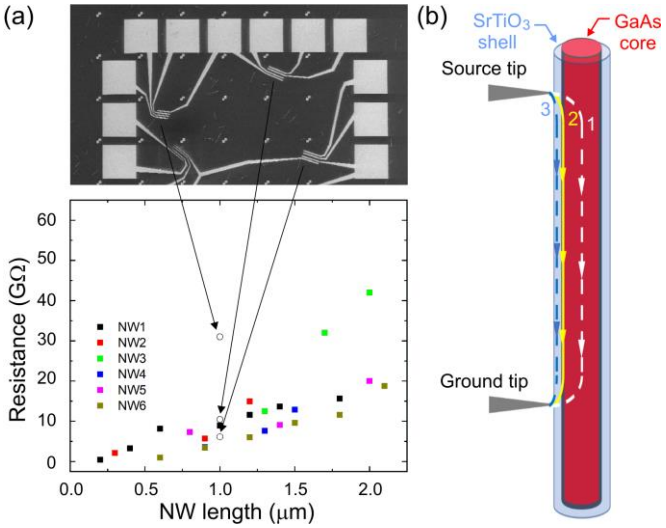

Figure 5. Variation of the resistance as a function of the tip separation for 6 different GaAs/$SrTiO_3$ core-shell nanowires. The resistances are compared with the 4-probe resistances of three GaAs nanowires with native oxide sidewalls for a separation between the potential probes of 1μm. These three GaAs nanowires shown in the upper inset were contacted with access-electrodes patterned using e-beam lithography. (b) Schematics of a GaAs/$SrTiO_3$ core-shell nanowire contacted with two tips which shows three conductance channels: (1) through the GaAs core, (2) at the GaAs/$SrTiO_3$ interface, (3) through the $SrTiO_3$ shell and along its surface.

Similar *I–V* characteristics were measured for 6 NWs. When the variation of the corresponding resistance is plotted as a function of the tip separations, as seen in Figure 5(a), a reproducible behavior is found: the total resistance increases linearly with the length of the NWs. The majority of the NWs show a high resistance per unit length of a few GΩ/μm, although one of them steps out from this range with a higher resistance per unit length. This resistance is very high in comparison with the resistance found in ultra-thin $SrTiO_3$ film grown on Si or GaAs [27,33]. Indeed, three different charge transport pathways have to be considered: 1) through the GaAs core, 2) at the GaAs/$SrTiO_3$ interface and 3) through the $SrTiO_3$ shell and along its surface. These channels being in parallel between the source tip and the ground tip (figure 5b), the NW resistance is obtained from the inverse of the algebraic sum of the reciprocal value of each of the resistance.

The GaAs core is nominally undoped, but residual impurities in the growth chamber can produce an unintentional doping [34,35]. Based on the Hall measurements of reference thin film samples, we estimate a residual hole concentration between $5x10^{15}$ and $1x10^{16}$ cm^{-3} in the core. Assuming a mobility about tens of $cm^2.V^{-1}.s^{-1}$ [36] or smaller, due to the presence of twin planes and stacking faults, as seen in the STEM image of figure 6a, resistances per unit length in the GΩ/ m range can be obtained, similar to the mesured resistances. However, the absence of photoluminescence in the GaAs/$SrTiO_3$ NWs

indicates the presence of numerous interfacial defects [25]. They are either caused by the oxidation of the GaAs sidewalls during the growth of the $SrTiO_3$ shell or the interdiffusion of metallic species into the GaAs core. These defects are likely to pin the Fermi level midgap, leading to the full depletion of the core [37,38]. Hence, the resistance of the core increases by a few order of magnitude and makes the core insulating [39].

The second channel consists of the GaAs/$SrTiO_3$ interface. While we are not aware of any theoretical study of the electronic properties of the GaAs (110) /$SrTiO_3$ interface, the existence of Ga-O bonds has been predicted to give rise to a type I heterostructure for the GaAs (100) /$SrTiO_3$ interface [**Erreur ! Signet non défini.**]. Such a band alignment prevents the formation of an accumulation layer at the interface in the $SrTiO_3$ shell. But the existence of interfacial states caused by the oxidation of the GaAs sidewalls could support a measured resistance per unit length of a few GΩ/µm [39,40]. To assess the electrical contribution of the interface to the transport, the resistance of GaAs NWs contacted with access electrodes patterned with e-beam lithography was measured. For such NWs, the sidewalls consist of a native oxide. As seen in figure 5(a), the resistances of both types of NWs are in the same range, corresponding to the resistances typically measured on semi-insulating GaAs wafers with oxidized surfaces [41,42]. Although the two-step growth process to grow the $SrTiO_3$ shell minimizes the formation of an amorphous oxide layer on the {110} sidewalls of the GaAs core, it does not prevent the oxidation of the Ga and As surface atoms, as found by X-ray photoelectron spectroscopy [25]. Hence, the oxidation of the GaAs sidewalls leads to the formation of interfacial states with a density high enough to account for the measured conduction. Moreover, Ti is known to react with GaAs to form an intermetallic compound Ga_xTi_y [43], which could also give rise to conducting interfacial states.

Therefore, the resistance of the shell is either of the same order of magnitude than the resistance of the GaAs/$SrTiO_3$ interface or even higher, in significant contrast with the n-type conductivity found in $SrTiO_3$ thin films [26,44]. For comparison, considering a conduction only through the $SrTiO_3$ shell with 10 GΩ/µm, the equivalent resistivity would be around 200 Ω cm with a large sheet resistance of 1 GΩ/sq, corresponding to a low carrier density of a few 10^{15} cm^{-3} with low 10^{-5} at.% of oxygen vacancies [45], which is reasonable with these growth conditions. As the resistance depends on the crystal quality of the material, the morphology of the shell was investigated with high-resolution STEM. Figure 6 shows two representative high-resolution STEM images of the GaAs/$SrTiO_3$ interface. The shell is unambigously identified based on its distinct crystal structure with respect to the GaAs core. In some regions (figure 6(a)), it appears to be continuous and shows the intended thickness of 2 nm, whereas in other regions (figure 6(b)), the shell consists of connected $SrTiO_3$ nanocrystallites with different orientations, consistent with previous observations [**Erreur ! Signet non défini.**].

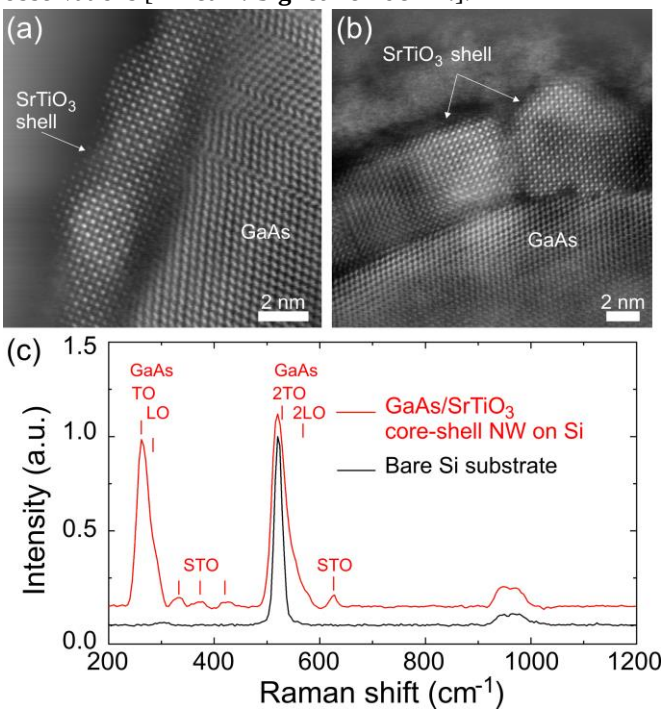

Figure 6. (a-b) Two examples of crystal structures observed with STEM for the $SrTiO_3$ shell. (c) Raman spectroscopy performed on cleaved GaAs/$SrTiO_3$ core-shell nanowires that were dispersed on a Si substrate. The vertical segments indicate phonon modes corresponding to the GaAs core and the $SrTiO_3$ shell. The transverse and longitudinal optical phonon modes in GaAs and their overtone are labelled TO and LO respectively.

This polycrystalline nature of the shell around the whole core of the NW is confirmed by the examination of cleaved NWs lying flat on a Si substrate with Raman spectroscopy. As shown in figure 6(c), while the most intense peaks correspond to the longitudinal (LO) and transverse optical (TO) phonon lines of the Si substrate (LO-TO at 520 cm^{-1}, 2TO at 960 cm^{-1}) [46] and the GaAs core (TO at 266 cm^{-1}, LO at 290 cm^{-1}, 2TO at 532 cm^{-1} and 2LO at 580 cm^{-1}) [47,48], small peaks are measured in between. We attribute them to phonon lines of the $SrTiO_3$ shell. Although bulk $SrTiO_3$ has no first-order Raman fingerprint due to its cubic perovskite structure, a wealth of second order peaks exist [49]. Moreover, with the small thickness of the shell and the existence of defects, the inversion symmetry of the crystal is broken and can lead to the occurrence of first-order phonon lines [50]. As several peaks are detected (332 cm^{-1}, 372 cm^{-1}, 424 cm^{-1}, 625 cm^{-1}) with wave numbers that are not found in single phase of $SrTiO_3$, we believe that the different phonon lines reflect the polycrystallinity of the shell in agreement with the Raman spectra obtained for nanocrystalline $SrTiO_3$ powders [51,52,53,54]. From the absence of peaks at 700 cm^{-}

[1] [55], we also confirm that the degree of oxygen reduction, which could occur due to the growth conditions, is small, making the shell barely doped with oxygen vacancies. Therefore, the grainy polycrystalline nature of the shell limits the electron mobility to values much lower than the single crystal mobility of ~10 $cm^2/V.s$ [56,57]. Such a low mobility (<0.1 $cm^2/V.s$) combined with electron concentration much smaller than 10^{18} cm^{-3} yields resistances for a 2 nm-thick shell which are higher than the measured resistances in the GΩ range.

While transport along the GaAs/$SrTiO_3$ interface and through the shell accounts for the resistance of the NWs, a conduction on the surface of the shell cannot be excluded. For single $SrTiO_3$ nanocubes with 6 square {100} facets and sizes ranging between 200 nm and a few micrometers, recent two-probe electrical measurements have shown that the nanocrystals were not conductive for bias below 15 V [58]. But, performing the same measurements on truncated nanocubes revealed a surface transport, the current depending on the orientations of the facets around the truncated nanocrystals. Similar currents as the ones measured in figure 4(b) were obtained, suggesting that the surface of the shell might be responsible for the measured resistance. In contrast to these single crystals, the shell of the NWs is highly granular, leading to a less efficient hopping conduction. Therefore, based on the grainy polycrystalline nature of the shell, we rule out a surface conduction efficient enough to account for the measured resistance.

4. Conclusion

Two-tip transport measurements of as-grown undoped GaAs/$SrTiO_3$ core-shell NWs yield resistances per unit length of a few GΩ/μm. These values are consistent with an electrical transport along the heterointerface or through the slightly reduced $SrTiO_3$ shell although of high resistance. In the case of a conduction along the heterointerface, we attribute its physical origin to the presence of a high density of interfacial states which are caused by the oxidation of the GaAs{110} sidewalls and, to a lesser extent, by the formation of intermetallic TiGa compounds. The electrical resistance of the shell has a magnitude similar or higher than the resistance provided by the GaAs/$SrTiO_3$ interface. This result is in contrast to previous studies on reduced thin $SrTiO_3$ films, which are highly conducting due to a significant accumulation of electrons. As the electron concentration depends on the excess of oxygen vacancies, we believe that the polycrystalline nature of the shell and the proximity of the GaAs interface strongly limits the formation of oxygen vacancies in the shell. Such an effect gives rise to a highly resistive shell, which, if better controlled, could be of interest when used as a gate insulator in III-V field effect transistors or to further grow functional oxide layers.

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