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Antoine Bulteau[1], Yves Lembeye[1], David Frey[1]

[1] Univ. Grenoble Alpes, CNRS, Grenoble INP[*], G2Elab, France

Corresponding author: Antoine Bulteau, antoine.bulteau@g2elab.grenoble-inp.fr

Abstract

This paper presents the development of a model for the design of a 4 legs inverter taking into account different limiting parameters. The context of this application is a converter which enables the link between a Quad Active Bridge (QAB) [1][2] and the grid, allowing an unbalanced active and reactive power injection realizing an energy router (ER) function [3][4]. In this case, the inverter is confronted by several constraints. The design of the DC capacitance and the limitation of the neutral current are taken into account in function of possibilities and constraints imposed by the QAB and the grid. This methodology can be applied to other 4 legs inverter structures.

1 Introduction

Currently, a converter network architecture is proposed based on a multiport converter (MC). This MC is composed of two converters showed in **Fig 1**, the Quad Active Bridge, connecting the DC components and the 4 legs 2 levels inverter, allowing the interconnection to the AC grid making it possible to exchange energy between these equipments.

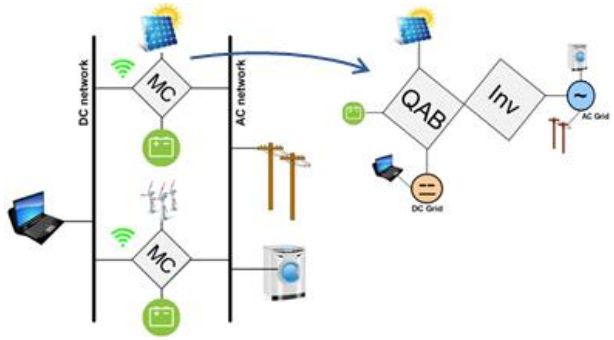

Fig 1 : Application of a multiport converter, splited in two converters; the QAB and the inverter, for energy routing in micro-grid application

In this article, the focus will be done on the 4 legs inverter part which is represented in **Fig *2***. First, we will discuss the constraints and limitations of connecting this converter to a grid and exchange power in an unbalanced way. Next, we will propose an adapted control and a more efficient design for this converter.

The study case we propose to address here is a three-phase network with single-phase domestic loads. This network is therefore potentially unbalanced as shown in **Fig *2***. In this application, the aim of the inverter is to furnish ancillary services to the network by acting as an energy router. Therefore, it helps to increase the load balancing by transferring power from one phase to another one. As we will see, this functioning will add new constraints in the inverter design.

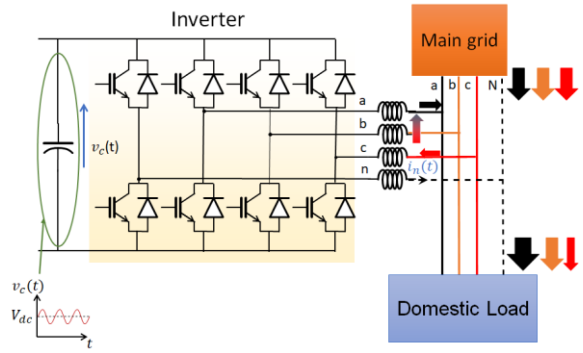

Fig 2: Inverter architecture, 4 legs, 2levels for micro-grid application, apparition of fluctuating voltage on DC bus capacitive and neutral current which is different from 0

This configuration brings constraints that will be explained in section 2. Section 3 will validate these constraints by simulation. Section 4 will present a validation of the simulation by experimentation. Finally, we will conclude in section 5.

2 Inverter Design

2.1 Neutral current limitation

[*] Institute of Engineering Univ. Grenoble Alpes

The design hypothesis is that the neutral current limit is the same as the one of the phases. The neutral current can be expressed by one equation with 6 unknowns (3 active P_i and reactive Q_i powers). This equation (1) is used in an algorithm to determine the cases that can fulfill the requirements for the inverter.

$$I_n = -\sum_{i=1}^{i=3} \frac{\sqrt{P_i^2 + Q_i^2}}{\widehat{V}_i} \sin(\omega_g t - \varphi_i) \qquad (1)$$

Therefore, this algorithm allows to determine the different possible cases and to evaluate the worst configuration. Thanks to the limitation in neutral current value ($I_{nmax} = I_{nom}$), it is possible to reduce the number of cases to design the capacitor. The **Fig 3** shows the percentage of configurations which respect a current neutral value under its nominal value.

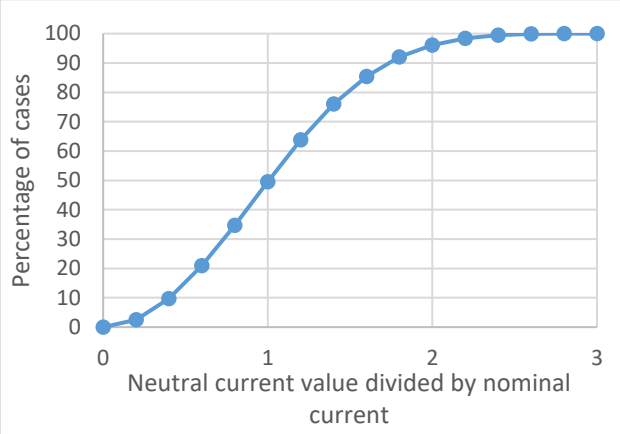

Fig 3: The percentage of cases below the value of the neutral current divided by the rated current

To obtain these values, it was chosen to vary the active and reactive power independently for each phase with a linear increment from $-P_{max}$ to $+P_{max}$ and identically for the reactive power per phase from $-Q_{max}$ to $+Q_{max}$. For each calculation, a value of the neutral current is obtained

Only 49% of the cases have its neutral current acceptable considering this nominal current limitation. If the criterion is to accept all configurations, then the neutral part needs an oversizing and specific protection to accept these cases. This possibility is not in line with this converter which induces an extra cost. Attended those multiple converters have to be implemented simultaneously, this solution should not be economically sustainable.

This constraint can be deflected in using centralized control [5] which enables to cover any power request by using several converters.

Furthermore, this neutral current constraint is not linked to the fluctuated power constraint which will allow to design the capacitive DC bus. Indeed, the two Fresnel Diagram shown in **Fig 4** indicate the current and power of each phase. The current has a counterclockwise, whereas the fluctuated power is in opposite rotation. In addition, both systems are not the same frequency (50Hz for the current frame, 100Hz for the fluctuating power). Therefore, it indicates that there is no direct link between the amount of neutral current and the fluctuating power in the DC bus.

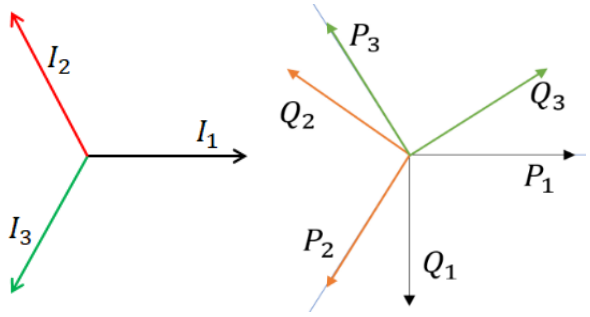

Fig 4: Fresnel Diagram for current and fluctuated power

On the **Fig 4**, the active power can be projected on direct and quadrature components, which allows to determine the magnitude and phase of fluctuated power that can be expressed with the following equation:

$$p_f(t) = P_f \cos(2\omega_g t - \phi_i) \qquad (2)$$

Table - 1 gives the result obtained for one configuration having 3680VA per phase corresponding to a current per phase of 16A.

Table - 1: Example of one configuration which enables to have a maximum fluctuating power value and a low value of neutral current

Variable	Value
P_1	3200W
Q_1	-1600VAR
P_2	-400W
Q_2	3600VAR
P_3	-3200W
Q_3	-1600VAR
P_f	**10,8kW**
I_n	**2,29A**

In this specific case, the maximum P_f can be equal to 3 times the apparent power for 1 phase. In the worst case P_f maximum value can reach 11kW, which is near to the value obtained in

Table - 1. For the neutral current, in that case, even if the fluctuating power is high, its value remains low. This current can reach 3 times the nominal current (48A) in the worst case for the neutral current.

This configuration shows the independence between the value of the fluctuating power and that of the neutral current

2.2 Classical design capacitor

The classical method to design the DC bus

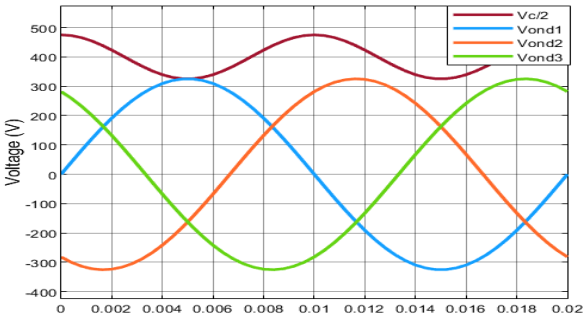

Fig 5: Voltage wave form from DC side and AC side. Case saturation limit when $min\ (V_c(t)/2) = max\ (V_{ond1}(t))$

capacitor is first to determine the maximum voltage fluctuation which enables the system to function properly. Then by using equation (3) the value of the capacitance can be determined:

$$C_{dc} = \frac{\max\left(p_f\left(t-\frac{T_g}{8}\right)\right)}{2\omega_g V_{dc} \max(v_{ac}(t))} \quad (3)$$

With $p_f(t)$ the fluctuating power at a frequency of $2\omega_g$, V_{dc} the DC bus voltage and v_{ac}(t) the allowed fluctuating voltage.

2.3 Minimal design capacitor

In the literature, there are many ways to design the bus capacitor depending on the hypothesis [6]. In this part, the only constraint used to minimize the capacitance value, is the inverter saturation corresponding to minimal voltage needed at its DC input.

Fig 5 shows the limit voltage shape wave base on this hypothesis It shows the worst configuration possible.

Taking into account the fluctuating power, it induces a fluctuating voltage on the DC bus. The expression of the capacitive bus voltage is represented in equation (4):

$$v_c(t) = V_{dc} + \frac{p_f\left(t-\frac{T_g}{8}\right)}{2C_{dc}V_{dc}\omega_g} \quad (4)$$

By definition, the modulation depth can be expressed as the ratio of the amplitude of the DC input to the peak-to-peak amplitude of the AC output of the inverter. Thus, per phase, the modulation depth is:

$$\alpha_x(t) = \frac{2v_{ond,x}(t)}{v_c(t)} \quad (5)$$

To simplify the equation and the resolution, the $v_{ond,x}(t)$ magnitude is expressed by $\widehat{V_{ond,x}}$ in the following equations and the variable $v_c(t)$ is replaced by its expression (3):

$$\alpha_x(t) = \frac{2\widehat{V_{ond,x}}}{\left(V_{dc} + \frac{p_f\left(t-\frac{T_g}{8}\right)}{2C_{dc}V_{dc}\omega_g}\right)} \quad (6)$$

Using this equation, the minimum capacitance value can be determined having in mind that the modulation depth must be kept under 1 (7) to avoid the saturation. The expression of the minimum capacitance value is given by equation (8).

$$1 \geq \max(\alpha_x(t)) \quad (7)$$

$$C_{dc} \geq \frac{\max(p_{finv}(t))}{2\omega_g V_{dc}} \cdot \frac{1}{V_{dc} - 2\widehat{V_{ond,x}}} \quad (8)$$

This equation could be more precise by taking account the phase shift between the fluctuation voltage and the AC voltage, but the improvement would be negligible. Furthermore, the determination of the capacity value does not need to be so precise due to the accuracy of these components.

In this application, we will consider an inverter with a DC bus voltage of 800V and a maximum fluctuating power of 10.8kW. In this case, to choose a constraint on the voltage fluctuation, the peak-to-peak voltage amplitude on the AC side is known, which is about 650V. Therefore, one can choose to use a minimum DC bus voltage that allows to be above this value. For example, the fluctuating DC bus value should not be below 680V, which allows a fluctuating voltage of 120V amplitude. The result of the dimensioning of this configuration is represented on **Fig 6** by the purple dot.

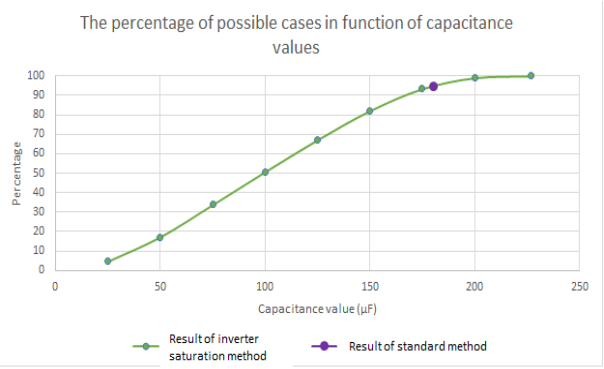

Fig 6: Comparison between standard method and specific method to design the capacitance for several value of DC voltages, in function of percentage of possible cases from energy router configuration.

This capacity value cannot cover all the cases given by the green curve. It only covers 95% of the cases. This means that 5% of the non-covered cases can lead to saturation of the inverter.

This method shows that the minimum capacitance value cannot be deduced simply by imposing a voltage fluctuation, but needs to take also into account the minimum voltage linked to the operating points and unbalanced power exchanged.

2.4 Average model

It is desired to control the inverter so that it can be used in unbalanced three-phase power configurations without error. For this purpose, a corrector must be implemented to avoid any static error. Before dimensioning the corrector, it is necessary to know the transfer function of the system under study. For this purpose, an average model is used and demonstrated. The average model used is presented in **Fig. 7.**

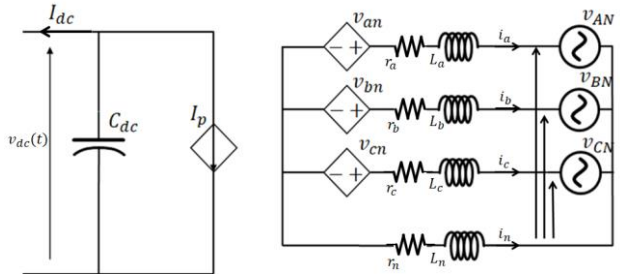

Fig 7: Average model from 4 legs and 2 level inverter

Afterwards, the equations from average model are synthetized in state space model represented in equation (9):

$$\dot{x} = Ax + Bu \qquad y = Cx \tag{9}$$

With the matrix values :

$$A = \begin{bmatrix} -A_L^{-1}A_r & A_L^{-1}\,dx^t \\ -\dfrac{\alpha_x}{C_{dc}} & 0 \end{bmatrix} \tag{10}$$

$$B = \begin{bmatrix} A_L^{-1} & 0_{31} \\ 0_{13} & -\dfrac{1}{C_{dc}} \end{bmatrix} \tag{11}$$

$$C = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \tag{12}$$

Besides, the inductance and resistance matrix have for expression:

$$A_L = \begin{bmatrix} L_n + L_a & L_n & L_n \\ L_n & L_n + L_b & L_n \\ L_n & L_n & L_n + L_c \end{bmatrix} \tag{13}$$

$$A_r = \begin{bmatrix} r_n + r_a & r_n & r_n \\ r_n & r_n + r_b & r_n \\ r_n & r_n & r_n + r_c \end{bmatrix} \tag{14}$$

The expression of modulation depth per phase is:

$$\alpha_x = [\alpha_a \quad \alpha_b \quad \alpha_c] \tag{15}$$

The transfer function of this multi-input multi-output (MIMO) system is:

$$Tf(s) = C(sI_4 - A)^{-1}B \tag{16}$$

$$Tf(s) = \begin{bmatrix} \dfrac{i_a}{V_{AN}} & \dfrac{i_a}{V_{BN}} & \dfrac{i_a}{V_{CN}} & \dfrac{i_a}{I_{DC}} \\ \dfrac{i_b}{V_{AN}} & \dfrac{i_b}{V_{BN}} & \dfrac{i_b}{V_{CN}} & \dfrac{i_b}{I_{DC}} \\ \dfrac{i_c}{V_{AN}} & \dfrac{i_c}{V_{BN}} & \dfrac{i_c}{V_{CN}} & \dfrac{i_c}{I_{DC}} \end{bmatrix} \tag{17}$$

For the application, only i_a/V_{AN}, i_b/V_{BN} and i_c/V_{CN} are used.

To reduce the error, feedback is used. In the case of an unbalanced three phase control, in the Park domain, it is necessary to use proportional integrator and resonant (PI-R) corrector [7]. Therefore, the controller computation is not simplified versus a standard time domain.

To simplify the design, a PR corrector[8] [9], [10] is directly used with the following transfer function:

$$PR(s) = K_p + \frac{2K_r\omega_c}{s^2 + 2\omega_c + \omega_{50}^2} \tag{18}$$

The value used for this transfer function is summarized in the **Table - 2**:

Table - 2: Coefficient values for PR corrector

	VALUE
K_r	20
K_p	0.1
ω_{50}	$314{,}5\ rad/s$
ω_c	$10 rad/s$

This enables to have the transfer function represented in **Fig 8**. Both transfer function are represented, without and with PR(s) corrector.

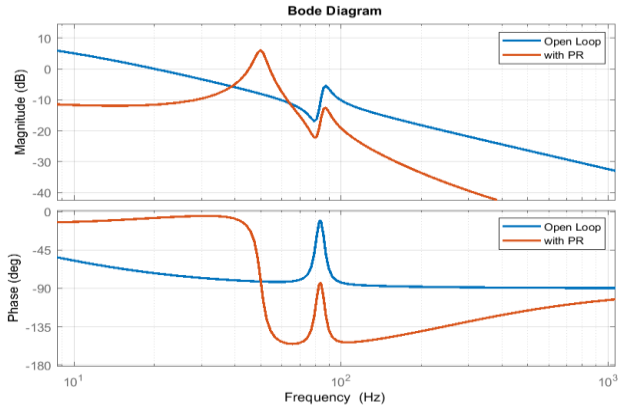

Fig 8: Transfer function of inverter with and without PR corrector

3 Simulation

The implementation of the controller and its effectiveness has first been tested on Matlab/Simulink with a commutated model to represent the converter.

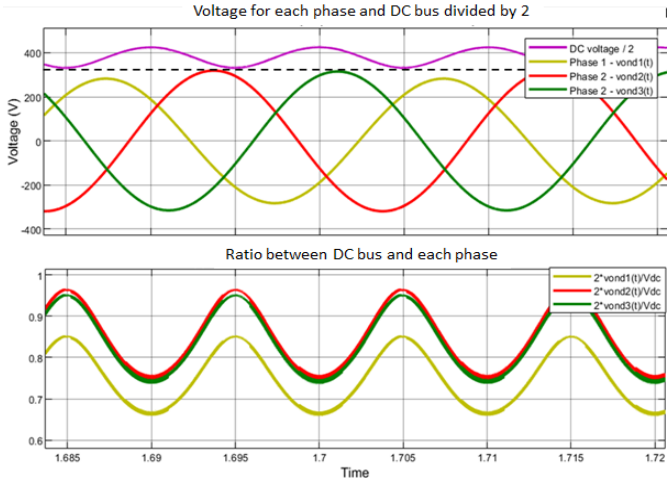

Fig 9: Application of capacitor design with minimum capacity design for the unbalanced three phase case presented in **table - 3**

The DC capacitor takes have the value of $340\mu F$. The **Fig** shows the result for depth modulation. This modulation doesn't fluctuate above 1, which is the limit of saturation.

Furthermore, the error in power of PR control is below 1%. It shows that this control remains very precise, add confirms its use.

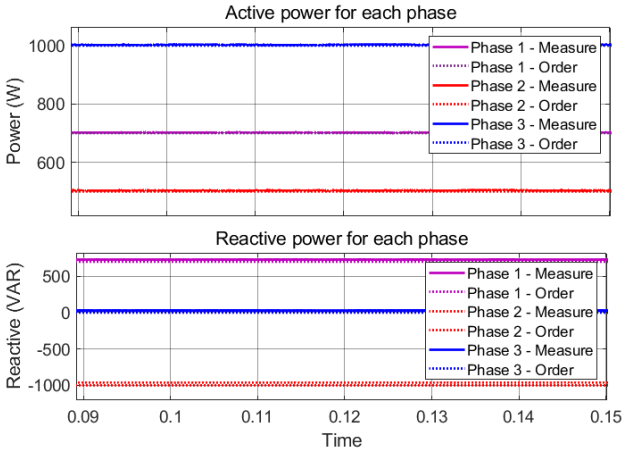

Fig 10: PR regulation on Active and Reactive Power for each phase

The **Table – 3** shows the difference between order and measure.

Table - 3: Values from **fig 9**, to compare and calculate the static error

	ORDER	MEASURE	ERROR
PHASE 1	700W	702W	0.3%
	700VAR	701VAR	0.15%
PHASE 2	500W	500.5W	0.1%
	-1000VAR	-999VAR	0.1%
PHASE 3	1000W	1003W	0.3%
	0VAR	0.1VAR	

It is desired to control the inverter so that it can be used in unbalanced three-phase configurations without error. For this purpose, it is seen in the literature that a PR corrector can compensate for these errors. In addition, in order to dimension this PR corrector, it is first necessary to know the transfer function of the system under study. For this, a modelling of the mean model is used and demonstrated. The average model used is shown in **Fig 7.**

4 Experimentation

4.1 Bench test

The test rig used is based on a two-level 4-leg inverter connected to a DC bus. The initial capacitor of the DC bus was disconnected in order to adapt the capacitance value to match the study value. These capacitances are represented by the 340µF bus in **Fig 11**.

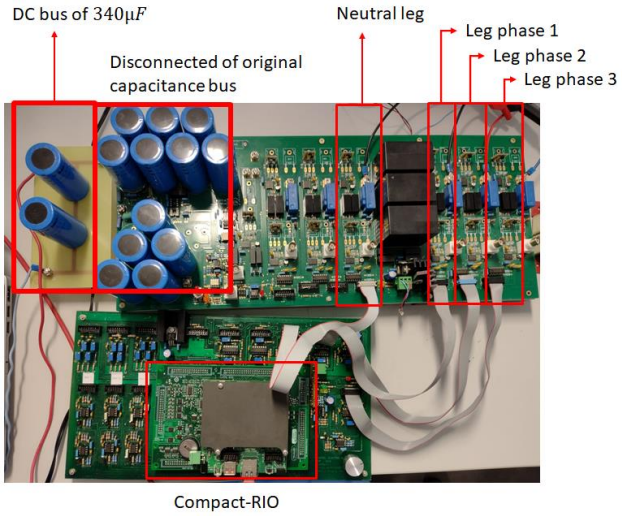

Fig 11: Bench test of four legs, two levels inverter controlled by a compact-Rio

In order to measure accurately the impact of the fluctuating power induced by the unbalance operation on the DC voltage bus and avoid any interaction with the power supply, an additional inductance (L_{DC} see Figure 12) has been added between the power supply and the DC bus. Its value is given in **Table - 4**. The inductance has been designed in order to present an impedance almost 100 times higher than the capacitive DC bus at the 100Hz frequency. Thus, allowing to ensure that the fluctuating power is effectively passing through the capacitance and therefore have accurate results.

Table - 4: Capacitance and inductance value for LC filter

L_{dc}	720mH
C_{dc}	0.340µF

On the AC connection, an inductive filter with a value of 5mH is added to cancel current harmonic on each of the four legs. Finally, the test bench corresponds to the one presented on **Fig 12.**

In order to maximize the ratio of the fluctuating voltage versus the DC one, the latter has been

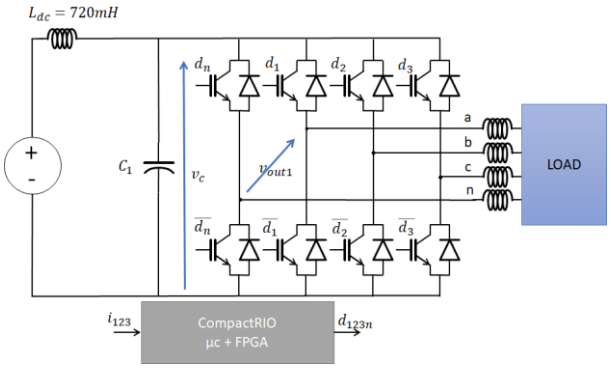

Fig 12: Electrical circuit of Bench test

adjusted in order to have a depth modulation close to 1. The V_{dc} value is predetermined from simulation and applied on the bench test. The approach remains the same.

4.2 Exploitation of the results

Several operation points have been tested. The **Table – 5** shows the results obtained theoretically and experimentally.

Table - 5: Test results from bench test with different unbalanced configuration

	Test 1	Test 2	Test 3	Test 4
P1	990W	1080W	80W	480W
Q1	0	0	640VAR	380VAR
P2	0	80W	1080W	500W
Q2	0	640VAR	0	-400VAR
P3	0	20W	20W	10W
Q3	0	-700VAR	-700VAR	-380VAR
V_{dc}	685V	685V	685V	685V
	Theorical result			
P_f	990W	2.19kW	150W	403W
ΔV_{ac}	14.8V	32.8V	2.3	6V
	Experimental result			
P_f	983W	2,04kW	110W	450W
ΔV_{ac}	15V	30,6V	1.59V	6.68V
	Absolut error			
P_f	0.7%	6,8%	26%	11%
ΔV_{ac}	1.3%	6,8%	30%	11%

The **Table – 5** shows the theorical model accuracy for extreme operating point. The operating points with a low fluctuated power have a lower accuracy than the other points. In addition, for the same active power transferred the fluctuated power can be above or below the test 1 which should be one the most unbalanced case for the inverter.

Test 1 corresponds to the single-phase mode for a three-phase inverter, which should correspond to one of the most unbalanced cases. Finally, configuration 2 with the same active power shows that the fluctuating power is much higher. Thus, this configuration is more unbalanced than the single-phase case. Test 3 shows that by having the same powers as case 2 but reversing 2 phases. The fluctuating power becomes almost non-existent.

Finally, case 4 shows a case providing the same active power as the other tests, with a distribution of this power between two phases, with the addition of reactive power exchange. It is obtained a fluctuating power 2 times lower than in the single-phase case.

5 Conclusion

The proposal of this dimensioning of the capacity on the DC voltage bus, allows to predict, according to the use of the inverter, the minimum capacity to be used to avoid the saturation of the inverter.

The simulated and experimental study validated this approach. However, the inaccuracy error is due to the use of a simple model. This simplification does not take into account certain phenomena such as the voltage drops induced by the conduction of the transistors.

This reduction in capacitance makes it possible to reduce the size of the components, their cost, and even to change the capacitor technology. The only condition to allow such a fluctuation on the DC bus is that the equipment connected to this bus is able to operate with this disturbance, using a control law adaptation and/or an active filter.

The capacitance value chosen, at the end of the sizing study, must take into account many more constraints, such as EMC, filtering or the voltage withstand of components such as transistors. By superimposing all these constraints, the most important value of the capacitance must be kept.

It has been seen that the energy router operation of an inverter cannot take all configurations because of the limit on the neutral current. Knowing that the application of energy routing is in the context of an inverter grid, it is possible to use a higher level control on the principle of hierarchical control [5] .The purpose of this control would be to allocate viable configurations to the different inverters while responding to grid services. This control ensures that the neutral current does not exceed its nominal value.

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