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Book of Abstracts, 1st International Workshop on Plasma Cryogenic Etching Processes (PlaCEP)

Sylvain Iséni, Rémi Dussart

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1ST INTERNATIONAL WORKSHOP ON PLASMA CRYOGENIC ETCHING PROCESSES



PlACEP 2022

May 16-19, 2022 - Orléans, France

First International Workshop dedicated to Plasma Cryogenic Etching Processes

Book of Abstracts

placep.sciencesconf.org



**May 16-19, 2022
Orléans, France**

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1 Foreword

The first International Workshop on Plasma Cryogenic Etching Processes (PlaCEP) will take place at Hotel Dupanloup in Orléans, FRANCE from **16th to 19th of May 2022**.

The conference will be organized in *hybrid mode*. PlaCEP will take place at the following address:
Hôtel Dupanloup, rue Dupanloup, 45000 Orléans FRANCE.
(Plus Codes for Google Maps: [WW26+XR Orléans](#))

Scope of the conference:

The workshop PlaCEP is a gathering of enthusiastic scientists and engineers in the field of cryogenic etching of semiconductor-based materials using e.g. SF₆, HBr or Cl₂-plasma chemistry at temperatures below –10 °C. It includes the modeling, simulation and/or experimental (atomic layer) etching of conventional materials like silicon, germanium, gallium arsenide, indium phosphide and emerging materials (2D materials like graphene or MoS₂), but also its oxide and nitride ceramic compounds. Furthermore, research activities on e.g. porous low-k materials (such as organosilicate glasses) – where cryogenic adsorption and subsequent etching is beneficial or the study of reactive gases (and physisorbed self-assembled monolayers SAMs) that only adsorb on the to-be-etched materials at low temperatures – are encouraged to join. Finally, studies on low-damage and high-selective plasma process, the formation of cryogenic dust plasmas or black silicon surfaces that benefit from cryogenic conditions are highly welcomed.

A large part of the workshop will be dedicated to discussions about last requirements on nanofabrication issues that cryogenic processes could address.



2 Conference Committees and Program

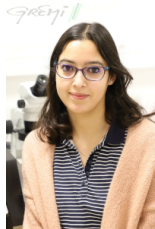
Local Committee

Research Group in the Energetics of Ionized Media (GREMI), UMR 7344 CNRS / University of Orléans, FRANCE.

Prof. Rémi DUSSART – Chair



Ms. Rim ETTOURI



Dr. Sylvain ISÉNI



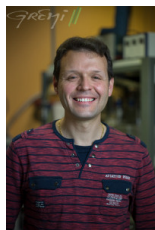
Ms. Elane KOUADOU



Mr. Jack NOS



Dr. Thomas TILLOCHER



Ms. Corinne DELHAYE



Ms. Lamiae HAMRAOUI



Ms. Sylvie JAUFFRION



Mr. Philippe LEFAUCHEUX



Dr. Arnaud STOLZ



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- Dr. Christophe CARDINAUD, *IMN*, Nantes, FRANCE
- Dr. Mike COOKE, *Oxford Instruments*, Bristol, Yatton, UNITED-KINGDOM
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- Dr. Henri JANSEN, *Technical University of Denmark*
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- Dr. Stefan TINCK, *University of Antwerpen*, BELGIUM

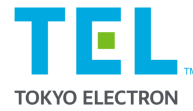


Orleans	Tokyo	New-York	San Francisco	Monday, May 16th	Tuesday, May 17th	Wednesday, May 18th	Thursday, May 19th
09:00	16:00	03:00	00:00	Organization	InvTalk4 : Rémi DUSSART GREMI 9:00-9:40	*InvTalk9 : Noritaka SAKAKIBARA University of Tokyo 9:00-9:40	InvTalk14 : Andrei AVRAM IMT Bucharest 9:00-9:40
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				Welcome talk - R. DUSSART 14h15-14h30			
				InvTalk1 : Thomas TILLOCHER GREMI 14:30 - 15:10	InvTalk6 : Aurélie GIRARD IMN 14:30 - 15:10	InvTalk12 : Jean-Francois DE MARNEFFE IMEC 14:30-15:10	
				InvTalk2 : Ahmed RHALLABI IMN 15:10-15:50	*InvTalk7 : Jose Maria DE TERESA Instituto de Nanociencia y Materiales de Aragón 15:10-15:50	InvTalk13 : Maria GAUDIG Martin Luther University Halle-Wittenberg 15:10-15:50	
				Coffee break	Coffee break	Coffee break	Visit of Chambord
				Talk 1 : Francesco VILLASMUNTA Technische Hochschule Wildau 16:20 - 16:45	*InvTalk8 : Mingmei WANG Tokyo Electron America 16:20-17:00	*Talk6 : Andam Deatema REFINO TU Braunschweig 16:20-16:45	
				*Talk 2 : Abid S. ALI SENTECH 16:45-17:10	*Talk5 : Rimantas KNIZIKVICIUS Kaunas University of Technology 17:00-17:25	Talk 7 : Uldis ŽAIMIS Liepaja University 16:45-17:10	
				*InvTalk3 : Alvaro GARCIA DE GORORDO Applied Materials 17:10-17:45	Industrial session	Industrial session	
					Guided visit of Orleans		
				Wine and Cheese			
						Diner at Bateau Lavoir - 19:30 - 22:00	

(*) Online talk

3 Sponsors

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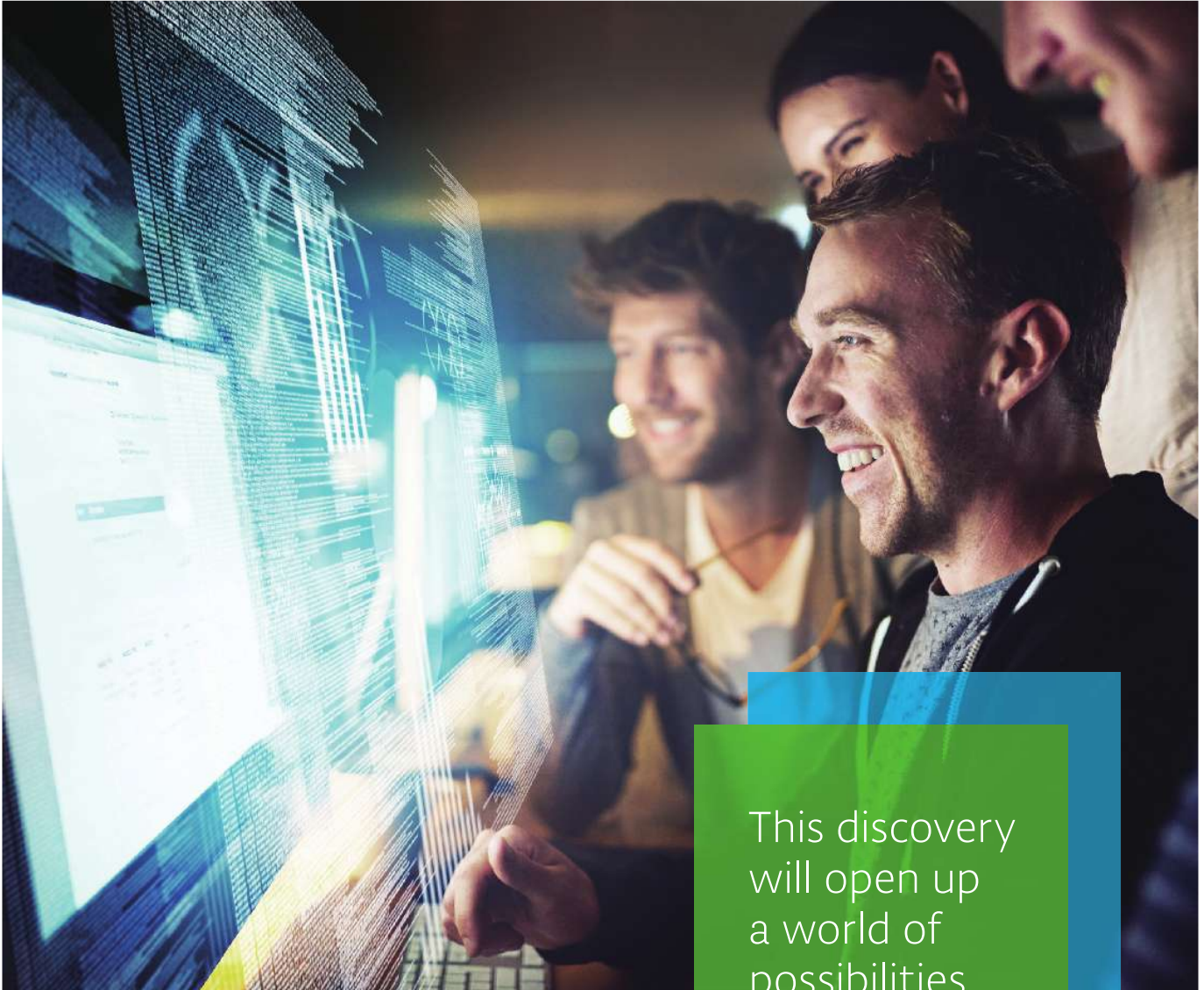


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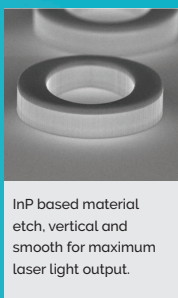
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- Atomic Layer Etch & Deposition
- Ion Beam Etch & Deposition
- Deep Silicon Etch
- Nanoscale Growth



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- Brazing Materials
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customized
- Carriers, FOUPs, Boxes
incl. customized parts
- Carbon based parts
- OEM and customized
Ceramic Substrates &
Packaging

Equipments and Service

- Wet area Equipments
- Dry Strip & Etch
Equipments
- Thermal treatments
Equipments
- Chemicals & Gas
delivery systems
- Particle Monitor and
control systems
- Fire Suppression
System
- Robot and Assembly
Repair
- Refurbished
Equipments

HF Vapor phase etching



Gas abatement systems



Dry Etching (RIE/ICP/ALE)-deposition (ALD/PECVD/ICPCVD)- IBE/IBD

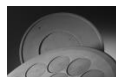


Particle measurement tool



RTP/RTA/RTO

Horizontal and Vertical diffusion Atmos/LPCVD



Materials: Quartz - SiC - Graphite

PVD and Evaporation Materials

Dopants TEOS -TEB-TEPO-SiCl4





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+1,8M
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- Un gaz conformes à vos spécifications
- Une prise en charge de l'installation par Air Liquide
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SENTECH

SI 500 C

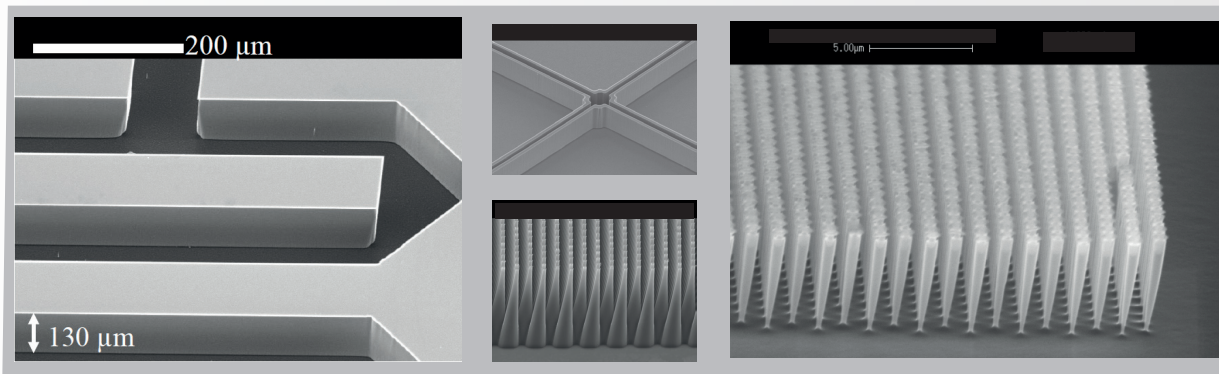
Cryogenic plasma etching



The **SI 500 C** enables the application of a wide-range of plasma etching processes from normal RIE to high-density processes, especially at extremely low temperatures down to -150°C . Many low-temperature etch processes allow the etching of highly anisotropic profiles by self-passivation, not only in silicon but also in other materials. In silicon cryogenic etching it produces smooth sidewalls. It allows nano-structuring and low damage etching.

BENEFITS AND APPLICATIONS

- Smooth sidewalls
- Tuning of angle and shape of the etch profile
- Low damage processing using PTSA, ICP plasma source
- Fluidics, sensors, optics, photonics



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SENTECH SI 500 C CRYOGENIC PLASMA ETCHER

The inductively coupled cryogenic plasma etcher SI 500 C is designed for cryogenic etching of silicon for smooth sidewalls, silicon etching at room temperature (optional) and deep silicon etching using the Bosch process (optional).

BENEFITS OF THE SI 500 C

- Cryogenic ICP plasma etching system for silicon and new materials
- PTSA ICP plasma source with low and narrow ion energy distribution for low damage processing
- Substrate temperature from -150°C to 80°C (LN2 cooling)
- Substrate temperature -10°C to 150°C for Bosch process with circulation chiller (optional)
- Automatic switching unit for comfortable change between cryogenic etching and RIE-process
- With vacuum load lock or cassette station plus transfer chamber



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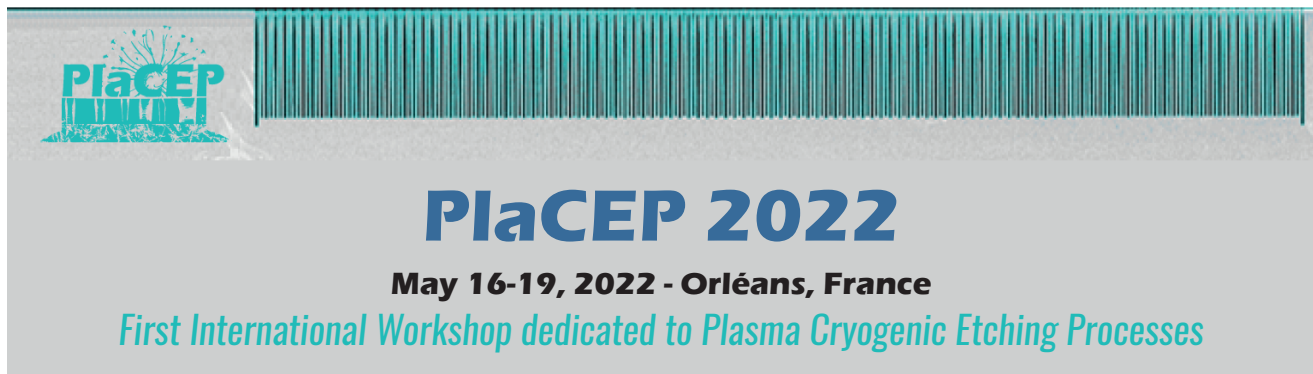
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4 Topics

First international workshop dedicated to Plasma Cryogenic Etching Processes.

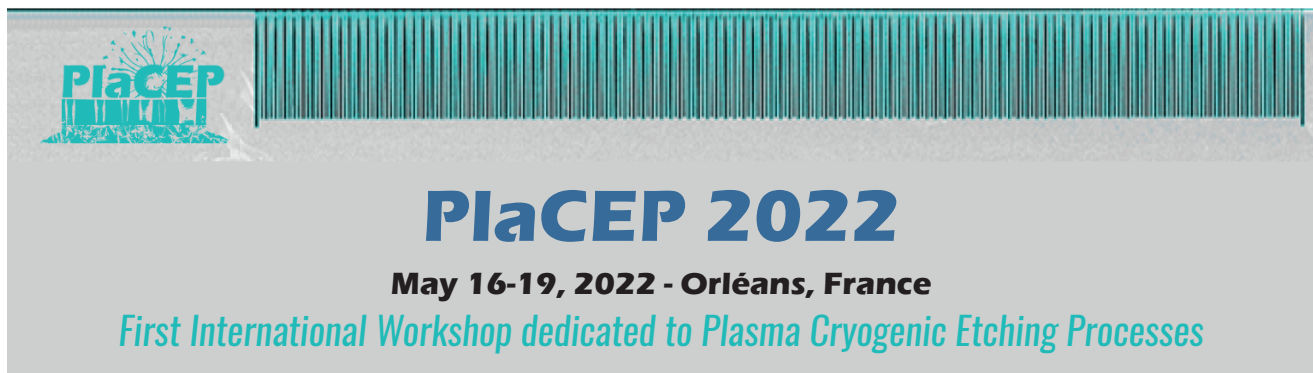
PlaCEP 2022 aims at gathering researchers and engineers working, or interested in cryogenic etching and share knowledge as well as experience in this very specific field.

- Cryogenic etching processes of silicon and other materials (low-K, ...)
- Modelling and simulation of cryogenic processes
- Passivation layer growth and surface mechanisms at cryogenic temperature
- Cryo-Atomic Layer etching
- Black silicon formation
- Cryogenic related technology



5 Abstracts

The abstracts (full-text) are collected in the following section. They are sorted according to the schedule shown in page 8.



Cryogenic etching of silicon with SF₆, O₂ and SiF₄ based plasmas: from monocyclic to time-multiplexed process

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The cryogenic process was initially developed for silicon deep etching, with applications for 3D integration in microelectronics and MEMS. It consists of exposing to a monocyclic SF₆/O₂ plasma a patterned silicon substrate cooled down to a cryogenic temperature [1]. Different benefits arise from these low temperature conditions. Firstly, a complementary modeling and experimental study has highlighted a local cooling of the gas above the wafer, increasing the gas density as well as the incoming neutral gas flow [2]. Therefore, this leads to a higher etch rate at low temperature (see comparison between 173 K and 300 K in Fig. 1). Secondly, a SiO_xF_y passivation layer is formed on the sidewalls and prevents lateral etching. This film is stable only at low temperature and has the property to desorb when the substrate is warmed back up to room temperature or under ion bombardment. O₂ proportion in the gas mixture, substrate temperature and bias are relevant parameters tuning passivation conditions, that are clearly related to an oxidation threshold where the etch stops. This has been observed by direct etch rate measurement with double spot reflectometry and mass spectrometry. These results show good correlation with the evolution of radical fluxes as a function of the same parameters, computed from a fluid model [3].

It is also shown that SiF₄/O₂ plasmas can be used to create or reinforce a passivation layer in cryoetching [1]. This led to the development of the STiGer process, which consists of cycling passivation (SiF₄/O₂ plasmas) and etching steps (SF₆ or SF₆/O₂ plasmas) to get vertical structures. This is similar to the Bosch process principle, but it is polymer free and clean since the passivation layer forms only on cooled surfaces. In addition, profiles are less sensitive to temperature variations in comparison with "standard" cryoetching. Typical profiles (Fig. 2) as well as a comparison with standard cryoetching will be presented.

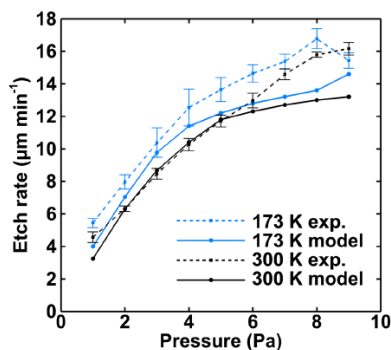


Figure 1. Computed and measured etch rates as function of pressure at 173 K and 300 K

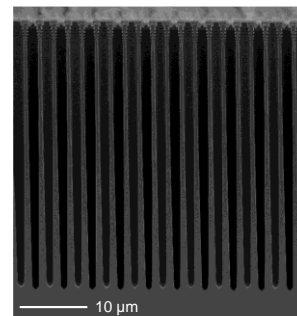


Figure 2. Deep trenches of Si (CD = 800 nm) etched with the STiGer process

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Multiscale approach for the simulation of silicon cryogenic etching under ICP SF₆/O₂ plasma mixture

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SF₆ based plasma is widely used in the dry etching of silicon. In many new devices manufacturing such as Systems in Packages (SIP) or Micro-Electro-Mechanical Systems (MEMS), deep etching of silicon without any local morphological defects like bowing, undercut or trenching is required. Cryogenic silicon etching is used by adding oxygen in order to inhibit the sidewall etching and then improve the silicon etch anisotropy. The fraction of oxygen in SF₆/O₂ plasma mixture is one of the critical parameters in the control of this process.

In order to know more about the plasma surface interaction in cryogenic ICP silicon etching process, we have developed silicon etching simulator. The model is composed of three modules: plasma kinetic model, sheath model and etching model. The plasma kinetic model is based on the 0D global approach which allows the calculation of the average densities and fluxes of neutral and ion species as well as the electron density and temperature in ICP SF₆/O₂/Ar plasma mixture versus the ICP machine parameters. Such output parameters are introduced as input parameters in the sheath model and silicon etching model. Cellular Monte-Carlo method is used to describe the plasma surface interactions in a probabilistic way for silicon etching through the mask.

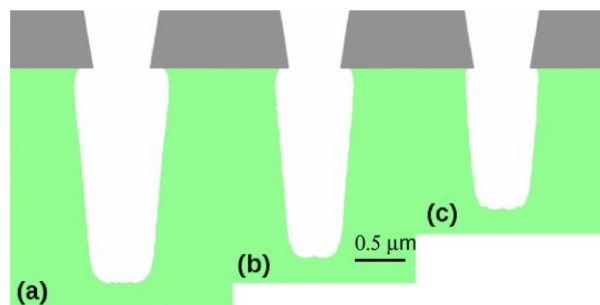


Figure 1. Silicon etch profiles for $p=10\text{mTorr}$ and $P_{RF}=2000\text{W}$, (a) $\%O_2=10\%$, (b) $\%O_2=15\%$ and (c) $\%O_2=25\%$. [1]

References

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In-situ Plasma Emission Interferometry to Control the Cryo-etching of Deep Silicon Structures

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Cryogenic SF₆/O₂ etching of silicon substrates and especially of high aspect ratio through-silicon vias (TSVs) is a challenging process of great interest for the development of sophisticated microelectronic and photonic systems [1]. Real-time control of the etch depth and quality of the structures can greatly facilitate the often complex and time-consuming process development and significantly improve reproducibility. For the in-situ monitoring of etch rate and depth, laser interferometry is conventionally used for deep reactive ion etching [1, 2, 3]. In contrast to laser interferometry, we use the optical plasma emission itself to determine the etch rate and depth, a method originally proposed for thin film plasma processing [4, 5]. It is shown for the first time that the method can also be advantageously applied to the structuring of bulk material if a suitable spectroscopic setup is used, which ensures sufficient local and temporal coherence. Since the plasma is a broadband emitter, different wavelengths are available for this purpose. Our system allows the monitoring and evaluation of multiple time-dependent wavelength intensities simultaneously, ranging from deep UV to near IR [6]. In addition to the etch depth progression, mask erosion can be detected at the same time. The potential and limits of the method are discussed using hole and trench structures with CD values from 3 to 10 μm, different pitches and aspect ratios up to 20. In addition, the full-wafer-thickness etching of optical through-silicon waveguides [7] with critical dimensions up to 250 μm is investigated.

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Cryogenic etching: Process and applications

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Cryogenic etching is used for silicon etching since the late eighties [1]. Although it has some great benefits in Deep-RIE it was always in the shadow of the well-established Bosch process [2]. Currently there is rising notice of the technology, not only for silicon etching. SENTECH offers cryogenic plasma etch tools for twenty years. We present current results on the cryogenic etching of silicon for a broad range of applications. Tuning and optimizing of the process will be shown as well as measurements of the sidewall roughness.

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Plasma Cryogenic Etching of Organic films: Technology and Challenges

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As the demand for memory continues, taller stacks of memory cells demand deeper etch at higher aspect ratios. Taller structures require increasingly more time and selectivity. Cryogenic etch offers an opportunity to improve selectivity. We will discuss the current state of the art at Applied Materials© and the critical questions that need to be answered including neutral transport, adsorption potentials, and activation barriers. The answers to these questions will help us to explain the higher etch rates as shown in **Figure 1** along with improved selectivity at low temperature as shown in **Figure 2**. © Applied Materials, Inc. All Rights Reserved

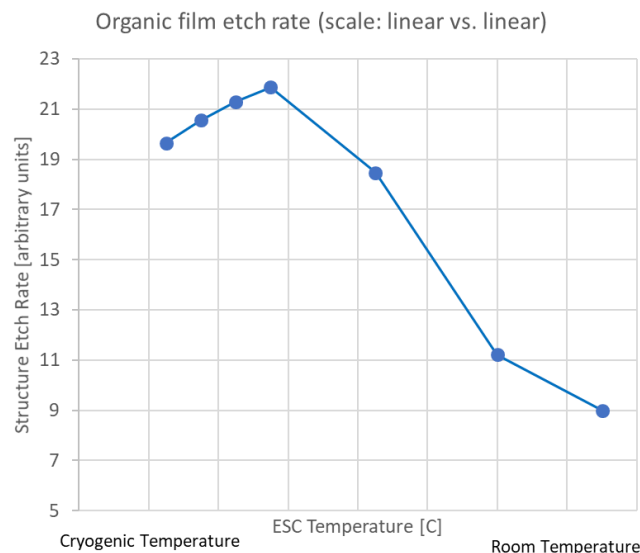


Figure 1: Etch rate dependence on temperature

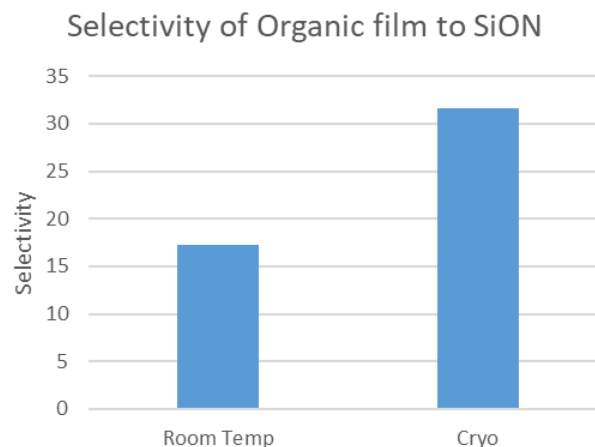


Figure 2: Selectivity improvement at low temperature

An overview of cryo-etching: from its birth to its recent renewed interest

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Thirty one years after its first introduction by a Japanese team [1], the cryoetching process is gaining again the interest of both academics and companies for advanced material etching. Initially, this process was proposed in order to freeze chemical reactions on vertical sidewalls while etching the silicon structure bottom submitted to the ion bombardment. In SF₆/O₂ standard cryoetching, it was actually shown that a passivation mechanism was responsible for the etching anisotropy [2]: a SiO_xF_y inhibiting thin film forms at the sidewalls. Such a film can be obtained at room temperature as well, but the concentration of O₂ has to be much higher to produce anisotropically etched features [3]. In this case, the passivation layer which is similar to a SiO₂ thin film remains at the sidewall after the process [4]. At low temperature, it seems that the stoichiometry of the SiO_xF_y is quite different. In addition, it was shown that a large part of the passivation layer was desorbing when warming the substrate to room temperature [5, 6]. From ellipsometry, in-situ XPS analysis and mass spectrometry measurements, different properties of cryoetching have been highlighted.

Even if very high aspect ratio structures have been obtained with the standard cryoetching process, the use of liquid nitrogen has aroused reluctance of many companies who preferred the so-called "Bosch" process to etch high aspect ratio structures. However, cryoetching offers many other possibilities that are again of interest for advanced material etching. Cryo etching was successfully used for porous SiOCH low K material etching [7]. Cooling the wafer was also recently proposed to etch dielectrics such as SiO₂ [8] and other stacks of materials [9]. Finally, cryo-Atomic Layer Etching was successfully tested to etch SiO₂, atomic layer by atomic layer [10]. All these recent developments will be presented in details.

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Benefits of cryogenic processes applied to atomic layer etching

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Several cryogenic etching studies have demonstrated the benefits of low temperature processing. Cryogenic processes reduce material damages ¹ and minimize reactor wall contamination ².

Cryogenic atomic layer etching (cryo-ALE) is proposed as an alternative to control etching while preventing process drifts due to reactor wall contamination. Indeed, at low substrate temperature, the residence time of species on the surface is increased. Therefore, the precursor can be injected in gas phase and physisorbs on the cooled substrate surface, while no adsorption occurs on the reactor walls that are maintained at room temperature. Thus, the amount of reactive species used for etching is well controlled. After this physisorption step, etching is performed as in standard ALE of SiO₂. An argon plasma etch step is performed until the self-limited etching is reached ³.

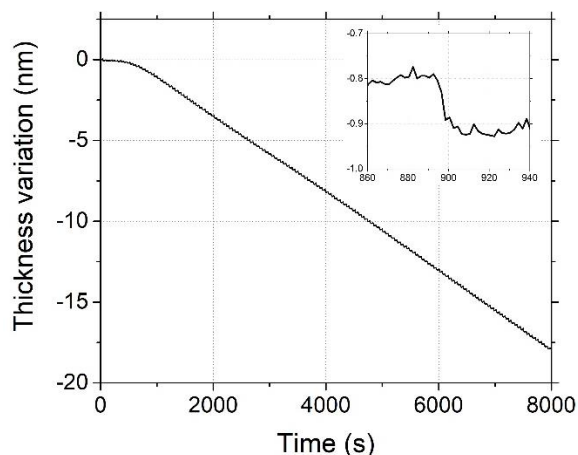


Figure 1. 150 cycles of cryo-ALE at -90°C on SiO₂

Fig. 1 presents 150 cycles of cryo-ALE performed in an ICP reactor at -90°C on SiO₂. Each cycle consists of a step of C₄F₈ injection without plasma, an Ar purge step without plasma, an Argon plasma step with a low bias and a pumping step. The etching was monitored in-situ by an ellipsometer in kinetic mode. As observed in Fig. 1, about 12 cycles were needed before reaching a steady amount of SiO₂ Etch Per Cycle (EPC) of 0.12nm. The obtained etching linearity shows that the substrate surface is the same at the beginning of each cycle, which enables the same EPC, all along the process. Mass spectrometry was used to characterize the process and study the species desorption at different pressures and temperatures. This presentation will show and explain how to better control this type of cryo-ALE process.

Acknowledgements

The authors would like to thank S.Tahara for all the discussions that helped contributing to those results.

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Study of etching process using CHF₃ gas condensed layer in cryogenic region

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For the fabrication of semiconductor devices with 3-dimensional structures, plasma etching is required to form high-aspect-ratio holes in dielectric films. However, the radicals and ion flux both decrease at the hole bottom with increasing the aspect ratio, and this leads to the etch rate decrease [1]. Therefore, we adopt a cycle process consisting of CHF₃ gas condensed layer formation and Ar plasma etching in cryogenic region. As a result, more etching species can be obtained through the condensed layer that formed at the bottom of the hole, and the etch rate can be improved.

In our research, we introduced liquid nitrogen into the lower electrode of the capacitively coupled plasma device to cool substrate. Subsequently, the condensed layer was formed by introducing CHF₃ gas. After exhausting the redundant CHF₃, Ar plasma etching was performed, then this cycle was repeated. The pressure was fixed to 4 Pa. A 60-MHz (400 W) and RF power was applied to the upper electrode and 2-MHz (500 W) power was applied to the lower electrode of 100-mm diameter. The sample was SiO₂ film on Si, and the film thickness was measured by an in-situ spectroscopic ellipsometry.

Figure 1 shows the etch rate as a function of calculated CHF₃ condensed layer thickness. Ar plasma etching time was fixed to 10 sec. It can be known the etch rate of Ar sputter when condensed layer thickness is 0. The etch rate increased almost linearly with increasing condensed layer thickness. From this result, it was considered that the CHF₃ gas introduced into the chamber was condensed on the SiO₂ surface when the stage temperature was -186°C. The etch species increased as the thicker condensed layer thickness, then the high etch rate was obtained by the impact of Ar ions from plasma.

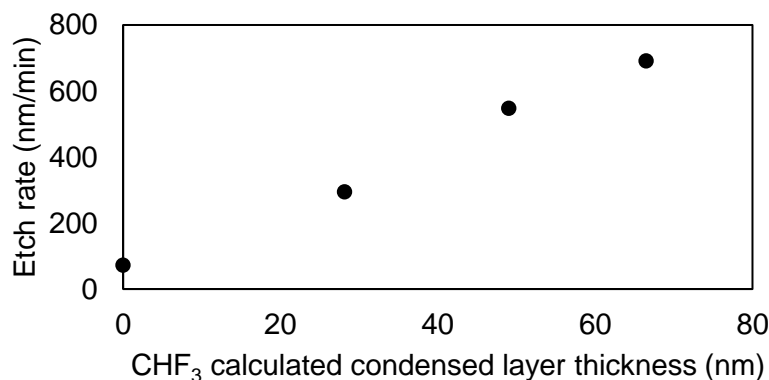


Figure 1. Etch rate by 10-sec Ar plasma etching vs. calculated CHF₃ condensed layer thickness.

Acknowledgements

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Cryo-ALE of Si and SiO₂ using SF₆ Physisorption

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Cryogenic Atomic Layer Etching (Cryo-ALE) using C₄F₈ as a precursor gas has been previously presented as an alternative method to achieve ALE of SiO₂. In this process, C₄F₈ is injected in gas phase during the “chemical modification” step, in order to physisorb on a cooled SiO₂ surface. The etching step is then achieved using an Ar plasma with a low energy ion bombardment. The temperature window of this process was between -120°C and -90°C^{1,2}. However, C₄F₈ injection at cryogenic temperatures does not allow high etching selectivity of SiO₂ over Si and Si₃N₄ as the deposited CF_x passivation layer is not thick enough to efficiently passivate Si and Si₃N₄ surfaces. As a result, another gas chemistry has to be tested in order to achieve higher etching selectivity.

In 1996, Royer *et al.* studied the chemisorption of sulfur and fluorine on Si during a simultaneous exposure to SF₆ gas and Ne⁺ ion beam. In this work, they showed by XPS measurements that the fluorine quantity on the Si surface tends to increase as the temperature decreases, for a process window between 20°C and -130°C³. Therefore cryo-ALE study based on SF₆ physisorption was carried out to extend the use of this alternative approach to other materials.

This work was carried out using a cryogenic ICP reactor equipped with in-situ diagnostics. Mass spectrometry measurements enabled to characterize the SF₆ physisorption and its surface residence time at different temperatures. Spectroscopic ellipsometry was used to monitor the etching rate and to characterize the sample surface at the nanoscale during the three process steps: SF₆ physisorption, pumping and Ar plasma etching. Tests were performed on SiO₂, Si₃N₄ and p-Si coupons glued on SiO₂ 6” carrier wafers.

SF₆ physisorption experiments will first be studied and presented notably to find the optimal temperature and purging time for the process. Subsequently, cryo-ALE test results on Si, SiO₂ and Si₃N₄ will be shown. These results will finally be compared to the ones obtained previously using C₄F₈ physisorption.

This research project is supported by the CERTeM 2020 platform, which provides most of the equipment and funded by the European Union (FEDER fund) as well as the French National Research Agency (ANR PSICRYO fund).

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OPTIMIST: a system for studying and characterizing the Plasma-Surface or Gas-Surface interaction mechanisms

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The Optimist platform is a shared tool of the CNRS Plasmas Froids network [1] located at IMN. Optimist provides a plasma reactor **directly** connected to a X-ray surface analysis equipment^a. In addition to the possibility of carrying out *quasi in-situ* analysis of treated surfaces or deposited thin layers, the specificity of Optimist lies in its sample holder, which is DC or RF biasable and controlled in temperature from -180 to $+1100$ °C.

The plasma reactor is composed of an inductively coupled RF source (ICP); 4 gas lines are currently installed. The transfer between the reactor and the surface analysis chamber as well as the surface analysis can be done while keeping the sample at the treatment temperature or any other temperature in between -180 °C / $+110$ °C.

Thanks to this equipment, it is possible to study the physical and chemical mechanisms involved in plasma surface or gas surface interaction including during cryogenic processes or high temperature treatments.

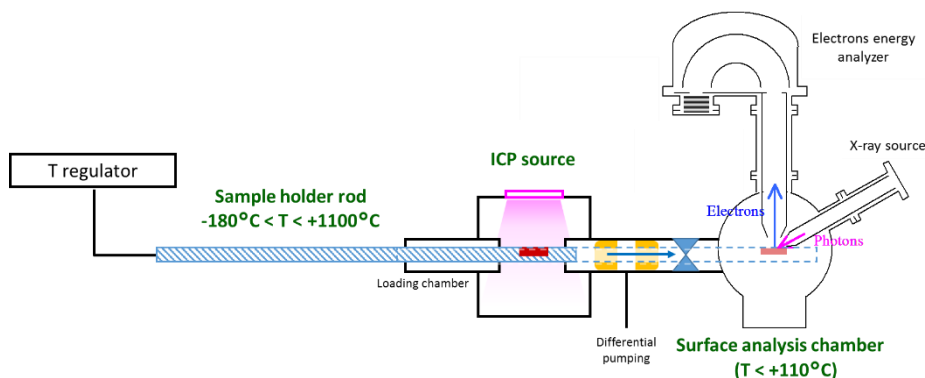


Figure 1. Schematics of the OPTIMIST platform

The presentation will detail the possibilities of the equipment when operating in cryogenic conditions. Examples will concern past and current studies such as Si passivation in SF_6/O_2 cryoetching [2], condensation of plasma CN_x species from CH_4/N_2 mixture [3] and physisorption / chemisorption mechanisms on semiconductors.

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^a The XPS system combines a monochromatised X-ray source (Specs XR50M-Focus500) and a hemispherical analyser (Specs Phoibos 150HR / 1D-DLD).

Overview on experiments of Cryo-FIBID using W, Pt and Co precursors, including the use of a thermoelectric plate

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Focused Ion Beam (FIB) equipment is a relevant tool in nanolithography to directly pattern materials and build devices. In my talk, I will introduce Focused Ion Beam Induced Deposition (FIBID), where the FIB decomposes precursor molecules in order to grow deposits. Special attention will be drawn to the use of FIBID under cryogenic conditions (Cryo-FIBID), a new technique based on the formation of a condensed layer of the precursor material via substrate cooling. By using a cryogenic module based on liquid N₂, we have applied Cryo-FIBID to grow W-C [1, 2], Pt-C [3] and Co [4] deposits, observing a few-hundred-times enhancement in the growth speed when compared to room-temperature FIBID. Applications of Cryo-FIBID to grow electrical contacts on micro-structures will be shown. The perspectives opened by Cryo-FIBID processing will be discussed, in particular the use of a thermoelectric plate reaching -60 °C [5].

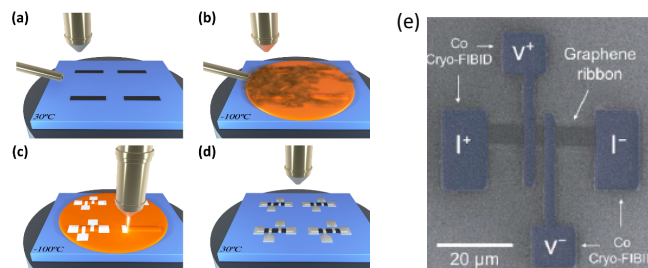


Figure 1. (a) to (d) the four steps of the Cryo-FIBID process, used to contact graphene ribbons (e) [4]

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Cryogenic Atomic Layer Etching: What Plays the Magic?

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Recently, semiconductor industry has been showing incrementing interest in cryogenic processes, particularly dry etch. As device scaling reaches its limit and Moore's law stops working, etch process is also facing unrepresented challenges that cannot be resolved using traditional approaches due to trade-offs between etch rate, selectivity, and etch profile etc. Cryogenic etch as an alternative option has showed different behaviors than room temperature or high temperature approaches. Back in 30 years ago, S. Tachi et al. observed that Si etch rate increased exponentially in SF₆ plasma when temperature was below -100°C while etch rate of photoresist (PR) and SiO₂ dropped dramatically, which means there was a huge etch selectivity boost at cryogenic temperature [1]. In 2017, Stefan Tinck et al. published HPEM (Hybrid Plasma Equipment Model [2]) simulation results, which showed much higher plasma density on wafer surface than in the bulk plasma. This can potentially cause higher etch rate at -100°C than at 20°C. [3]

In this talk, we look deeply into the gas/solid interface using DFT (density functional theory) and MD (molecular dynamics) simulation and propose an enhanced physi/chemi-adsorption mechanism which dramatically changes material etch behavior at cryogenic temperature. From the simulation results, enhanced physisorption of C₄F₈ on material surface, only at cryogenic temperature, has been observed to facilitate fast ALE (atomic layer etching) following by an Ar desorption on SiO₂, Si₃N₄ and Si without much selectivity between materials. SiF₄ plus O₂ plasma etches SiO₂ and Si much faster at cryogenic conditions and can have much higher etching selectivity to Si₃N₄ by adding H₂ treatment. Detailed selective bonding formation will be discussed with supports from DFT and MD simulation results.

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What desorption activation energies of reaction products tell about chemical etching rate of silicon?

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The chemical etching of silicon in fluorine-based plasmas is investigated theoretically. The etching process is described mathematically using chemical kinetics and transition state theory. It is shown that maximum etching rate is equal to the desorption rate of formed products

$$V_{\max} = \frac{kT}{h} \exp\left(\frac{-E_d}{kT}\right),$$

where h is the Planck constant, k is the Boltzmann constant, T is the temperature, and E_d is the desorption activation energy of i -th type species. Desorption activation energies of SiF_x species [1] found by fitting the experimental data are used to calculate maximum etching rate of silicon. When desorption activation energy is equal to 0.64 eV, the chemical etching rate equals to one monolayer per hour at temperature $T = 200$ K. In practice, the etching rate can be much higher because of thermal heating of the reaction layer by the exothermic chemical reactions and poor thermal contact between substrate and substrate holder. These processes change effective temperature of the reaction layer but do not affect the desorption activation energy.

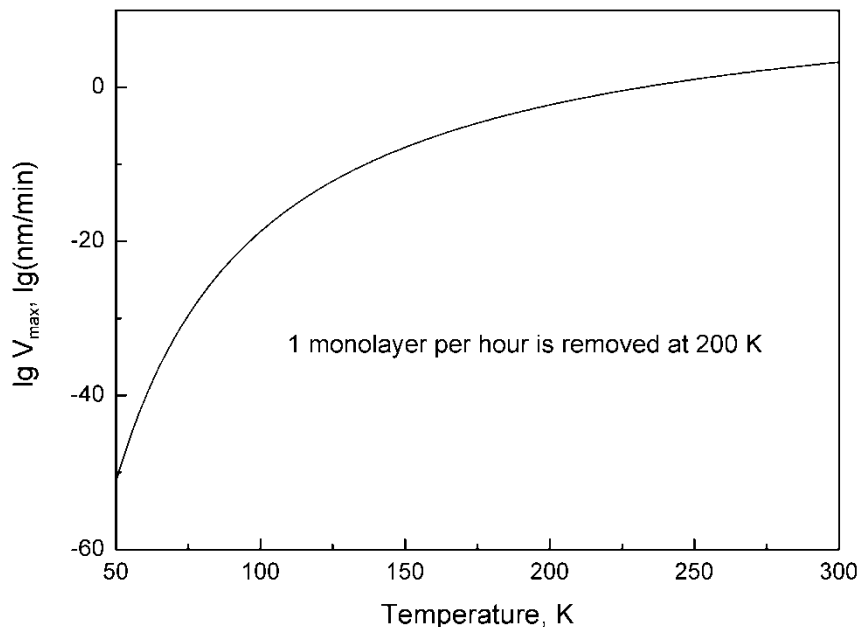


Figure 1. The theoretical dependence of maximum etching rate of silicon in the fluorine-containing plasmas on temperature.

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Cryoplasma as a unique approach to cryogenic world

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Looking back on the history of plasma science and technology, new types of plasma sources, such as atmospheric-pressure low-temperature plasmas, have been leading and established various innovative applications for materials design, agriculture and bio-medicals [1]. Our group has developed a novel plasma source called cryoplasma [2], that is a low-temperature plasma whose gas temperature can be controlled continuously at wide range of cryogenic temperatures lower than room temperature (Fig. 1), by limiting the spatial (< 1 mm) and temporal (< 100 ns electrical or optical excitation) scales of the plasma. The development of cryoplasma potentially extends the current applications of low-temperature plasma to cryogenic temperatures, with promising applications in materials processing, bio-medical and semiconductor industry.

In this talk, we will give a topic about characteristics and application of cryoplasma [3, 4]. Furthermore, as a more recent topic, we will also introduce cryoplasma in contact with ice, that is expected to provide very unique materials science and processing [5, 6].

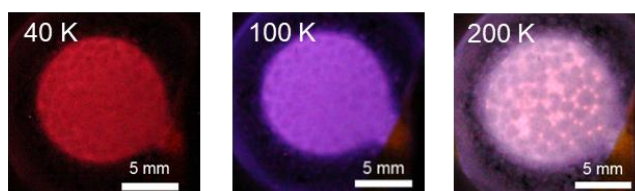


Figure 1. Images of cryoplasma generated at different cryogenic temperatures in contact with ice [5]

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Effect of Liquid Nitrogen Cooling on Plasma-exposed Gallium Nitride

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These days, gallium nitride (GaN) has a huge demand on the application to high-power devices; the wide-bandgap makes the devices even smaller. Talking about device miniaturization, we cannot neglect material processing with plasma. Plasma gives a benefit in etching and deposition in material processing through the generation of the energetic species, e.g., ions and radicals, but also giving a drawback in making undesiring process; creation of damage after plasma processing. Therefore, we need to understand the damaging process for plasma-exposed GaN. To understand plasma-exposed GaN, we exposed GaN to argon plasma which was expected to make mainly physical damages rather than chemical reactions between plasma and GaN surface. We evaluated the degree of damage by observing the evolution of the fluorescent spectrum, how much damage the plasma gave and what affected the spectrum evolution etc. Our experiment showed that the evolution of the uorescent spectrum after plasma exposure can be minimized by using LN2; LN2 enabled a small amount of change in the spectrum after plasma exposure. Also, the no-LN2 cooling result showed that plasma exposure affected mainly on the yellow luminescent range (480 - 700 nm) decreasing and on the blue luminescence range (400 - 480 nm) increasing. The giving presentation will show more details and analyses based on our publication.

The technology of cryo-etching

M Cooke, Z Ren

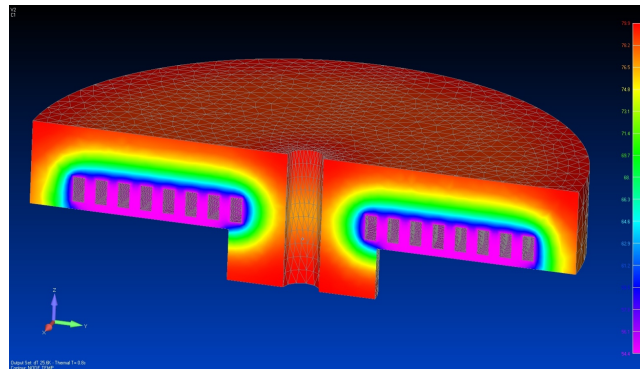
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The introduction of cryogenic etching is traced from early lab experiments to its commercial introduction. There were technological challenges including safety; temperature control of an RF-biased table; cryogenic cooling; useful cooling and heating rates; sealing technology; sample temperature and table temperature differences, and maintaining temperature uniformity. Heat transfer between sample and table is reviewed, and the prospects for direct substrate temperature measurement and control are considered.

The design was adapted for non-cryogenic cooling with conventional fluids, and also as a heated rf-biased etch table to assist etching of low volatility compounds such as indium compounds and even copper. More recently, an electrostatically clamped version has been evaluated. The barriers to introduction beyond the laboratory are considered.

Cryo-etching of silicon is often considered as a complementary technology to gas-chopping processes for deep silicon etching, which has also developed considerably. We present the latest results in silicon etching comparing these alternatives.



Figures: Wide range electrostatically clamped wafer table (left) Thermal simulation (right)

Acknowledgements

The contributions of engineering and technology teams at OIPT over 25 years is acknowledged with gratitude. Good work, people.

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Low damage plasma etching of porous dielectrics using cryogenic temperature: a review

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The use of cryogenic temperature for porous dielectrics has received extensive attention in the last few years. The work was initiated by an early experiment [1], attempting to explore the use of cryo-plasmas for dielectric etching. Subsequent tests were performed by Zhang [2] using SF₆-based plasmas, with only the wafer cooled to low temperature. This resulted in the appearance of unusual by-products, visible by FTIR, and stable at room temperature. They were identified as alkyl alcohols and aldehydes, present in large relative amounts, i.e. condensed into the pores. In order to enhance and control condensation, C₄F₈ was added into the process, leading to controlled micro-capillary condensation around -110°C [3]. The patterning of nanostructures, using a SF₆/C₄F₈ plasma at -109°C, was demonstrated for 30 nm lines. Fab integration constraints prevent the use of liquid-N₂ cooled plasma chambers, requiring to look for precursors enabling pore filling at T > -60°C. High-boiling point molecules used for cryogenic low-k etch need to cumulate multiple physical and chemical properties: low vapor pressure in the temperature range of interest, ability to wet Si-CH₃ terminated surfaces, low molecular radius and high molecular flexibility, stability of the condensed phase, plasma-induced molecular fragmentation enabling plasma etch and low chamber contamination. Systematic molecular screening allowed to pin-point a particular high molecular weight CF_xO_y linear monomer, *nerima* (HBPO) [4]. Combined with NF₃, this gas allows the formation of a stable condensate at -40°C, full low-k protection (see figure 1) and good patterning capabilities.

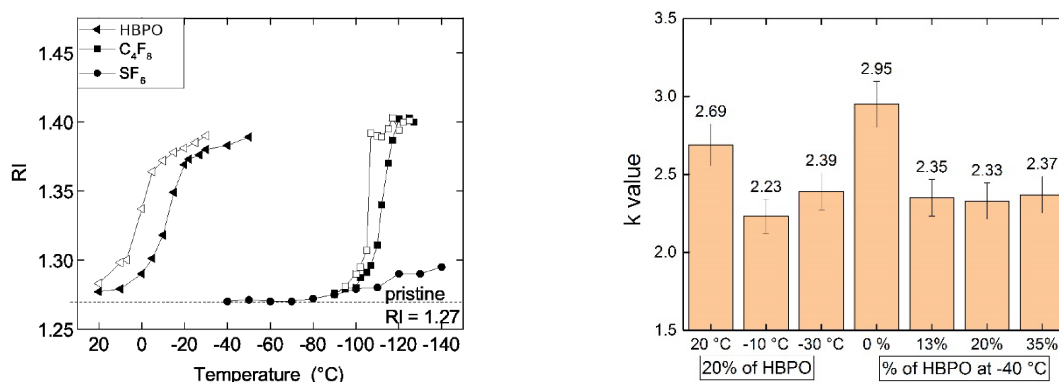


Figure 1. (Left) condensation isobars for SF₆, C₄F₈ and *nerima* (HBPO) into a 34% porous ultra-low-k [4]. RI = refractive index. (Right) Low-k plasma damage reduction: post-etch k-values as a function of processing temperature and HBPO content, in a NF₃-*nerima* (HBPO) mixture [5].

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Formation of Black Silicon through mask free plasma etching at non-cryogenic temperatures

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Since Black Silicon (b-Si) can significantly reduce reflection losses and simultaneously enhance light scattering, it is attractive for solar cells and other optical devices. A common fabrication technique is the mask free plasma texturing, usually performed at cryogenic temperatures. To get rid of the expensive nitrogen cooling, we investigated the formation of non-cryogenic b-Si at temperatures above 0 °C. Experimentally, we developed b-Si wafers with a strongly increased absorption and excellent minority carrier lifetimes (~ 2 ms). These optoelectronic properties are as good as those prepared by cryogenic processes and are also sufficient for PV applications. We further analyzed the b-Si formation by different surface-sensitive characterization methods such as XPS, Raman, SEM and TEM. As one result, a 1 nm thin SiO_xF_y layer is observed on the wafer surface during the texturing, which confirms the “selfmasking” process as it is already described for low-temperature processes. These findings agree well with the outcome of our b-Si modeling. Here, we assume that the initial nano-roughening is only affected by local temperature inhomogeneities on the surface and ignore the impact of directed plasma ions. This novel approach is verified by a linear stability analysis of the surface mechanisms with the result that plasma particle diffusion along the surface is the main factor for nano-roughening.

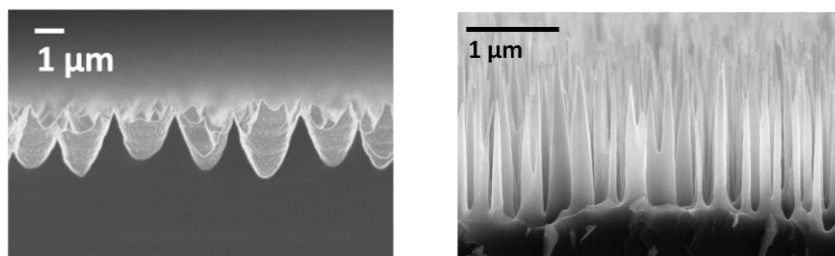


Figure 1. Experiments: Two different B-Si textures (Left: parabolic microstructures, Right: Needle-like nanostructures) prepared by mask free plasma etching at temperatures > 0 °C.

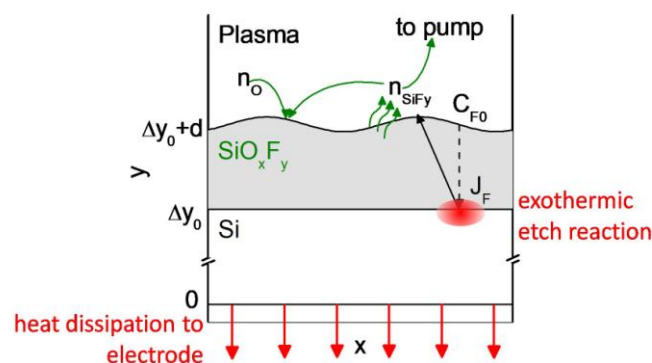


Figure 2. Simulation: Schematic of the considered mechanisms at the silicon surface during plasma etching (n_0 – oxygen flow in the plasma, n_{SiF_y} – surface density of SiF_y molecules in the plasma, Δy_0 – Si wafer thickness, d – SiO_xF_y thickness, C_{F0} – F concentration in the plasma, J_F – current density of F)

High-aspect-ratio silicon nanowire arrays by cryogenic and chemical etching

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Vertical arrays of silicon nanowires fabricated directly on top of silicon wafer has met a wide range of applications particularly in portable electronic devices, from MEMS and sensors to microscale energy harvesting and energy storage systems [1–3]. The ability of integrating the process into semiconductor fabrication lines is crucial for the adoption into large-scale manufacturing. Here, silicon nanowire arrays fabricated by cryogenic inductively coupled plasma reactive ion etching (ICP-RIE) is presented. The process was optimized in order to obtain high-aspect-ratio nanowires of more than 20. Further increase of the aspect ratio has been achieved by decreasing the nanowire diameter using the combination of thermal oxidation and chemical etching using hydrofluoric acid (HF). By applying this hybrid process, vertically aligned silicon nanowire arrays with an aspect ratio of up to 93 with relatively smooth and vertically straight sidewalls have been realized, showing a potential method for implementation in miniaturized semiconductor devices.

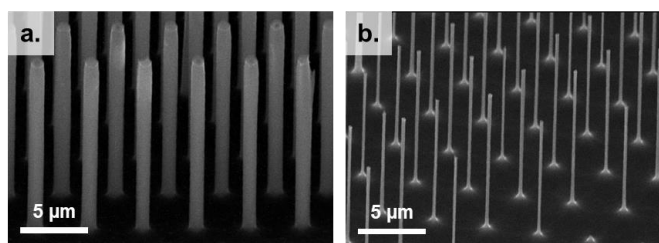


Figure 1. Vertically aligned silicon nanowire array fabricated by subsequent (a) cryogenic ICP-RIE and (b) 3 cycles of thermal oxidation and HF etching.

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This work was conducted within a project of SiNanoBatt funded by the German Federal Ministry of Education and Research (BMBF) and Indonesia Endowment Fund for Education (LPDP) under the Southeast Asia – Europe Joint Funding Scheme for Research and Innovation. This project has received funding from the EMPIR program co-financed by the Participating States and from the European Union's Horizon 2020 research and innovation program under No. 19ENG05 Nanowires.

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Simulation of flowing liquid nitrogen using Lattice Boltzman method

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The low kinematic viscosity of liquid nitrogen (about one-fifth of the water viscosity at room temperature) places special demands on the surface morphology of used materials in order to regulate their hydrophilic and hydrophobic properties.

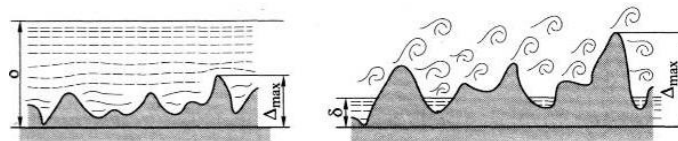


Figure 1. Schematic presentation of the liquid nitrogen flow

The flow of liquid nitrogen near the structured surfaces is simulated using regulators in the MatLab software package. It is shown that the regulators introduced in the Boltzmann lattice increase the accuracy of Newtonian fluid parameters (front shape, turbulence and velocity distribution) in the vicinity of structured surfaces. Depending on the adhesion, the flow rate, and the Reynolds number behind the ridges, turbulence or even cavitation zones form in the flow of liquid nitrogen. This significantly affects the flow in the narrow channels. The surface roughness of used materials required to obtain hydrophilic surfaces are determined.

Silicon cryogenic etching processes for the fabrication of high aspect ratio metasurfaces

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Metasurfaces are structured surfaces used to manipulate light at an unprecedented level, which typically consisting of planar arrays of resonant structures much smaller than the wavelength of the electromagnetic field. By using metasurfaces, the phase, polarization, amplitude, and dispersion of the transmitted or reflected electromagnetic field interacting with the surface can be controlled. [1]

The present study focuses on the fabrication of high aspect ratio structures consisting of artificial patterns of subwavelength dimensions obtained by cryogenic etching of silicon. For this purpose we have used a PlasmaLab 100 system (Oxford Instruments, UK), fitted with a 120 liter dewar for liquid nitrogen cooling. We will discuss the effect of different masking layers on the end results, as well as considerations taken for ensuring process reproducibility as well as decreasing surface roughness.

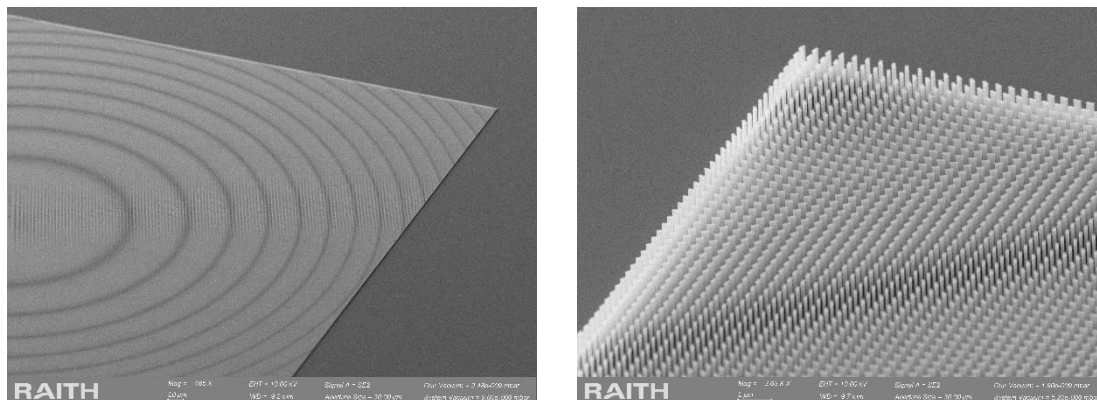


Figure 1. SEM image of metasurface fabricated by cryogenic etching of silicon: (left) 165x magnification, (right) detailed view showing orientation of etched pillars

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DRIE / Silicon Ultra Low Temperature Plasma Etching:

Its applications, limitations & evolution

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In recent decades, much research has been done on ways to increase the performance of silicon technologies while reducing their cost of production. In order to remain competitive in the highly competitive market of semiconductor & M(O)EMS (Micro (Opto) Electro Mechanical System), companies must reduce their cost by about 25% per chip per year. To achieve this, many objectives are set as: decreased chip size thanks to the DRIE technology allowing 3D integration, increase the size of substrates, but also process optimization and etching equipment to maximize productivity.

Even if there are some challenges, Deep Plasma Etching becomes a key technique in the fabrication of semiconductor devices for microelectronic companies. The key of future success is the mastering of this unique technology by a better control and widespread use.

To better understand and control this technique, one needs to know more about: plasma, Hardware, the way of controlling the process to obtain the best performances on etch profile. Nevertheless, even with this, some technical issues and limitations in performance remain. To go further in the mastering, we need also to have a global vision of the whole technique such as process monitoring and profile simulation, in order to lead it to industrialization and make it evolve.

