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Abdelhalim Saadi, Marc Margalef-rovira, Youcef Amara, Loïc Vincent, Sylvie Lepilliet, Christophe Gaquière, Philippe Ferrari

Received: 27 December 2021 | Revised: 5 April 2022 | Accepted: 18 April 2022

IET Microwaves, Antennas & Propagation

DOI: 10.1049/mia2.12260

The Institution of Engineering and Technology WILEY

ORIGINAL RESEARCH

Innovative millimetre-wave resonators based on slow-wave coplanar stripline components

Abdelhalim A. Saadi[1] | **Marc Margalef-Rovira**[2] | **Youcef Amara**[3] | **Loïc Vincent**[4] | **Sylvie Lepilliet**[2] | **Christophe Gaquiere**[2] | **Philippe Ferrari**[3]

[1]NXP Semiconductors SAS, Toulouse, France

[2]IEMN, Université de Lille, Villeneuve d'Ascq, France

[3]RFIC-Lab, Grenoble INP, Université Grenoble Alpes, Grenoble, France

[4]Grenoble INP, Grenoble, France

Correspondence

Abdelhalim A. Saadi, NXP Semiconductors SAS, 134 Avenue du General Eisenhower, Toulouse, France.

Email: abdelhalim.saadi@nxp.com

Abstract

In this paper, the slow-wave coplanar stripline (S-CPS) technology is utilised to design high performance and small footprint resonators operating within the millimetre-wave band from 50 to 80 GHz. The proposed resonators are designed based on high quality factor quasi-lumped capacitances and inductances offering a great flexibility in terms of design. The derivation of these components from the S-CPS is explained theoretically and their behaviour is validated by EM simulation; an equivalent electrical model is also developed. The proposed concepts are demonstrated in the BiCMOS 55-nm technology, and a good agreement between modelling, EM simulation and measurement results is achieved. The proposed devices could later be considered as interesting elementary blocks for the design of mm-wave filters.

1 | INTRODUCTION

The development of the microelectronics industry has effectively contributed in the growth of various sectors such as aerospace, security, automotive, health and care, and telecommunications, among others. In most of these fields, the radio frequencies (RF) were used as a carrier to transmit the big amount of the generated data. Due to the increase of this data, the current generation of wireless circuits and systems is being pushed to operate beyond RF spectrum and go towards the millimetre-wave (mm-wave) frequencies.

In response, the semi-conductor companies propose advanced CMOS/BiCMOS technologies to fulfil the current industrial trends. Technologies featuring devices with higher f_t and f_{max} have been developed, enabling full benefit of the advantages of the mm-wave spectrum to reach wider frequency operating bands [1–3]. However, realising high quality integrated passive devices based on lumped components are still challenging at mm-waves, due to (i) increased conductors' losses leading to weak quality factor (Q-factor), in particular for capacitances and (ii) increased parasitic effects leading to more complex designs for inductances and transformers. For example, a measured Q-factor of 10 and 15 at 60 GHz for MOM (Metal-Oxyde-Metal) capacitances and spiral inductance, respectively, have been reported in ref.[4]. In ref.[5], the measured Q-factor of MOM capacitances realised in a BiCMOS 55-nm technology goes from 14 at 60 GHz to less than 9 at G-band (140–220 GHz). Thus, the more favourable BEOL (Back-End-Of-Line) of BiCMOS technologies makes it possible to significantly improve the quality factor of inductors and capacitors, but this remains very limited.

To address these issues, designers prefer using transmission lines (Tlines) above around 50-80 GHz, since their design is more straightforward and their dimension becomes acceptable at mm-wave frequencies. Conventional integrated Tlines are microstrip lines and coplanar waveguides (CPW), the CPW

This work was performed while employed by RFIC-Lab, Grenoble INP, Université Grenoble Alpes, 38000 Grenoble, France.

topology being used only when dealing with SOI substrates due to unacceptable substrate losses occurring in bulk technologies [6]. Since the mid-2000s, a new type of integrated Tlines has started to be developed, the slow-wave Tlines. They lead to a higher Q-factor as compared to microstrip lines. The concept of slow-wave (SW) was firstly proposed in ref.[7] for coplanar waveguides (CPW) and in ref.[8] for coplanar striplines (CPS), leading to Slow-wave CPW (S-CPW) and Slow-wave CPS (S-CPS). Models were further developed in ref. [9, 10] for S-CPW. The method developed in ref.[10] can also be used to model S-CPS. Subsequently, circuits were designed with the SW concept, mainly based on S-CPW as in ref.[11] where a 60-GHz bandpass filter was realised to demonstrate the performance that could be achieved with S-CPW. The Q-factor improvement in SW Tlines (S-CPW or S-CPS) is obtained thanks to the use of a shielding layer underneath the strips, which (i) drastically reduces the electric field interaction with the lossy silicon substrate and (ii) separates magnetic and electric fields (thus slowing the wave and increasing the propagation constant β). The SW concept also provides the benefit of longitudinal dimensions shrinking, thus leading to shorter Tlines. However, their width is larger as compared to their microstrip lines counterpart, resulting in comparable areas; the comparison depending on the characteristic impedance being considered. In ref.[11], resonators were realised by using a distributed approach of the S-CPW, that is, quarter wavelength stubs. It demonstrated the superiority of S-CPW as compared to microstrip lines in terms of insertion loss, but led to large footprint, even at mm-waves.

Between lumped and distributed approaches, the semi-lumped approach can be very interesting to consider. It consists in using Tlines, well defined from their robust characteristics, that is, characteristic impedance and guided wavelength, and in producing components of small size compared to the wavelength, hence the term quasi-lumped. This concept was proposed in ref.[12] to realise high-Q-factor quasi-lumped inductances and capacitances based on the S-CPS topology. The resulting components were used in designing a 40-GHz LC resonator implemented in the low-cost 0.35-µm CMOS technology from AMS. Starting on the results presented in ref.[12], the current paper provides an in-depth study of the equivalence between the S-CPS and the quasi-lumped component's behaviour. Next, their potentialities are demonstrated through the design of mm-wave resonators operating at various frequencies, from 50 to 80 GHz, realised in an advanced BiCMOS 55-nm technology from STMicroelectronics. It will be shown also how the quasi-lumped approach is the best compromise between the size and electrical performance when considering the frequency range from 50 to 100 GHz.

The paper is organised as follows. In Section 2, the principle of S-CPS topology is described and the method to derive the quasi-lumped inductance and capacitance is shown theoretically. It is based on the modelling proposed in ref.[9, 10] for S-CPW. In Section 3, several topologies of resonators based on the quasi-lumped components are presented, highlighting the high flexibility of the components design. Measurement results are compared to EM simulation and the electrical model developed for the quasi-lumped components, showing a good agreement. In Section 4, a comparison to the state-of-the-art is performed. Finally, the conclusion is carried out in Section 5.

2 | SYNTHESIS OF HIGH Q-FACTOR INDUCTANCE AND CAPACITANCE WITH S-CPS

2.1 | S-CPS principle

As sketched in Figure 1a, the S-CPS is made up of two parallel strips laid out on the top thick metal layer of the BEOL shown in Figure 1b, a lower metal layer being used to realise the floating shield made up of thin ribbons placed perpendicularly to the propagation direction. The floating shield ensures slow-wave propagation, as described in ref.[13]. As it will be shown later, two metal layers can be stacked to realise thicker strips in order to reduce the metallic losses, and the BEOL in Figure 1b could be used in various stack-ups. According to the notations in Figure 1, the strips thickness, width and length are (t), (W) and (l), respectively. They are spaced from a distance (G). We define also the total S-CPS width as (D), which is equal to $(2 \cdot W + G)$. The height between the CPS strips and the floating shield is (h). As explained in ref.[13], the floating shield brings a capacitive effect that increases the linear capacitance as compared to a classical CPS, without modifying the linear inductance, thus leading to slow-wave behaviour. Furthermore, it practically cancels the interaction between the electric field and the lossy silicon substrate. Both effects result in a Q-factor improvement, as compared to conventional transmission lines such as microstrip, CPS or CPW. As discussed in ref.[9], the floating ribbons are patterned in a way that they are able to capture the electric field, with spacing SS lower than the height (h). Also, their width must be limited to avoid eddy current losses, but not too narrow to limit the

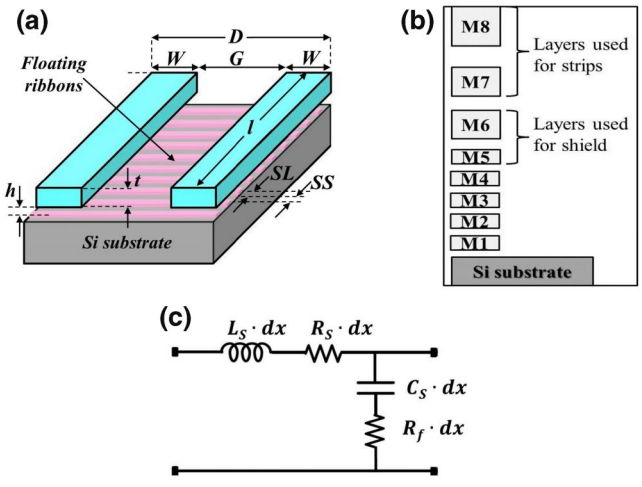

FIGURE 1 S-CPS description. (a) 3D topology, (b) the BEOL of the BiCMOS 55-nm of STM. Thickness of M8 is 3 µm, and (c) RLRC model associated to elementary section of S-CPS with a length of $dx = (SS + SL) \ll \lambda_g$ [9]

metallic losses, thus leading to a trade-off. To fulfil this trade-off, SL and SS were both set to 0.6 μm, for all the designs presented in this paper. With the availability of these parameters, more interesting designs could be performed using the S-CPS in comparison with the conventional microstrip line, for instance, (1) a wider range of synthesisable characteristic impedances, (2) shorter physical length for the same phase shifting thanks to the slow-wave effect, (3) a higher Q-factor and (4) a possibility of designing high Q-factor quasi-lumped capacitance/inductance as discussed in this paper.

The RLRC distributed electrical model initially proposed for the S-CPW topology in ref.[9] is also valid for the S-CPS topology; it is depicted in Figure 1c. The method developed in ref.[10] was used for the calculus of the RLRC elements of the S-CPS model. Briefly, L_S and R_S represent the series linear inductance and resistance; C_S is the linear capacitance between the strips and the floating shield, and R_f is the linear resistance of the floating ribbons. Then, this model was used for the synthesis of the S-CPS based quasi-lumped inductance and capacitance in the next sub-sections. The use of the model makes the design much faster as compared to the use of time-consuming EM simulations.

2.2 | Quasi-lumped capacitance based on S-CPS

2.2.1 | Calculation of the equivalent capacitance

As stated in the introduction, a high Q-factor capacitance can be designed from the S-CPS structure. We first remind in this sub-section that the input impedance of an open circuited S-CPS, whose electrical length is below $\lambda_g/4$, where λ_g represents the guided wavelength, can be equivalent to a quasi-lumped capacitance, which is a well-known behaviour of an open-ended stub with this consideration, and we give the expression of the equivalent capacitance. Next, the derivation of the Q-factor of the capacitance is presented.

Let us consider the equivalence illustrated in Figure 2, where an S-CPS is terminated with an open circuit and seen from its input; the input impedance $Z_{in_{cap}}$ calculated using ABCD matrix is given in Equation (1).

$$Z_{in_{cap}} = \frac{A}{C} = Z_C/\tanh(\gamma l) \tag{1}$$

with $\gamma = \alpha + j\beta$ the complex propagation constant, α the attenuation constant, β the propagation constant, l the transmission line physical length and Z_c its characteristic impedance, respectively.

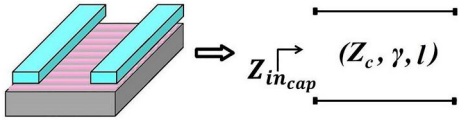

FIGURE 2 Equivalent model for S-CPS terminated with open circuit

By considering the lossless case, that is, $\gamma = j\beta$, $Z_{in_{cap}}$ can be written as in Equation (2):

$$Z_{in_{cap}} = Z_C/j\tan(\beta l) \tag{2}$$

The equivalent capacitance C_{eq} is deduced from:

$$Z_{in_{cap}} = \frac{1}{j\omega \cdot C_{eq}} = Z_C/j\tan(\beta l) \tag{3}$$

Consequently, the expression of the equivalent capacitance is as follows:

$$C_{eq} = \frac{\tan(\beta l)}{\omega \cdot Z_c} \tag{4}$$

Expression (4) is a well-known result. The quasi-lumped equivalence is valid for a physical length lower than about $\lambda_g/8$, where λ_g is the guided wavelength, as mentioned in ref. [14], in order to avoid too great dispersion. In that condition, for the sake of simplicity, the approximation in Equation (5) can be considered, leading to the new simplified expression of C_{eq} given in Equation (6):

$$\tan(\beta l) \approx \beta l \tag{5}$$

$$C_{eq} \approx \frac{l \cdot \sqrt{\varepsilon_{reff}}}{c_0 \cdot Z_c} = C_s \cdot l \tag{6}$$

with c_0 the light velocity in vacuum, ε_{reff} the relative effective dielectric constant, and C_s the linear capacitance of the RLRC electrical model of the S-CPS.

2.2.2 | Calculation of the equivalent capacitance quality factor

The quality factor of the equivalent capacitance C_{eq} can be expressed using $Z_{in_{cap}}$ in Equation (1):

$$Q_{eq-C} = \mathrm{Imag}\left(Z_{in_{cap}}\right) \Big/ \mathrm{Real}\left(Z_{in_{cap}}\right) \tag{7}$$

After some simple calculations, we get Q_{eq-c} expression:

$$Q_{eq-C} = \frac{\tan(\beta l) \cdot \left[1 - (\tanh(\alpha l))^2\right]}{\tanh(\alpha l) \cdot \left[1 + (\tan(\beta l))^2\right]} = \frac{\tan(\beta l)}{\tanh(\alpha l)} \cdot \eta \tag{8}$$

$$\eta = \frac{1 - (\tanh(\alpha l))^2}{1 + (\tan(\beta l))^2} \tag{9}$$

Let us apply to Equation (8) the conditions $l < \lambda_g/8$ and the approximation $\alpha l \ll 1$, since the S-CPS is a low loss transmission line. We get:

$$Q_{eq-C} = (\beta/\alpha) \cdot \eta \quad (10)$$

At low frequency when $\beta l \ll 1$, η is equal to the unity and $Q_{eq-C} = (\beta/\alpha)$, which is twice the well-known Q-factor of a transmission line.

This means that the quality factor of the equivalent capacitance of an open-ended stub is twice the quality factor of the transmission line that is used for the stub. Since the S-CPS has, like the S-CPW, a high quality factor, which can reach more than 30 depending on the used technology, the equivalent capacitance quality factor can reach more than 60, which is much higher than the quality factor obtained with MOM capacitances at mm-wave frequencies [4, 5].

2.2.3 | Quasi-lumped inductance based on S-CPS

The methodology is similar to that used for the equivalent capacitance, with the conventional use of a short-circuited stub instead of an open-ended stub, as illustrated in Figure 3. The input impedance calculated using ABCD matrix for a lossless S-CPS is expressed in Equation (11).

$$Z_{in_L} = \frac{B}{D} = Z_C \cdot \tan(\beta l) \quad (11)$$

The equivalent inductance is derived as:

$$L_{eq} = Z_C \cdot \tan(\beta l)/\omega \quad (12)$$

By proceeding in the same way as to derive the expression of C_{eq}, we obtain:

$$L_{eq} \approx \frac{Z_c \cdot l \cdot \sqrt{\varepsilon_{reff}}}{c_0} = L_S \cdot l \quad (13)$$

with L_S the linear inductance of the RLRC electrical model of the S-CPS.

Similarly also the quality factor of the equivalent inductance is twice the quality factor of the S-CPS, at low frequency when $\beta l \ll 1$:

$$Q_{eq-C} = Q_{eq-L} = (\beta/\alpha) \quad (14)$$

2.3 | S-CPS geometries for quasi-lumped capacitance and inductance synthesis

As stated in Section 2.1, the S-CPS electrical model proposed in ref.[9] and coded in an algorithm in reg.[10] was used for fast synthesis of the quasi-lumped capacitance and inductance without using EM simulation. Based on this algorithm and using the BEOL of the 55-nm BiCMOS technology, a wide study was carried out at 60 GHz to plot design graphs for the synthesis of quasi-lumped capacitances and inductances. Even if the study presented herein was carried out at a particular frequency, the conclusions can be extrapolated at frequencies from a few tens of GHz to more than 100 GHz, for which the S-CPS model used is still valid. This study also demonstrates the flexibility of the S-CPS since the targeted value of capacitance and inductance can be realised in various configurations thanks to the design parameters offered by the structure (i.e. t, h, G, L and W).

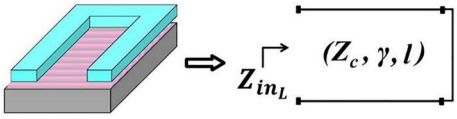

FIGURE 3 Equivalent model for S-CPS terminated with short circuit

Moreover, it is also important to mention that the model of a Tline (the S-CPS in our case) is much more robust as compared to that of spiral inductances, or MOM or parallel plate capacitances at mm-waves, in particular concerning the Q-factor, since no physical discontinuities are present, as the ones presented by vias in MOM or parallel plate capacitances, and because it takes into account the distributed nature of the electric and magnetic fields together, unlike inductors for which the electric field constitutes an element that can be qualified as parasitic because it leads to parasitic capacitances. Hence the proposed approach leads to both high flexibility and modelling robustness.

The results of the study are plotted in Figures 4 and 5. The equivalent quality factor $\left(Q_{eq}\right)$ was plotted using Equation (7) for C_{eq} and a similar expression for L_{eq}. A value of $t = 5$ µm was used, considering a stack of two thick metal layers.

Figure 4 illustrates the behaviour of the capacitance/inductance values and the associated Q_{eq} versus the S-CPS length (l) and total width (D). Three cases were considered for (D), namely, 50, 60 and 70 µm. Results are plotted in Figure 4a–c, respectively.

Higher L_{eq} inductances are reached with wider (G), which was expected, the magnetic flux being stronger, and hence the linear inductance of the S-CPS. On the contrary, C_{eq} decreases with (G), since (W) decreases for a given (D). This is due to the decrease of the S-CPS linear capacitance, which is almost proportional to (W), due to the presence of the floating shield. Also, both C_{eq} and L_{eq} increase with the length (l).

Another important conclusion that can be carried out is that higher Q_{eq} is obtained for wider S-CPS. This is due to the fact that the linear inductance of the S-CPS increases with (G), as already mentioned above, resulting in a higher S-CPS Q-factor. However, for a given value of width of the structure (D), there is an optimum set of gap between the strips (G) and width of the strips (W) leading to maximum Q_{eq}. This optimum results from a compromise between the intrinsic series resistance of the S-CPS, which increases when (W) decreases, and the value of the inductance, which increases with (G). The optimum value for (G) increases with (D), since for a given (G), (W) increases with (D). The optimum (G) is between 20 and 30 µm. Another important observation is that Q_{eq} decreases when the device length (l) increases. This was predicted by Equations (8) and (9), where the term η decreases with l.

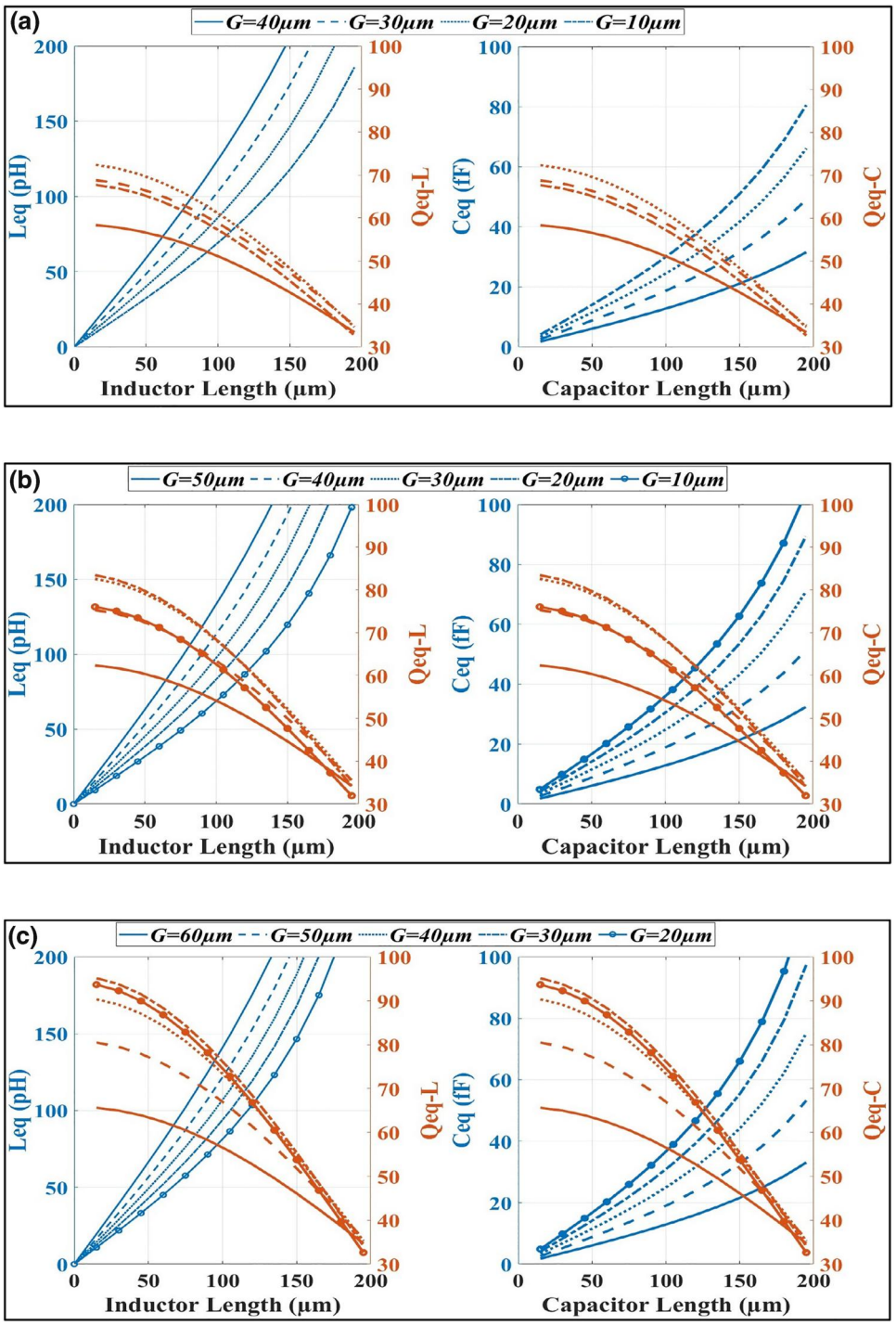

FIGURE 4 S-CPS based quasi-lumped device performances at 60 GHz for several planar dimensions, where $t = 5$ μm and $h = 2$ μm. The curves in blue are for the capacitance/inductance values. The curves in orange are for the Q-factor values. (a) For $D = 50\ \mu m$, (b) for $D = 60\ \mu m$, and (c) For $D = 70\ \mu m$

Figure 5 figures out the impact of the shield position (height) on the performance of the S-CPS components. For this study, a total width (D) of 60 μm was considered. The behaviour of L_{eq} and C_{eq} versus (h) is different, hence they are commented separately below.

First, it is observed that for a given value of L_{eq}, a much higher Q_{eq} is realised for greater (h). The 'price to pay' is a slightly greater length for a given inductance value. For instance, if an inductance value of 200 pH is considered, its length is equal to 140 μm for $h = 1$ μm, as compared to 163 μm for $h = 2.5$ μm. The impact of the floating shield position is moderated by the fact that the flux of the magnetic field is practically unmodified with or without the floating shield. The length difference for a given inductance value comes only from the modification of the propagation speed according to the value of (h).

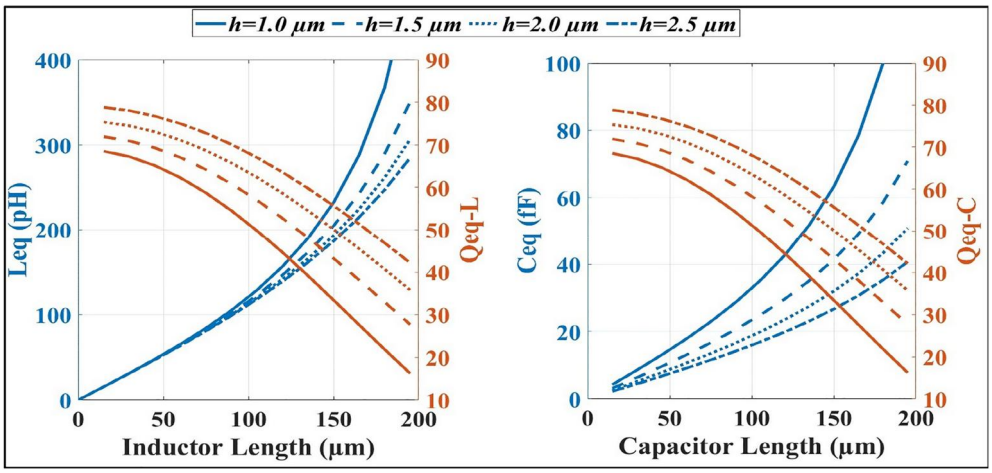

FIGURE 5 Study of shield position on the performance of the S-CPS based quasi-lumped devices at 60 GHz, for $D = 60$ µm, $G = 40$ µm, and $t = 5$ µm. The curves in blue are for the capacitance/inductance values. The curves in orange are for the Q-factor values

Hence, it is interesting to use a high (h) value for the synthesis of inductances, to optimise the Q-factor, and a small (h) value for the synthesis of capacitances, to reduce their size.

As an overall conclusion, while considering the design constraint, the targeted components values (C_{eq} and L_{eq}) can be synthesised in various configuration taking advantage of the flexibility offered by the S-CPS structure. Also, some trade-offs appear between Q-factor and size. In the next section, the performance of L_{eq} and C_{eq} synthesised with S-CPS is compared to that of components available in the process design kit (PDK).

2.4 | S-CPS based capacitance and inductance versus their conventional counterparts available in the PDK

Before addressing the resonators design in the next section, a practical case is highlighted in this section with the comparison of the proposed components with their conventional counterparts implemented on the same technology. For this comparison, two components synthesised with S-CPS, namely a capacitance C_{r1} equal to 24 fF and an inductance L_{r1} equal to 84 pH, respectively, were considered since they will be used in the forthcoming resonators design. Figure 6a shows the performance comparison of the capacitance (C_{r1}) with a MOM capacitance having the same value and being dedicated to RF applications. The latter is provided in the PDK. Figure 6b shows the comparison of the inductance (L_{r1}) with a RF purpose spiral inductance also provided in the PDK. The dimensions of (C_{r1}) and (L_{r1}) are given in Table 1. For the S-CPS based capacitance/inductance, we have provided two types of data in Figure 6, namely, (1) those associated to the model of ref.[9, 10], which has been used in the study illustrated in the previous section and (2) the data resulting from the EM simulation.

The first important remark is related to the difference between the S-CPS electrical model and the EM simulation for

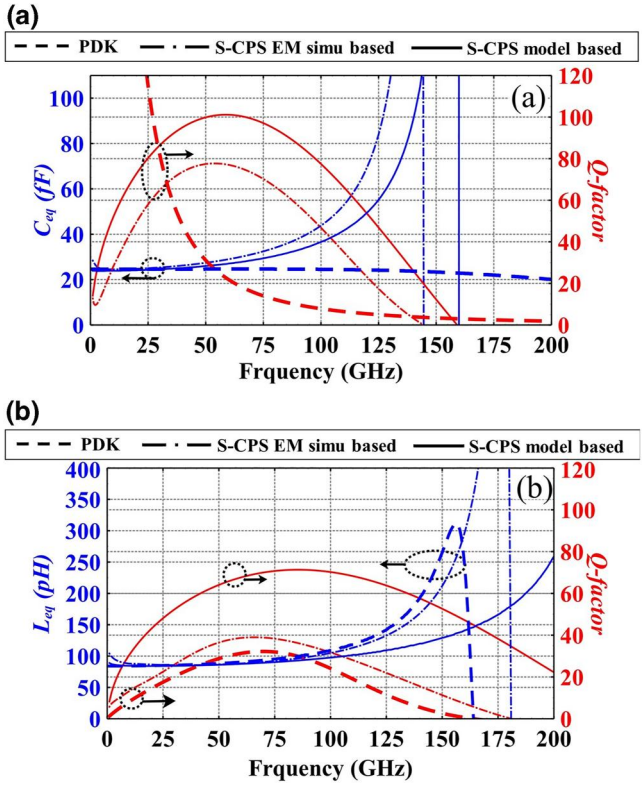

FIGURE 6 Comparison of S-CPS quasi-lumped components with their counterparts available in the PDK. (a) S-CPS capacitance versus MoM capacitance and (b) S-CPS inductance versus spiral inductance

both S-CPS based components. This mismatch was expected because the modelling presented in the previous sections did not consider the discontinuities effect, namely, the open circuit for the capacitance as explained in Figure 2 and Equation (1), and the short circuit for the inductance as depicted in Figure 3 and Equation (11). These discontinuities being taken into account in the EM simulation, they lead to more losses, thus

TABLE 1 Dimensions of the designed S-CPS quasi-lumped capacitance and inductor

Device	W	G	l_{S-CPS}	Strip layer	Shield layer	Value	R_S (mΩ)	L_S (pH)	C_p (fF)	R_p (mΩ)
C_{r1}	20	30	120	M8	M6	24 fF	1	1.13	476	300
C_{2-F1}	20	30	156	M8	M6	31 fF				
C_{2-F2}	20	30	108	M8	M6	21 fF				
C_{F2}	20	30	72	M8	M6	14 fF				
L_{r1}	10	40	80	M8M7	M5	84 pH	2	1.31	413	2560
L_{F2}	10	40	24	M8M7	M5	25 pH				

Note: MiMj means that metal layers Mi is stacked till Mj by the maximum density of vias allowed by the technology.

decreasing the Q-factor and adding more parasitic producing shift in the cuff-off frequencies. However, even with this degradation, the S-CPS based capacitance/inductance remain very competitive against their PDK counterpart as it is explained here after. Moreover, as demonstrated in Section 3, these parasitic effects are considered and well predicted by the proposed advanced modelling.

Figure 6a shows that both capacitances have the same value at low frequency, below about 50 GHz, as expected by design. Then the S-CPS capacitance increases very fast up to about 150 GHz. This frequency corresponds to an electrical length equal to 90°, beyond which the open circuit stub presents an inductive behaviour.

In terms of the Q-factor, the one achieved by the S-CPS based capacitance is much higher than the one related to the MOM capacitance above about 30 GHz. The 'price to pay' is the size. The MOM capacitance dimensions are $4.24 \times 5.85\ \mu m^2$ as compared to those of the S-CPS quasi-lumped capacitance having dimensions of $120 \times 70\ \mu m^2$. Hence, MOM capacitances must be clearly preferred when dealing with high-value capacitances (say greater than 100 fF) for biasing purposes, whereas S-CPS capacitances could be very well suited to realise resonators or matching networks for mm-wave applications.

In the same way, Figure 6b shows that both inductances have the same value at low frequency, below about 80 GHz. The same cut-off occurs around 150 GHz.

The Q-factor is improved over a broad frequency range. The S-CPS inductance can operate within wider frequency range since it has higher self-resonance-frequency (RSF) of about 175 GHz. Another important feature is the compact surface occupied by the S-CPS inductance with $80 \times 60\ \mu m^2$ against $110 \times 109\ \mu m^2$ for the conventional inductance provided in the PDK.

Finally, the flexibility of S-CPS based inductance and capacitance can be mentioned again. It has been shown that various geometrical dimensions can be chosen to reach a particular performance. This can be highly appreciated when an advanced technology is used where the technological constraints imposed by strict design rule manuals are stronger.

The next section shows how these quasi-lumped components can be used to carry out compact and flexible resonators.

3 | RESONATORS BASED ON QUASI-LUMPED S-CPS CAPACITANCES AND INDUCTANCES

In this section, a set of resonators is designed using the S-CPS components described in Section 2. Only parallel resonators were considered here since we do not have a solution for the design of series ones without using impedance inverters. Each design is presented through its EM simulation carried out using ANSYS HFSS, an electrical model helping to understand the physics, and measurement results.

All the presented S-parameters measurement results, in this section, were carried out using an Anritsu VectorStar® ME7838A4 VNA to measure from 70 kHz to 145 GHz while the G-band (140–220 GHz) was explored with a R&S ZVA VNA. An off-wafer LRRM calibration was performed to put the reference planes at the GSG pads using a commercial calibration kit. Subsequently, a second-tier on-wafer TRL calibration was carried-out to de-embed the GSG pads and the feeding lines. Two different lengths for Line standard are used to cover the targeted broadband measurement. In fact, the electrical length difference between the Line and Thru standards should ensure a proper reading.

3.1 | S-CPS based capacitance and inductance synthesis

As stated in the introduction the objective of this paper is the design of resonators based on S-CPS quasi-lumped components. Hence, the synthesis of the capacitances and the inductances that were used for this purpose are first presented. By using the four design parameters offered by the S-CPS structure (h, G, l and W), a tradeoff was made between the foreseen capacitance/inductance value, the quality factor and the size. Table 1 summarises the dimensions of the designed S-CPS quasi-lumped capacitances and inductances using the approach described in Section 2.

The presented capacitances/inductances values are the quasi-static ones. The values of the RLCR model associated to each S-CPS are also provided in Table 1. These values are used in the modelling of the resonator presented in the next-subsection.

3.2 | S-CPS based basic resonator

The first targeted demonstrator circuit is a simple short circuited LC parallel resonator (named R_{1SC}) as described in Figure 7a. As observed from its micrograph shown in Figure 7b, the resonator was designed by connecting the capacitance (C_{r1}) in parallel with the inductance (L_{r1}) and fed through a T-junction microstrip line laid-out on metal layer (M8) and having a reference ground plane on metal layer (M1). The length of the vertical transmission line connecting the T-junction to the resonator matters, since it adds a phase shift to the resonator. The longer this transmission line, the lower the resonant frequency will be. However, the price to pay is an increase in size, with the addition of an inefficient microstrip approach in terms of quality factor. Thus in our study this length was reduced to the maximum. The ground plane covers the entire chip surface except the region underneath both S-CPSs. The used stack-up for all components is also given in Table 1. The S-CPS strips were formed by M8 or a stack of M8 and M7; the floating ribbons were formed by M5 or M6.

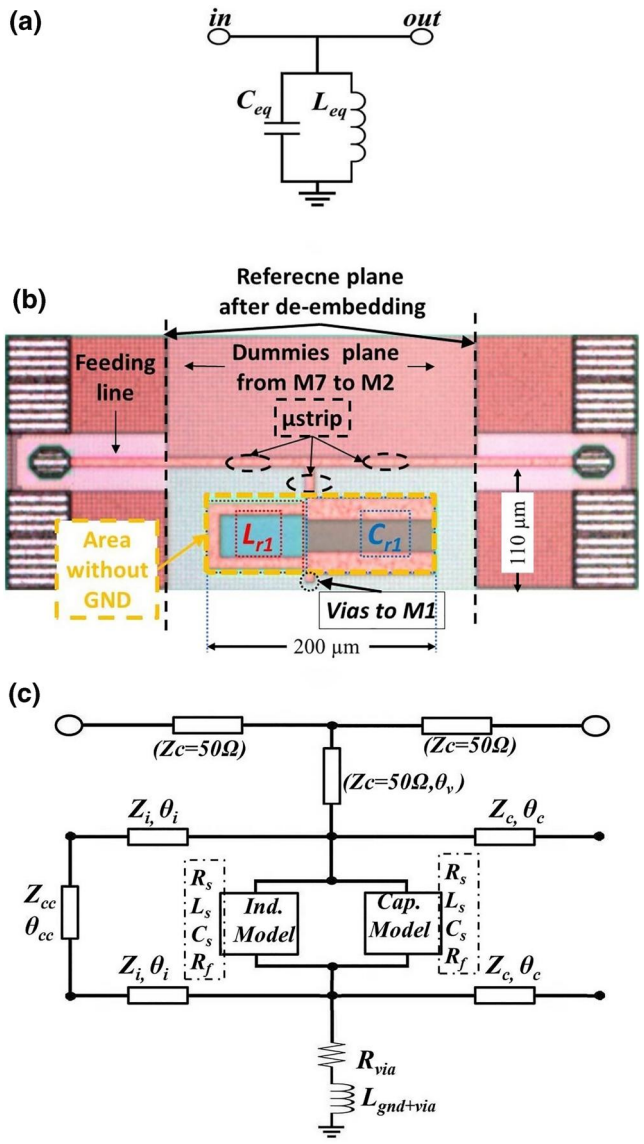

FIGURE 7 Short circuited LC parallel resonator (R_{1SC}). (a) The targeted design, (b) the chip photo, and (c) the electrical model; the S-CPS capacitance/inductance boxes are modelled by the S-CPS electrical model of Figure 1c

In order to keep the S-CPS propagation mode, the bottom strip connecting L_{r1} and C_{r1} is connected to the ground plane ('Vias to M1' as sketched in Figure 7b) through a set of vias. Therefore, the two S-CPSs can behave well as quasi-lumped capacitance and inductance, as predicted by the theoretical study presented in Section 2.

The resonance frequency (f_r) can be calculated with the well-known formula defined in (15) and based on the values given in Table 1. However, Equation (15) gives an approximate result due to the dispersive behaviour of S-CPS based capacitances and inductances, as already discussed in Section 2.

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{15}$$

To understand the physics behind the operation of the LC resonator, the electrical model presented in Figure 7c is proposed. The T-junction was modelled by the Tlines having 50 Ω characteristic impedance and a propagation constant γ. The stack of vias was modelled by a resistor (R_{via}) in series with an inductance ($L_{gnd+via}$), which also models the parasitic return-current path inductance. As for the S-CPS components, each box is replaced by n sections of RLRC electrical circuit of Figure 1c defined by its elements (R_S, L_S, R_f, C_S) whose values are provided in Table 1. Each section is related to S-CPS length of SS/2 + SL + SS/2, which corresponds to one ribbon with length (SL) trapped between two half-gaps (SS/2). Therefore, the number of sections is calculated as follows:

$$n = l_{S-CPS}/(SS + SL) \tag{16}$$

where l_{S-CPS} is the S-CPS length, given in Table 1.

Besides the S-CPS propagation mode that is modelled by the RLRC electrical circuit in Figure 1c, a degenerated microstrip mode (DMM) is created around the S-CPS components due to the proximity of the ground plane on (M1). Looking from the input of L_{r1} and C_{r1}, below the microstrip junction, the DMM propagates through two stubs, one formed by the top strip forming C_{r1}, and the second formed by the strip forming L_{r1} in cascade with the bottom strip forming C_{r1}. Three different characteristic impedances were considered for the DMM. The DMM corresponding to C_{r1}/L_{r1} strips leads to Z_c/Z_i characteristic impedances, and the DMM corresponding to the S-CPS short to form L_{r1} leads to Z_{cc} characteristic impedance, respectively.

Table 2 summarises the values of the electrical model elements, where R_{via} and $L_{gnd+via}$ were extracted using ANSYS Maxwell 3D software and the various characteristic impedances as well as the electrical lengths were estimated using EM simulation.

Figure 8a illustrates the measured S-parameters of the resonator R_{1SC} compared to those predicted with EM simulation

TABLE 2 Values of the model associated to resonator R_{1SC}

R_{via}	$L_{via+gnd}$	Z_i	Z_c	Z_{cc}
0.1 Ω	26 pH	61 Ω	59 Ω	105 Ω
θ_v	5° @ 70 GHz			
θ_i	4.8° @ 70 GHz			
θ_{cc}	4.8° @ 70 GHz			
θ_c	22° @ 70 GHz			

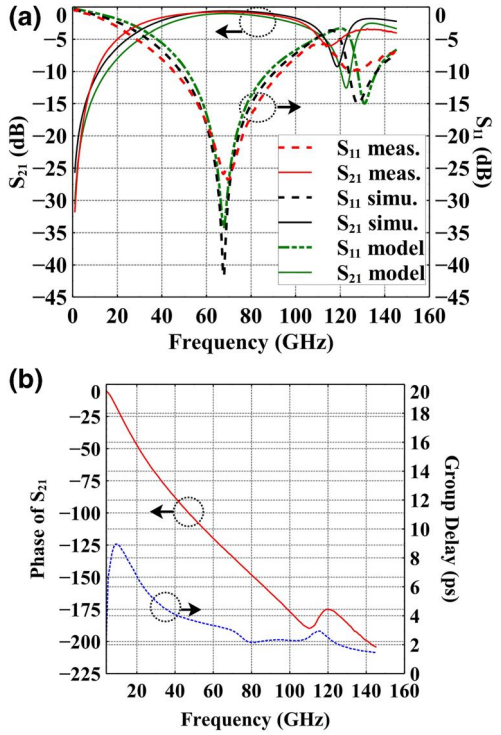

FIGURE 8 (a) S-parameters of the resonator (R_{1SC}). Measurement, EM simulation and model responses. (b) Measured phase and group delay

and the electrical model. It can be noted that the measured S_{11} and S_{21} were well predicted from both the EM simulation and the proposed model up to 100 GHz. Above 100 GHz, disagreement appears. However, the resonance frequency of 70 GHz was well predicted.

It could be noted on the results presented in this article, the difference between the EM simulation and the measurement, especially for frequencies was above approximately 100 GHz. The most acceptable hypothesis to justify this mismatch is the presence of the dummies made compulsory to fulfil the metal density rules for the used technology. These dummies could not be considered during the simulations, otherwise, colossal means of calculation will be required. Nevertheless, we believe that the agreement between simulations and measurements is sufficient to validate the concept of the resonators proposed in this manuscript. For future designs, however, it will be necessary to address the problem of dummies' parasitics by developing complete models taking into account dummies influence.

Regardless of the registered response shift, a good electrical performance of the designed resonator is noted, with 0.7 dB of measured insertion loss (IL) against 0.6 dB in EM simulation at the central frequency, and good impedance matching with a measured return loss (RL) was better than 25 dB while it was 40 dB in EM simulation. In addition, Figure 8b shows the phase as well as the group delay of the resonator where it could be noted the relatively flat group delay within the band of interest between 30 and 100 GHz. Such flatness is required for filter in order to avoid any distortion of the filtered signal. Finally, with a delay of around 4 ps, very limited latency could be added by this resonator if used within receiver chain.

The presented resonator could be designed for lower frequencies, for example, 28 GHz, considering the fact that their size is still very moderate. The insertion loss would be slightly higher, because the quality factor of S-CPS increases with frequency [9], which is the case with all types of transmission lines, because the propagation constant increases faster than the attenuation constant with frequency. As an indication, for a resonator having a FBW (Fractional Bandwidth) of 100%, the insertion loss obtained in simulation would be 1.2 dB at 28 GHz, compared with 0.6 dB for the resonators developed in this article having a FBW of 120% around 70 GHz.

3.3 | Other topologies based on S-CPS

To further demonstrate the flexibility of the proposed S-CPS quasi-lumped capacitance and inductance, two other circuits were designed based on the components of Table 1. Their chip photos and responses are illustrated in Figures 9 and 10, respectively.

Both circuits derive from the same topology as the resonator (R_{1SC}) presented in the previous sub-section. As sketched in Figure 9a, the first circuit, named F_{1SC}, was obtained by adding to the resonator (R_{1SC}) a short circuited capacitance (C_{2-F1} as named in Table 1) placed on the upper side of the feeding line. The aim was to demonstrate that the resonator response could be adjusted by adding a quasi-lumped capacitance in parallel to the initial resonator (R_{1SC}).

The second circuit, (CF_{2S}), is based on the same topology as (F_{1SC}), but with smaller capacitance and inductance values. The aim was to show that the resonance frequency can be easily adjusted, and that the proposed concept is still valid at higher frequencies of the mm-wave spectrum.

The resulting response of the resonators (F_{1SC}) and (F_{2SC}) is depicted in Figure 10a,b, respectively. A good agreement is obtained between measurement and EM simulation results.

In comparison to the response of (R_{1SC}), the first resonance frequency f_r of (F_{1SC}) is shifted to a lower frequency, that is, 50 GHz as compared to 70 GHz for (R_{1SC}), due to the increase of the equivalent capacitance as it can be estimated with (15). Also, the shift in the response of (F_{2SC}) is due to the same reason. In addition, the new bandwidth of both resonators is different from the one associated to (R_{1SC}) due to the modification of the ratio C_{eq}/L_{eq}, which permits to control the

bandwidth of the resonator. The insertion loss is 1 dB in measurements against 0.95 dB in EM simulation.

Regarding the resonator (F_{2SC}), the first resonance frequency f_r is shifted to 80 GHz, as expected by the size reduction. Two transmission zeros are observed at DC and 180 GHz. The insertion loss is 1.05 dB.

Note that the responses of resonators (F_{1SC}) and (F_{2SC}) are much more interesting than the response of the initial resonator (R_{1SC}), since they exhibit two transmission zeros, at DC and about the double of the first resonance frequency f_r. This behaviour can be very interesting for the synthesis of filters based on the proposed resonators.

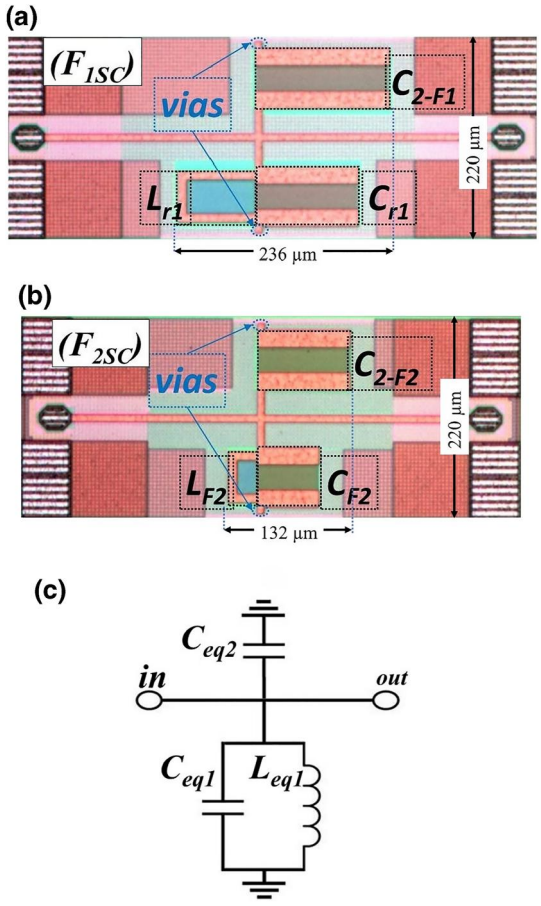

FIGURE 9 Resonator topologies based on (R_{1SC}). (a) Resonator (F_{1SC}), (b) Resonator (F_{2SC}), and (c) circuit diagram for both resonator

3.4 | Importance of 'Vias to M1' vias

In this section it is shown how the absence of short-circuit ('Vias to M1' in Figure 7) totally changes the response of the resonators, which in that case is only based on the degenerated microstrip mode.

The chip photo of the proposed resonator, named (R_1), is depicted in Figure 11a. It is exactly the same circuit as resonator (R_{1SC}), with the same dimensions. The only difference here is the cancelation of the vias connecting the bottom S-CPS strip to the ground plane.

The absence of vias in the resonator (R_{1SC}) totally changes its operation. Without vias, the S-CPS mode is no longer excited, since the electric field does not flow between the two strips of the S-CPS. In turn the DMM is still excited. The response of the resonator (R_1) is very similar to the well-know DBR [11, 15], with two transmission zeros appearing on each side of the passband due to two open-ended stubs of lengths l_1 and l_2, respectively. However, from an electromagnetic point of view its operation is more complicated because there is a strong coupling between the strips of the resonator, which is reinforced by the presence of the shielding layer. Therefore, it is not straightforward to calculate the frequency of the transmission zeros. Also this is beyond the scope of this article which focuses on the use of S-CPS mode.

Figure 11b shows the measured and EM-simulated S-parameters of (R_1). The agreement between simulated and measured S-parameters is acceptable. As expected, the response is that of a DBR with a resonance frequency at 95 GHz, with 1.56 dB of IL, surrounded by two transmission zeros, the first one occurring at 77.8 GHz and the second at 135 GHz, respectively.

Hence the 'Vias to M1' are mandatory in order to get the quasi-lumped S-CPS components behaviour.

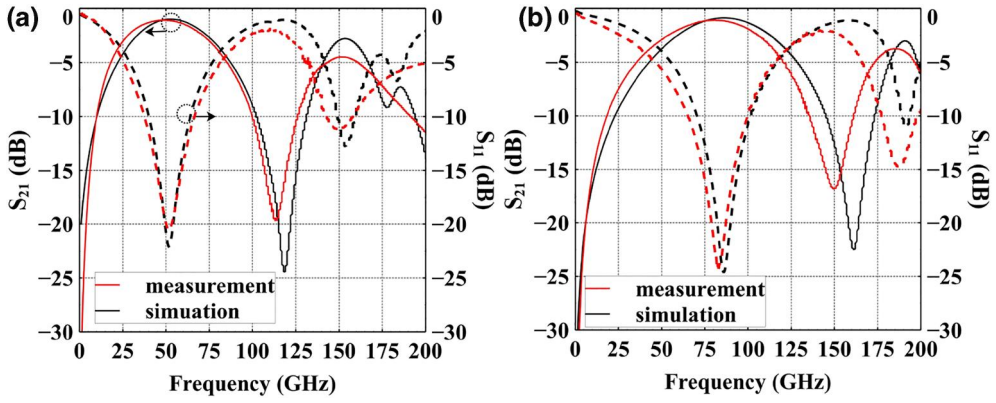

FIGURE 10 The S-parameters performance of the designed resonators. (a) Resonator (F_{1SC}) and (b) Resonator (F_{2SC})

The response shown in Figure 11b could also have an interest, however, the size reduction is much lower when using DMM, the resonance frequency being equal to 95 GHz with DMM as compared to less than 70 GHz (see Figure 8) with S-CPS quasi-lumped components, for the same footprint.

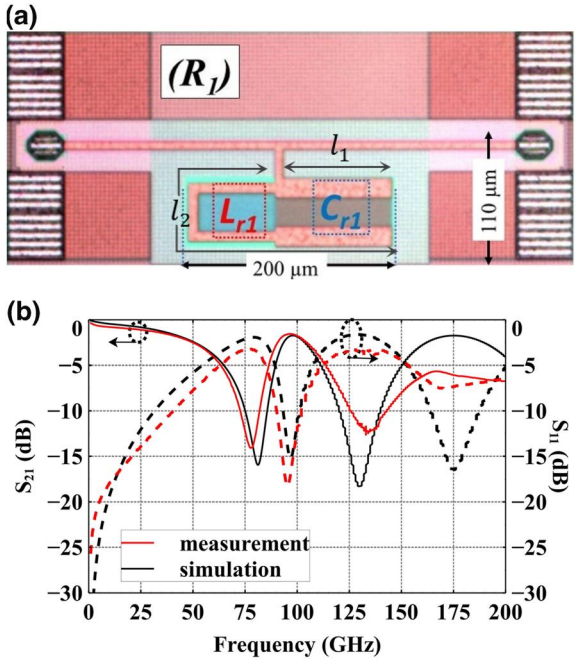

FIGURE 11 Resonator (R_1). (a) Chip photo. (b) Comparison of measured S-parameters with the EM simulation

TABLE 3 Resonator R_{1SC} insertion loss versus BEOL

h (µm)	t (µm)	$S_{21\text{-dB}}@f_0$	$S_{11\text{-dB}}@f_0$	FBW (%)
2.5	1	0.7	−29	117
2.5	5.4	0.6	−28	103.7
1	5.4	0.63	−33	112.3

3.5 | Impact of the BEOL on S-CPS based resonator insertion loss

In this subsection, we show some results concerning the impact of the BEOL on the S-CPS based resonator. The study was carried out on the resonator (R_{1SC}). The two most important dimensions were considered, namely t and h, with two values for each of these two dimensions, that is 1 µm and 2.5 µm for h and and 1 µm 5.4 µm for t. For each case the quasi-lumped inductor and capacitor were resized to get almost the same resonance frequency as the initial design of (R_{1SC}). Table 3 summarises the insertion loss obtained from simulation.

It can be noted that the BEOL has a small impact on the insertion loss. Such a study would be even more interesting if BEOLs of different technologies were considered. Such a study is, however, complicated because it is necessary to have access to many technologies.

4 | COMPARISON TO THE STATE OF THE ART

In this section, a summary of the presented designs performance is provided in Table 4. Also, in order to compare our contributions to similar works reported in the current state-of-the-art, a comparison with resonators designed in CMOS/BiCMOS technologies at mm-waves is carried out in Table 4. Although the mentioned references concern bandpass filter design, the circuit selected for the comparison is always a simple resonator or a first order filter. We have introduced as figure of merit the unloaded quality factor (Q_u), which can be derived from the formulation of the scattering parameter S_{21} defined as follow,

$$S_{21} = 20 \cdot \mathrm{Log}\left(1 + \frac{1}{\mathrm{FBW} \cdot Q_u}\right) \tag{17}$$

It is pertinent to note that the unloaded quality factor Q_u is different from the Q-factor stated in the previous sections. The former is used as a figure of merit for resonators and filters in

TABLE 4 Performance of the designed resonators

Ref.	f_r (GHz)	Tech.	FBW (%)	IL (dB)	Q_u	Size (mm^2)
[11]	60	0.13 µm BiCMOS	18	2.6	18	0.1119
[16]	60	0.35 µm CMOS	115	1.4	4	0.0471
[17]	40	0.13 µm BiCMOS	20	1.7	23	0.0115
[18]	59.4	0.13 µm BiCMOS	45	1.7	10	0.039
[19]	61.2	0.25 µm BiCMOS	11	5	11	0.32
[20]	57	0.13 µm BiCMOS	35	2.5	8	0.0243
R_{1SC}	70	55 nm BiCMOS	119	0.77	9	0.0223
F_{1SC}	50	55 nm BiCMOS	120	1.08	6	0.0519
F_{2SC}	80	55 nm BiCMOS	91	1.07	8	0.0291

Note: All the presented data are related to the resonators or first order filters presented in each reference.

order to assess the couple insertion loss (IL) and fractional bandwidth, whereas the latter is used to evaluate the electrical performance of simple passive devices such as inductances, capacitances or transmission lines. Thus, correlating those two parameters is not straightforward. Nonetheless, the Q_u is used in this section as a tentative to compare the proposed resonators with other works reported in the literature, knowing that comparing integrated passive circuits implemented on different BEOL is always subject to caution because the thicknesses of the metals are different, as well as the total thickness of the BEOLs.

The comparison is not easy since the resonators do not exhibit the same fractional bandwidth (FBW). Hence comparing the insertion loss (IL) is not fair. However, it can be seen that the size of the proposed resonators is comparable to the size of the ones published in the literature.

5 | CONCLUSION

In this paper, the capabilities of the S-CPS topology were demonstrated for the design of competitive mm-wave resonators. Firstly, the basic theory describing how S-CPS can be used to design high Q-factor quasi-lumped capacitances and inductances was briefly developed. In particular, it was exposed how the flexibility of the S-CPS topology could lead to simple components design. Then mm-wave resonators were designed based on the S-CPS based capacitances and inductances. The proposed resonators were demonstrated around 50–80 GHz; however, much higher resonance frequencies could be easily achieved. The next step in terms of perspective would be to develop filters by a conventional synthesis method including impedance transformers between resonators.

CONFLICT OF INTEREST

None.

DATA AVAILABILITY STATEMENT

Data sharing is not applicable to this article as no datasets were generated or analysed during the current study.

ORCID

Abdelhalim A. Saadi https://orcid.org/0000-0003-4092-1384
Philippe Ferrari https://orcid.org/0000-0002-2803-4830

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How to cite this article: Saadi, A.A., et al.: Innovative millimetre-wave resonators based on slow-wave coplanar stripline components. IET Microw. Antennas Propag. 16(7), 477–488 (2022). https://doi.org/10.1049/mia2.12260