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## 2 **Single Event Effects on the RD53B Pixel Chip Digital Logic** 3 **and On-chip CDR**

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14 **ABSTRACT:** The RD53B chip for HL-LHC upgrades of ATLAS and CMS pixel detectors needs to  
15 provide reliable operation in a radiation hostile environment with inevitable Single Event Effects.  
16 To answer the challenge, substantial efforts are made to protect and evaluate the critical parts of  
17 digital logic with different TMR schemes and to characterize the on-chip CDR. Cross-section for  
18 each TMR scheme and its effective SEE sensitivity are measured in several SEE campaigns. The  
19 on-chip CDR is characterized by measuring the SEE-induced phase shifts of its output clocks and  
20 their implication on the high-speed link stability.

21 **KEYWORDS:** Particle detectors, Radiation-hard detectors

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## 32 1 Introduction

33 RD53 is a common design framework of final pixel readout chips for the ATLAS and CMS phase 2  
34 upgrades developed in 65 nm CMOS technology. This framework aims at providing a fault tolerant  
35 system which meets stringent requirements of the HL-LHC environment and provides reliable  
36 functionality in its extreme radiation field. Besides having tolerance to immense total ionizing dose  
37 of 1 Grad, this field demands high redundancy to Single Event Effects (SEEs). Critical parts of its  
38 digital design are protected with different mitigation schemes to ensure reliable operation. Several  
39 heavy-ions and proton beam tests were performed to measure the efficiency of these protection  
40 techniques and to estimate a soft error rate in the final detector. During beam testing it has been  
41 seen that Single Event Transients (SET) can impact high-speed data link stability by causing several  
42  $\mu$ s long dropouts which motivated more detailed studies. The on-chip Clock Data Recovery (CDR)  
43 circuit was characterized by capturing heavy-ion-induced error signatures in its high-speed clock  
44 which drives the output data link.

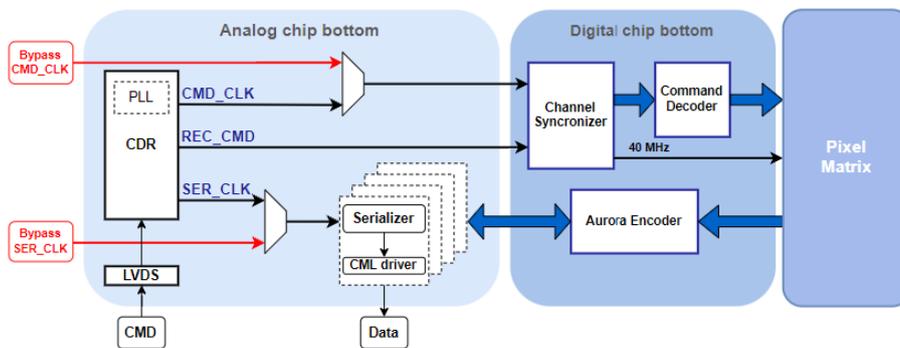
## 45 2 RD53B design for soft error mitigation

46 The RD53B chip [1] is the pre-production chip which will be followed by the final RD53C production  
47 chip with submission planned in 2022. The pixel chips for ATLAS and CMS are two instances of  
48 a common design with different analog front-ends and pixel matrix sizes. However, all SEE results  
49 are valid for both chips since they have the same digital design and analog blocks in the periphery  
50 including the on-chip CDR. Design robustness for soft error mitigation depends on the target level  
51 of reliability on one side and acceptable power and area overheads on the other. RD53 objectives are  
52 minimization of the upset rate for critical information and signals, and the capability of immediate

53 self-recovering in case of critical data corruption. This implies that the configuration memory, state  
 54 machines, critical event data, look-up tables are all SEE robust. The on-chip CDR is SET hardened  
 55 with triplicated clock divider, a bang-bang phase detector and an optimized voltage-controlled  
 56 oscillator (VCO) [2]. As a means of having a small pixel size and staying within power dissipation  
 57 constraints, the chip has different protection schemes for its pixel and global configuration memory  
 58 which prevents soft errors at two different levels of efficiency [3]. In case chip operation is critically  
 59 affected by SEEs, a Clear command is implemented for fast clear of data buffers and state machines.

### 60 3 SEE sensitivity of the Aurora serialized data

61 During beam campaigns, the 1.28 Gbit/s readout links showed susceptibility to SEEs with temporary  
 62 loss of synchronization with the DAQ receiver causing loss of multiple events. However, this  
 63 behavior is not observed if the high-frequency clock driving the data link output is provided  
 64 externally bypassing the on-chip CDR block.



**Figure 1:** Simplified data flow with the blocks for clock recovery and encoded data serialization.

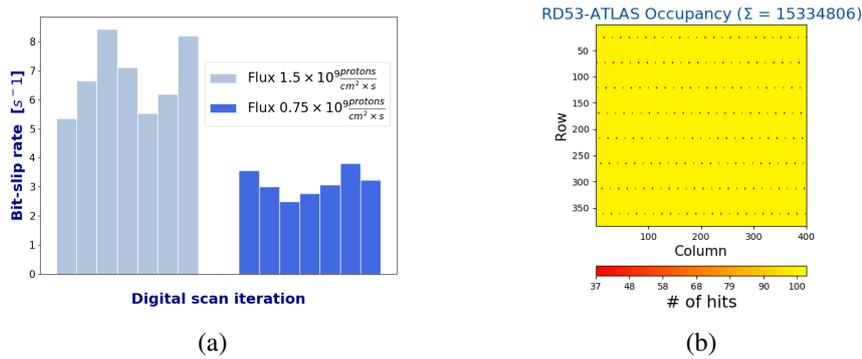
#### 65 3.1 Chip default operation mode and CDR-Bypass

66 Figure 1 shows clock generation inside the analog chip bottom and a simplified data flow. During  
 67 chip default operation mode, the CDR block recovers 160 MHz reference clock from the received  
 68 160 Mbit/s input command stream and generates a 1.28 GHz clock. This high-frequency clock  
 69 drives up to 4 serializers, each providing a 1.28 Gbit/s output data stream on a corresponding data  
 70 lane via a CML output driver. While characterizing performance of the pixel digital logic, when  
 71 exposed to particle beam, it is beneficial to decouple its soft error rate from the CDR SET sensitivity.  
 72 Thus, the chip features the possibility of enabling a so-called CDR-Bypass mode in which both  
 73 reference and serializer clocks are provided externally by the DAQ system.

#### 74 3.2 Hit loss induced by the SET sensitivity of the high-speed data link

75 Performance of the digital chain for hit processing is evaluated by injecting digital hit pulses  
 76 while irradiating device at a given flux and recording pixel matrix response. Hit data is acquired  
 77 through the 1.28 Gbit/s serial link via Aurora Xilinx IP receiver on a Kintex7-based DAQ [4] board.  
 78 Measurements with both heavy-ions and protons show that if the chip operates in the CDR-Bypass

79 modes, its data stream has high signal integrity with no stability issues induced by SETs. However,  
 80 the same test sequence with on-chip CDR enabled, leads to loss of the synchronization state with  
 81 the DAQ receiver due to clock cycle slipping. To measure hit loss caused by the SET sensitivity  
 82 of the serializer clock, receiver volatility to phase shifts of the input stream is eliminated. This  
 83 is achieved by disabling its sync state machine, thus all received bit-slipped headers are ignored  
 84 without instantiating Aurora lane re-synchronization.



**Figure 2:** (a) Bit-slip error rate per digital injection. (b) Hit loss in the occupancy map caused by data bit-slips.

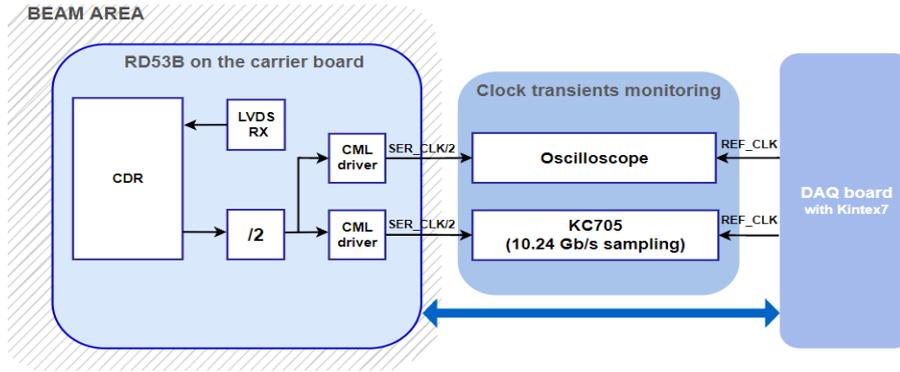
85 In figure 2a, data bit-slip rate induced by 480 MeV protons is shown for multiple iterations of  
 86 110 s long digital injection. If the proton beam is run at the at flux of  $1.5 \times 10^9 \frac{\text{protons}}{\text{cm}^2 \times \text{s}}$ , the average  
 87 bit-slip rate is  $3.13 \text{ s}^{-1}$ . With half the flux density, the bit-slip rate is  $6.78 \text{ s}^{-1}$ . An example of  
 88 an occupancy map when the digital injection is repeated 100 times per pixel is shown in figure 2b  
 89 (RD53-ATLAS has  $384 \times 400$  pixels). In the 480 MeV proton beam environment, hit loss induced  
 90 by the data bit-slips can be up to 0.2%. This motivated further studies to determine the exact  
 91 signature shape and duration of induced transients in the clock signal.

## 92 4 Characterization of heavy-ion-induced transients in the 1.28 GHz clock

93 To address the problem of high-speed data link dropouts in heavy-ion and proton beam environments,  
 94 transients in the clock signal driving this output are characterized. The experiment was carried  
 95 out at the GANIL irradiation facility in France, using a Xenon beam with a LET of  $27 \frac{\text{MeV} \times \text{cm}^2}{\text{mg}}$ .  
 96 Irradiation was done in the air at room temperature using the setup depicted in figure 3.

### 97 4.1 Setup with the 10.24 Gb/s signal oversampling

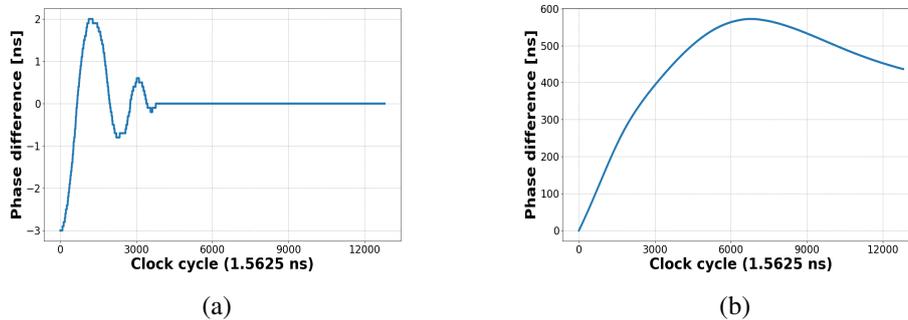
98 The high-frequency on-chip CDR output clock used for serialization of Aurora data is first divided  
 99 by two inside the chip analog bottom (SER\_CLK/2) and routed to the CML output driver resulting in  
 100 a 640 MHz frequency clock signal available for monitoring. Monitoring is done on an oscilloscope  
 101 which triggers which triggers in case of a phase shift larger than 390.625 ps with respect to  
 102 reference clock. The reference clock itself is provided by the DAQ board located outside the  
 103 beam area. To acquire better timing resolution, an FPGA-based setup was developed using the  
 104 KC705 Xilinx Evaluation Board to monitor the signal in parallel. This system is using a Xilinx



**Figure 3:** Setup for measuring clock SET sensitivity.

105 Gigabit Transceiver (GTX) [5] to oversample the clock under test with a 10.24 Gbit/s sampling rate,  
 106 providing 64 bits deserialized clock data at a 160 MHz word frequency. To enable oversampling  
 107 inside the transceiver, it is necessary to lock its internal CDR to the reference clock. The best  
 108 sampling performance is obtained by choosing Low Power Mode (LPM) equalizer and disabling its  
 109 auto-adaptive filtering. This system incorporates a triggering mechanism on the clock pulse width  
 110 deviation bigger than 97.65 ps, which is the resolution of the circuit.

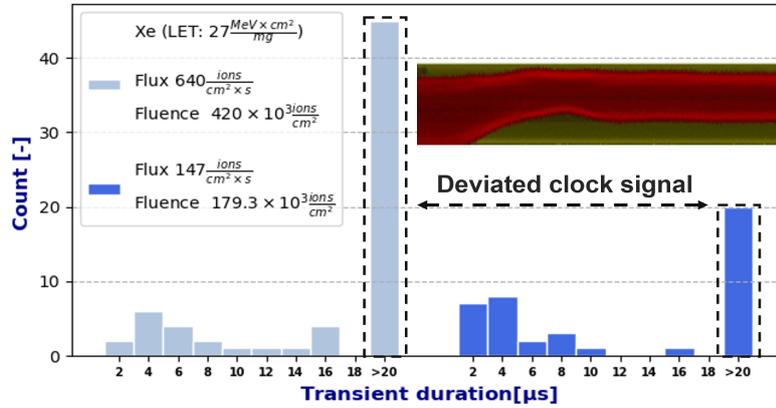
## 111 4.2 Results



**Figure 4:** Accumulated phase difference of the SER\_CLK/2's rising edge from its ideal position measured over 12800 clock cycles. (a) Example of a transient with 2 ns phase shift and duration of less than 18  $\mu$ s. (b) Example of a transient with large accumulated phase shift.

112 Signatures induced by the Xe beam can be grouped into two categories. In the first one, the  
 113 clock signal has transient phase variation but other signal parameters, like frequency and amplitude,  
 114 are transient free. An example event captured by the FPGA over-sampling is shown in figure 4a.  
 115 All transients in this group have a duration of less than 18  $\mu$ s and a clock phase shift of up to 5 ns.  
 116 However, the second group of events shows that ion strikes can cause clock amplitude and biasing  
 117 deviation. This further leads to a cumulative phase shift in the range from 50 to 700 clock cycles,  
 118 as seen in figure 4b. All events in this group are longer than 20  $\mu$ s which is the duration of saved  
 119 waveforms. Event duration distribution is shown in figure 5 for two values of Xe beam flux and

120 reached fluence. It can be concluded that transients longer than 20  $\mu\text{s}$ , which are also characterized  
 121 by the large phase shift and deviated signal, corresponds to a clear peak of the given distribution.



**Figure 5:** Distribution of transient duration at two different values of Xe flux. The red signal is an example of a deviated 640 MHz clock under test.

## 122 5 Conclusion

123 By evaluating the RD53B design robustness against SEEs, it has been observed that heavy-ions  
 124 and protons can induce high-speed data link dropouts limiting the reliability of the system. The  
 125 susceptibility of the 1.28 GHz clock driving the data output to transient faults is successfully  
 126 estimated by capturing its phase shifts with an oscilloscope and the proposed high-speed signal  
 127 sampling inside the FPGA. Two groups of different SET signatures were detected. In cases where  
 128 driver biasing and clock frequency are not affected, the phase shift is up to a few ns long. However,  
 129 ions can cause clock signal deviation and lead to phase shifts of several hundred clock cycles. These  
 130 shifts further lead to data link dropout and result in hit losses. The different nature of these events  
 131 indicates that except for the CDR block itself, its biasing circuit may also be SET sensitive. Further  
 132 assessment of the chip's biasing chain is being carried out with two-photon absorption pulsed laser  
 133 testing. This study has already pinpointed sensitivity in the chip's bandgap as the cause of the long  
 134 upsets. When finalized, the results will be documented in a separate publication.

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