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► **To cite this version:**

Rodrigo Iga Jadue, Sylvain Engels, Laurent Fesquet. A Novel Continuous TDC Measurement Technique. 27th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 2021), Sep 2021, Portland, United States. hal-03662324

**HAL Id: hal-03662324**

**<https://hal.science/hal-03662324v1>**

Submitted on 9 May 2022

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# A Novel Continuous TDC Measurement Technique

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**Abstract**— This paper presents a novel technique implementing a continuous Time-to-Digital Converter (TDC) measurement circuit that has been used for designing an Event-Based ADC (EB-ADC) implementing a LCSS (Level Crossing Sample Scheme). In the case presented in this brief, the EB-ADC has been connected to a bundled-data asynchronous digital ASK demodulation algorithm module, and has been sent to fabrication using FDSOI 28nm STMicroelectronics technology. For the ASK demodulation implementation purpose, only two crossing levels have been defined. Then, the EB-ADC is composed only by two comparators, one for each level. These comparators were characterized through an electrical simulation and then modeled in SystemVerilog in order to be integrated in a fully digital simulation. Thus, the TDC, its internal elements and the demodulation module has been synthesized and placed and routed, for obtaining the final layout. A post-layout simulation has been executed to validate the whole design and hence the continuous TDC measurement between each consecutive input request events. The obtained demodulation performance of the system has been a BER =  $3.33 \cdot 10^{-7}$  for a bitrate of 6.78 Mbps and SNR greater than 16 dB.

**Keywords**—Amplitude shift keying (ASK) demodulator, nonuniform sampling scheme, asynchronous logic, level-crossing analog-to-digital converters, time-to-digital converter (TDC).

## I. INTRODUCTION

Nowadays, smart sensor, IoT cards and all sort of standalone communication devices require very low power consumption implementation solutions, permitting that each battery charge can last for several years. One of the known alternatives for reducing the power consumption is the usage of asynchronous circuits, for taking profit of long idle or sleep periods, one of the main characteristics of these kind of devices.

For implementing a system taking profit of these idle times, a Level Crossing Sample Scheme (LCSS) can be used [1][2], to generate input events of the system only when new activity occurs. In this case, a new event will be generated on each level crossing, and a measurement of the time elapsed between two consecutive level crossing events must be done. This solution is called Event-Based Analog-to-Digital

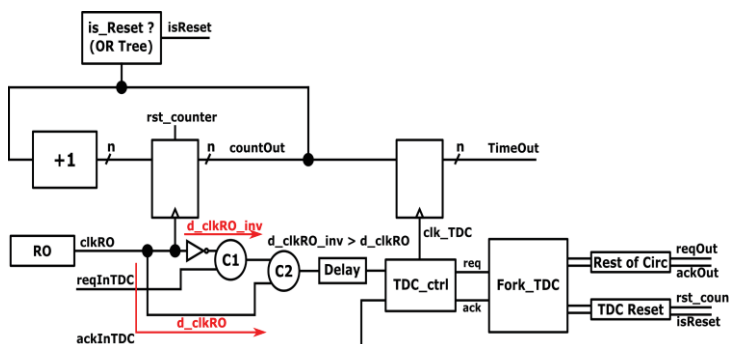


Figure 1: Diagram of the TDC solution.

Converter (EB-ADC). For designing the latter, two main blocks are necessary, the first allowing to detect the level crossings, for example a comparator connected to a Digital-to-Analog converter (DAC) with some already programmed levels in a memory, and the second block permitting to measure the time elapsed between two adjacent events, for example a Time-to-Digital Converter (TDC). The TDC designs found in literature usually measures the time between a start and a stop signal or the time equivalent to a pulse width. This brief presents a continuous time measurement TDC solution, allowing to measure the time between two successive request signal arrival (events) and ensuring the proper reset of the current TDC measurement before accepting a new input request.

## II. IMPLEMENTATION

The continuous measurement TDC circuit proposed in this work is presented in Figure 1. This TDC uses a Ring Oscillator (or a high-speed clock) connected to a n-bits counter. This counter is reset on each new input event (reqInTDC), and its current value is saved in the output n-bits register (TimeOut). For ensuring the correct registration of the output time value, a synchronization method has been implemented, using two C-elements in series (C1 and C2), to transmit a rising-edge of the reqInTDC signal, into the delay module, only on a rising edge of the clkRO signal, and consequently a falling-edge of reqInTDC only on a falling-edge of clkRO. This assertion will be only valid if the delay of the path through the C-elements, called  $d\_clkRO\_inv$  is larger than the delay of the path  $d\_clkRO$ . The latter configuration simplifies and ensures the timing assumption that the clkRO period must be larger than the added delays of C1, C2, the delay line, TDC\_ctrl and its interconnections.

The reset mechanism, presented in Figure 2, is the main contribution of this brief. As described before, it commands the reset of the TDC counter only after assuring the correct

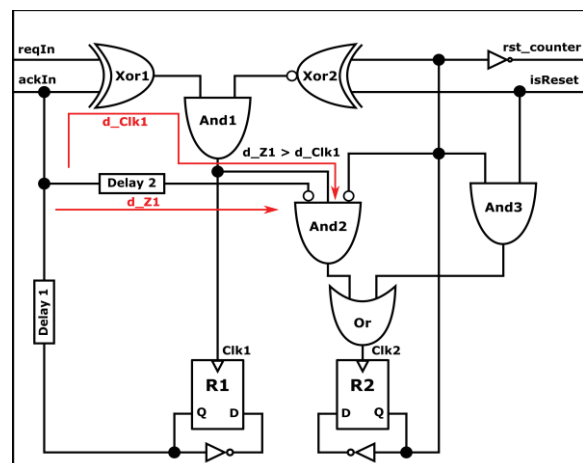


Figure 2: TDC Reset block implementation.

registration of the current time, and also blocking new event arrivals until the TDC counter was correctly reset. This method mixes a 4-phase WCHB protocol in the handshake signals input ( $reqIn$  and  $ackIn$ ) and a 2-phase handshake CLICK register controller [1] modified and shaped for the reset process. This solution uses the phase-decoupled version presented in [3]. The latter has been modified to activate the  $reset\_counter$  signal after the input request arrives, and then ensure that the reset has already been executed, verified by an  $or\_tree$  module, before switching back the input handshake signals to its initial state. Two timing assumptions must be considered for the right operation of this circuit. The first one is when the register  $R1$  returns to its initial state, value 0, we must assure that the propagation of the new initial state of  $R1$  through the  $Xor1$  gate ( $d\_Clk1$ ) is shorter than its propagation through  $Delay2$  ( $d\_Z1$ ) for avoid generating an erroneous rising edge in  $Clk2$ . The second timing assumption to consider, using  $Delay1$  is when a new input request arrives, then the rising edge of  $clk1$  produces a switching state in  $R1$ , so if the environment response is quicker than the switching state of  $R2$ , it will generate a wrong rising edge in  $Clk1$ .

### III. TESTCHIP AND RESULTS

This continuous measurement TDC implementation has been tested in a real digital event-based ASK demodulation circuit implementation, depicted in Figure 3. For this purpose, a level crossing detector circuit has been implemented using two comparators and two reference voltages, one near  $gnd$  (the reference of the circuit) and the other near  $vdd$  (the supply voltage of the circuit). The latter has been connected to the continuous measurement TDC to form the EB-ADC. The latter will generate new request events on each level crossing, and the TDC will provide the time measurement between two consecutive events. These measurements are used by a digital demodulation algorithm for obtaining the demodulated output symbols of the system. The resulting symbols are outputted to the test environment using an asynchronous serial communication.

The presented circuit has been conceived in FDSOI 28 nm from STMicroelectronics and delivered for fabrication. Nevertheless, it has not been received back yet. So, for confirming that the designed TDC solutions works in a real circuit implementation, a post-layout simulation of our proposal is presented in Figure 4. These simulations have been executed in a SystemVerilog (SV) ecosystem where the comparators have been characterized through electrical simulations and modelled in SV to be incorporated in a full digital simulation. The RF input signal and its noise model, expressed in Signal-to-Noise Ratio (SNR), has been modelled by replicating the  $awgn$  function of python's  $commpy$  library [4]. The input code of the system is randomly generated in 32-

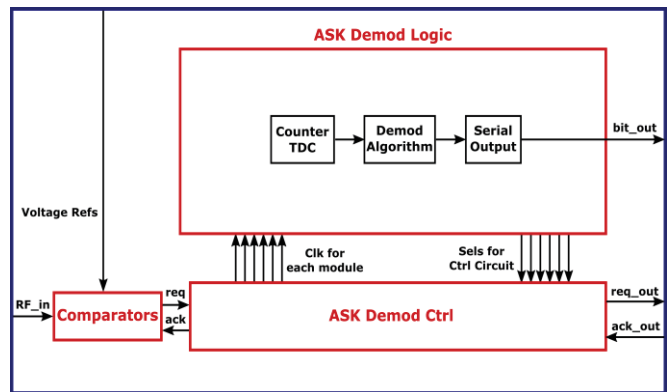


Figure 3: Schematic of the implemented testchip.

bit packets using  $urandom$  function, and the encoding is NRZ. In this result, all the simulations apply a RF input signal with a Modulation Index (MI) of 10% and a carrier frequency at 13.56 MHz. The simulations are limited by the number of error bits, the maximal number of sent bits and the simulation time. In all the testbench simulations, we have set the limits to 20 bit errors, 3,000,000 sent bits and 40 seconds of simulation.

The performance result of the designed testchip is showed in Figure 4, presenting a proper  $BER$  v/s  $SNR$  performance. A previous solution has been tested under the same simulation environment, observing a  $BER$  performance progress around 26 dB. As depicted in Figure 4, the proposed solution obtains a  $BER$  enhancement around 15 dB, demonstrating a significant improvement compared to the previous work. As an example, in the simulation where  $T_{symbol} = 2T_C$ , a  $BER$  of  $3.33 \cdot 10^{-7}$  is obtained for  $SNR \geq 16dB$ .

### IV. CONCLUSION

This paper proposed a continuous measurement TDC implementation, combining a 4-phase handshake protocol signals to a 2-phase CLICK register controller. This solution ensures in the first place the current time measurement registration, and then the right internal TDC counter reset, before letting the system to continue its normal operation. This proposal was validated using a real implementation of a digital event-based ASK demodulation circuit in FDSOI 28nm technology from STMicroelectronics. This solution uses a bundled-data asynchronous circuit and a demodulation algorithm to process the events and the measurements generated by the designed EB-ADC. The post-layout simulations result depicted in Figure 4 validate the right operation of the proposed TDC, reaching a  $BER$  value of  $3.33 \cdot 10^{-7}$  for  $SNR \geq 16dB$ .

### ACKNOWLEDGMENT

This work has been supported by the CIFRE ANRT/STMicroelectronics (N° 2018/0549) and the LabEx PERSYVAL-Lab (ANR-11-61 LABX-0025-01).

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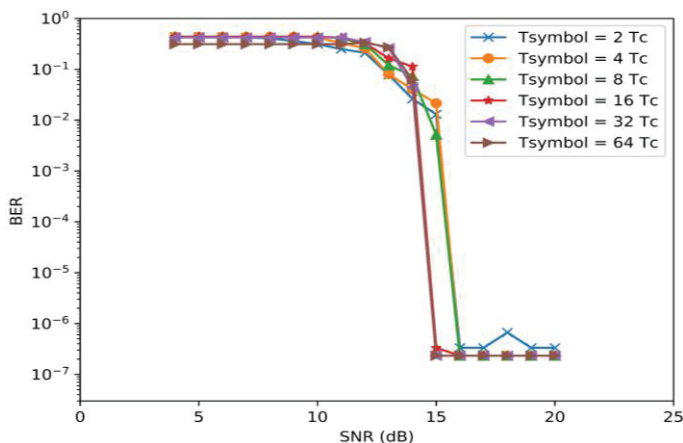


Figure 4: SNR v/s BER performance of the implemented testchip.