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# New Modelling Off-state TDDB for 130nm to 28nm CMOS nodes

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**Abstract**— We present a detailed analysis of Off-state Time Dependent Dielectric Breakdown (TDDB) under non-uniform field performed in MOSFET devices from 28nm FDSOI, 65nm SOI to 130nm nodes. Oxide breakdown in thin gate oxide is characterized under DC stress with different gate-length  $L_G$  and as function of drain voltage  $V_{DS}$  and temperature. We show that the leakage current is a better monitor for TDDB dependence under Off-mode stress whereas a new modeling is proposed. It is found that Weibull slopes  $\beta$  are higher in PFET due large amount of injected hot electrons than in NFET when hot holes are involved.

**Keywords**— CMOS, off-state damage, aging, TDDB, gate oxide breakdown, leakage current

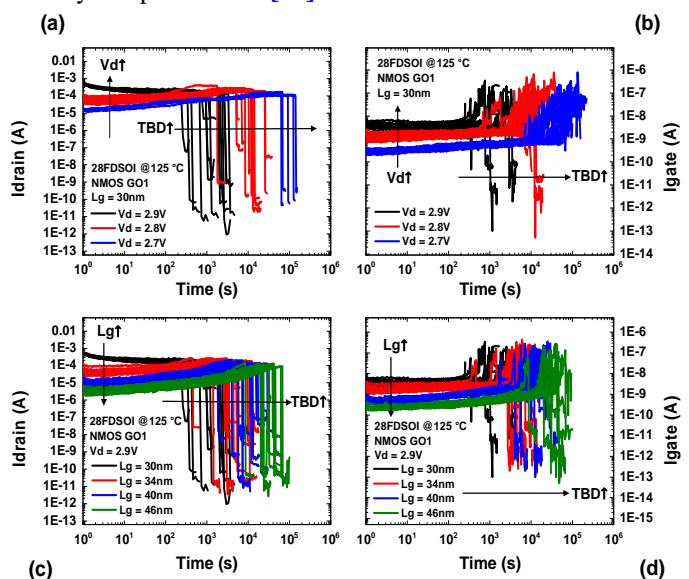
## I. INTRODUCTION

TDDB remains a key reliability concern in ultra-short channel CMOS nodes with the guaranty of speed performance and low consumption requirements. During AC RF signal operation “Off-state” occurs sequentially with “On-state” mode from low (kHz) to very high frequency range (GHz) [1-2]. Even if “Off-state” stress generally degrades device at smaller rate than “On-state” stress, it can become a limiting factor for device operation in RF domain and for mmW application at which supply voltage  $V_{DD}$  is usually doubled with respect to the one used in logic application. Not only device parameter drift might become significant but also hard breakdown (BD) may be triggered into gate-drain region. It is thus critical to precisely assess reliability for Off-state TDDB and deeply understand the wear out mechanisms at device level, as breakdown events can be observed on drain (Figs. 1a,c) and gate (Figs. 1b,d) currents in 28nm FDSOI CMOS node.

The hot-carrier (HC) generation under On-state or Off-state and its  $V_{GS}$  /  $V_{DS}$  dependence are clearly distinct in N-channel and P-channel due to difference in impact ionization (II) threshold energy and energy barrier height for holes and electrons [3]. Comparison was done between P- and N-channel [4] through HC sensitivity at low gate-voltage focusing on injected carrier efficiency, mostly regarded at the P-channel side under On-state hot-carrier degradation (HCD) on one hand, and on N-channel side under Off-state HCD on the other hand, due to the larger damage and BD sensitivity induced by hot-hole injections. This implied high energy HC that may trigger BD events in Off mode in gate-drain region [5-6] in relation to hot-hole efficiency [7].

Classical On-state HCD has historically been associated with broken  $\equiv\text{Si-H}$  bonds at Si/SiO<sub>2</sub> interface [8]. Recently Off-state HCD has been associated to broken  $\equiv\text{Si-O}$  bonds at the interface [5] with a bond dispersion model showing higher time exponent ( $n=0.7 - 0.8$ ), extending the findings to a universal modeling to On-state degradation [6]. This led to conclude that On-state HCD has no direct correlation with dielectric BD [9-11]. HCD in On-state was carried out using pre-stress step following On-state TDDB tests showing neither reduction nor acceleration of  $T_{BD}$  [12]. However, we observed recently that pre-stress HCD under multiple particle mechanism (MP) can lead to TBD reduction under Off mode TDDB compared to fresh TDDB [1, 2].

Degradation in short-channel transistors can occur in Off mode and under subthreshold conditions due to impact ionization (II) and non-conducting HC where this later is related to different leakage current components as surface band-to-band tunneling (BTBT) and gate-induced drain leakage (GIDL) [13-14]. These operation regimes may be sensitive to HC degradation and its relation to BD events with gate-voltage from  $V_{GS}$  to  $V_{Gmax}$ , where hot-hole injections near  $V_{TH}$  limit the NMOS device lifetime and may trigger more easily BD phenomena [14].



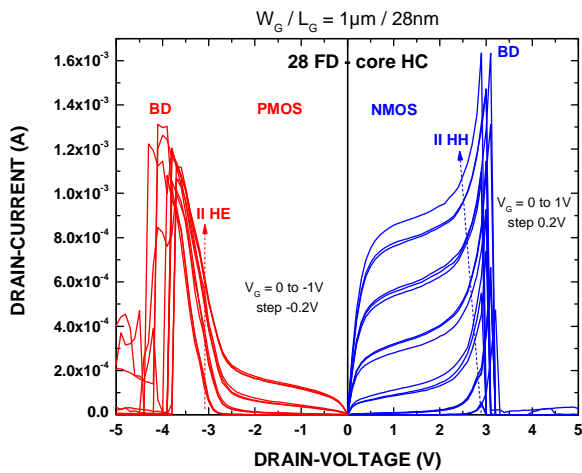
**Figure 1:** Leakage current until breakdown in 28nm FDSOI NFETs  $W_G = 1\mu\text{m}$  with various  $V_{DS}$  and  $L_G$  as a function of cumulative stress time. (a) drain and (b) gate initial currents increasing with  $V_{DS}$  for  $L_G = 30\text{nm}$ . Initial leakage current is smaller for longer devices, (c) drain current and (d) gate current monitors decreasing with  $L_G$  at the same bias  $V_{DS} = 2.9\text{V}$ .

After the description of experimental, devices used in this work and the role of impact ionization in Section 2, we present a TDDDB study under Off mode in Section 3 by studying voltage and  $L_G$  dependence using DC stressing at room temperature and high temperature (125 °C). Then in Section 4, we propose a first attempt of a TDDDB modeling under Off state stressing based on measurement of initial leakage currents.

## II. EXPERIMENTAL DESCRIPTION AND HOT-CARRIER DAMAGE FROM ON TO OFF MODE

For Off-state TDDDB study, we tested CMOS nodes with NFET and PFET 28nm devices fabricated with HKMG (EOT= 1.5nm), 65nm ( $T_{ox}$ = 1.85nm) to 130nm ( $T_{ox}$ = 2.3nm) with SiON dielectric that have been submitted to Constant Stress Voltage (CSV) applied on drain side while the gate is biased at 0V, between 125°C and 25°C. During stress we performed device I-V characterizations and leakage current measurements. First, TDDDB dependence with  $V_{DS}$ ,  $L_G$  and temperature is analyzed under DC stress on several dies and plotted as min and max BD time values ( $t_{BD}$ ). Then, the dielectric breakdown regardless soft or hard is investigated as a function of non-uniform electrical field component ( $E_{max}$ ) and the leakage currents induced by stressing drain bias ( $V_{DS}$ ).

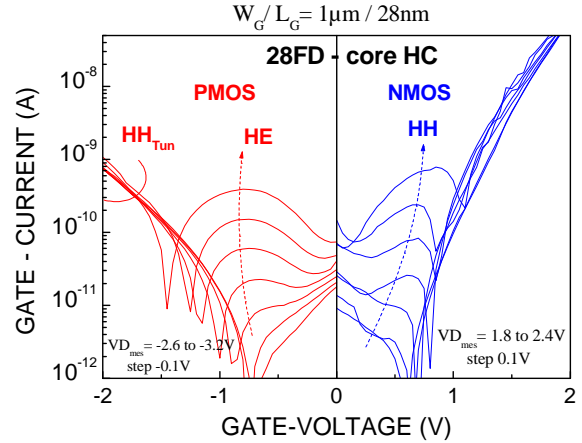
Due to high  $V_{DS}$  applied between source and drain of MOSFET, lateral electric field supplies high energy to channel carriers reaching non-equilibrium energy distribution [8]. These accelerated carriers can generate electron-hole pairs through II (Fig. 2) which may be injected into gate oxide depending on vertical field magnitude. This II phenomenon can be evidenced in Fig.3 through the measurements of electron/hole gate current. Although HC generation and its  $V_{GS}$  dependence are significantly distinct in PMOS and NMOS due to difference in II threshold energy and energy barrier height for electrons and holes, hot-hole (HH) implication in hard BD occurs earlier in Fig.2 than with hot-electron (HE) under subthreshold regime (low  $V_{GS}$ ) and under Off mode ( $V_G = 0$ ).



**Figure 2:**  $I_{DS}$  measurements until breakdown as a function of  $V_{DS}$  with variables  $V_{GS}$  in  $W_G / L_G = 1\mu m / 28nm$  FDSOI during Off-state and subthreshold conditions. Impact ionization current is higher in NFET than in PFET under same reverse bias and BD occurs around 3V in NFET with HH injection while it seems to reach -4V with HE injection before dielectric BD in PFET.

We can observe in Fig. 3 different bias regions of injected hot-electrons in PFET and hot-holes in NFET during Off mode and subthreshold bias condition which are then replaced at larger  $V_{GS}$  by direct hole (electron) gate tunneling current components in P-channel (N-channel, respectively).

As dielectric BD has been shown to be independent to hot-carrier degradation in On mode, we extracted in Fig. 4  $Id_{Lin}$  drift after  $10^4$  s stress between 25 °C and 125 °C in 28FDSOI NFET  $L_G = 30$  nm under DC HCD On-state (modeling shown in lines) on one hand and DC HCD Off-state on the other hand, for fixed  $V_D = 1.5$  to 1.8V and  $V_G = -1$  up to 1.8V.

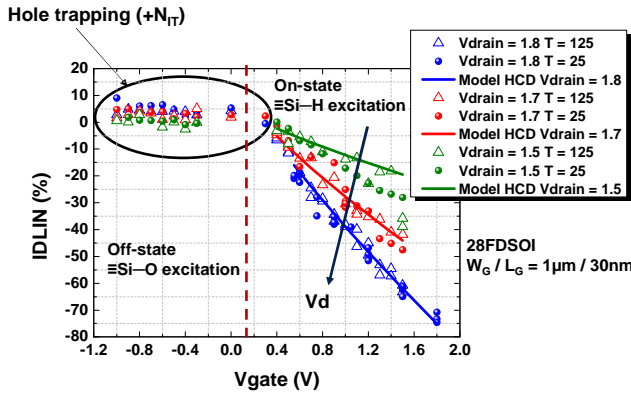


**Figure 3:** Consequence of Impact Ionization shown in NFET and PFET  $W_G / L_G = 1\mu m / 28nm$  FDSOI under HC mode seen by gate current ( $I_{gate}$ ) measurements in thin gate-oxide for  $V_{DS}$  and  $V_{GS}$  variables, showing the distinct injection mechanisms between hot-electrons and hot-holes at low  $V_{GS}$  which turns around to a single tunneling component at high  $V_{GS}$ .

This first shows that  $\Delta Id_{Lin}$  during On mode HCD above  $V_{TH}$  continuously increases (negatively) with  $V_{GS}$  and  $V_{DS}$  and follows a time power law reported as to be due to interface defects generation ( $\Delta N_{IT}$ ) [1-2] related to  $\equiv Si-H$  bonds breaking at Si/SiO<sub>2</sub> interface [8, 15, 16]. Whereas under Off mode HCD stress and subthreshold condition we observe in Fig.4 that  $\Delta Id_{Lin}$  is positive and doesn't exceed 10%, which might be related to  $\equiv Si-O$  bonds excitation, we observe the opposite behavior ( $\Delta Id_{Lin} < 0$ ) under On mode HCD stress (Fig. 4) according to acceptor type  $\Delta N_{IT}$ .

Time dynamics also differ between On and Off states HCD since this follows under Off mode a logarithmic time dependence commonly reported as to be due to hot-holes trapping (like under NBTI [17]) in N-channel case device. In our previous work [1] we had performed relaxation phases by alternating fresh Off-state sequence to recovery phase at  $V_{DS} = V_{GS} = 0V$  and that showed generation of permanent defects ( $N_{IT}$ ) and recoverable one. This implies trapped/detrapped charge in stressed interface layer under oxide on scaled device. Nevertheless,  $\Delta Id_{Lin}$  during HCD Off mode in 65 and 130 nm CMOS nodes has known to not recover on the removal of the stress conditions [5], probably due to the lack of ultra-thin gate-oxide defects. In [1] interaction between HCD On-state and HCD off-state on 28FDSOI NFET has been evidenced by alternating DC sequences as previously done in [18] showing a history effect when charges are captured in silicon dangling bonds at interface during Off-state. This interaction between HCD

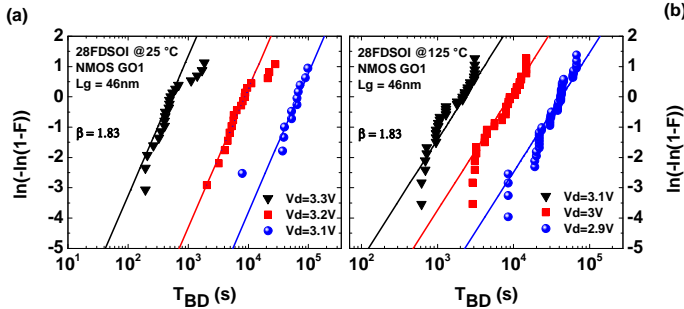
On and Off modes and the defect generation properties has been modeled in [2].



**Figure 4:**  $\Delta I_{D,lin}$  ( $V_d = 50$  mV) in 28FDSOI N-channel  $L_G = 30$  nm extracted at  $t_s = 10^4$  s. Vg dependence of  $\Delta I_{D,lin}$  under HCD in On and Off modes with Vg stress between -1 and 1.8 V with the modeling (lines) in On mode with room temperature (25 °C) and T = 125 °C.

### III. DC OFF-STATE TDDDB WITH VOLTAGE, GATE-LENGTH AND TEMPERATURE DEPENDENCE

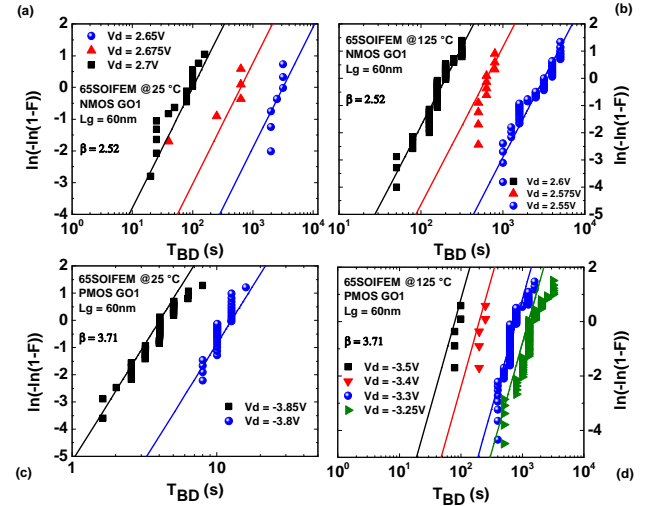
CVS are commonly used to monitor  $t_{BD}$  dependences and to build up the complete TDDDB distribution functions by using different stress voltages and devices areas. In this goal, the recent investigations on Off-state TDDDB are performed under CVS in thin gate oxide (GO1) from different technologies with different gate-length ( $L_G$ ). Under On-state stressing,  $\beta$  generally depends on gate-oxide thickness as expected for Poisson area scaling law while it is essentially independent of stress conditions such as temperature, voltage and frequency [19-22].



**Figure 5:** Cumulative distribution with same Weibull slope obtained in GO1  $W_G/L_G = 1\mu m/46nm$  28FDSOI NFET at various stressing drain bias between (a) 25 °C and (b) 125 °C.

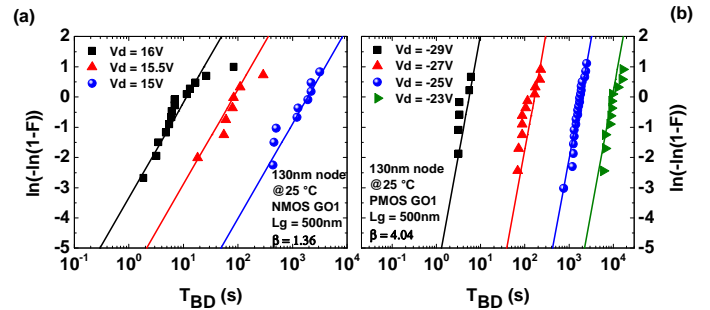
For fresh  $L_G = 30nm$  28FDSOI NFET ( $t_s = t_0$ ), the Stress Induced Leakage Current (SILC) component at drain side (Fig. 1a) and into volume gate-oxide (Fig. 1b) increases with  $V_{DS}$  while SILC is reduced in longer  $L_G$  at the same bias (Figs. 1c,d). Under these conditions, even without inversion layer build-up, carriers can be injected from drain edge by impact ionization, and with helps from GIDL and BTBT combination by the favoring vertical electric field, creating defects at the interface and into volume gate-oxide. This occurs not only in the small area of gate to drain overlap

region [23] but may extends towards the channel from the deep depleted drain layer.



**Figure 6:** Weibit distribution plots for GO1  $W_G/L_G = 10\mu m/60nm$  65 SOI NFET and PFET at various drain voltage (a) NFET at 25 °C, (b) NFET at 125 °C, (c) PFET at 25 °C and (d) PFET at 125 °C. Weibull distribution slopes  $\beta$  are higher in PMOS than in NMOS an independent of bias&temperature.

The gate current ( $I_{gate}$ ) is plotted in Fig. 3 below  $V_{th}$  and at high  $V_{DS}$  which evidences hole and electron injections into the gate oxide [4, 14]. Similar behavior was confirmed using charge pumping measurement [6, 24] showing the net increase in interface traps and the generation of bulk traps.  $t_{BD}$  is detected in Figs.1a-d, by current abrupt jumps at both drain and gate terminals confirming the creation of a percolation path in the (high-k) gate stack localized at the drain edge [25, 26].

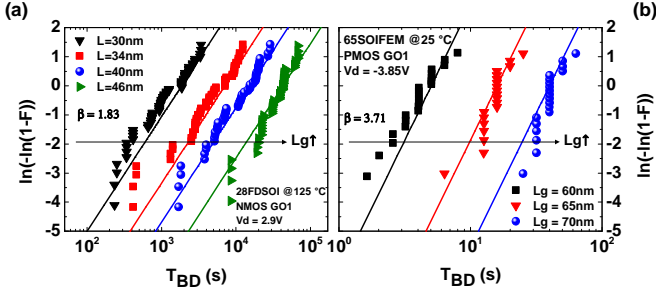


**Figure 7:** Time to breakdown distribution plots for GO1  $W_G/L_G = 10\mu m/500nm$  130nm FET at 25 °C and various drain voltage  $V_{DS}$  (a) in NMOS with lower  $\beta$  and (b) in PMOS devices.

Fig. 5 to Fig. 8, shows  $t_{BD}$  under Off-state in the case of NFET and PFET from various CMOS nodes with thin gate oxides, which are well characterized by Weibull distributions. This gives a smaller  $\beta$  value in NFET [6, 26], which suggests that hot-hole injection ( $E > 4.8eV$ ) is more damaging than hot-electron ( $E > 3.1eV$ ) injection in PFETs, as further confirmed by Monte Carlo based SMC simulation [27]. Percolation phenomenon modeling based on asymmetric paths could successfully explain the higher Weibull slopes observed for N- and P-channel Off-state breakdown time distribution [28] than the one expected from standard percolation model [29-30]. We see that the basic degradation mechanisms remain similar for both NMOS and PMOS transistors (Figs.6-7) with same geometries and



EOT. The lateral profiling of interface damage during Off-state stress [5, 6] shows that the peak degradation occurs outside the gate edge where BD occurs in the spacer region, co-located with peak interface damage. Nevertheless, the dielectric BD time at stress bias under Off mode and the Weibull slope for PMOS transistors is found to be higher compared to NMOS, due to the non-uniform bulk trap generation and the longer percolation path for holes in PMOS device [6].



**Figure 8:** TDDb time to failure distribution for different FET gate lengths at fixed drain voltage (a) 28 FDSOI NFETs  $W = 1\mu\text{m}$  for  $V_{DS} = 2.9\text{V}$  and (b) 65 FEM PFETs  $W = 10\mu\text{m}$  for  $V_{DS} = -3.85\text{V}$ . Breakdown occurs later for longer devices (same  $\beta$  as for various  $V_{DS}$  and temperature).

We observed in **Figs. 8a,b** with 28FDSOI NFETs and 65SOI PFETs that Off mode TDDb increases with  $L_G$  without changing markedly  $\beta$  slope value for each device type. However, voltage acceleration factors (VAF) that we obtain with (1) using a power law modeling [26] (**Figs. 9a-c**) are significantly higher than the one obtained under On-state TDDb (see Table 1).

$$t_{BD} = A \cdot L_G^{LAF} \cdot V_D^{-VAF} \cdot \frac{1}{w} \cdot e^{\left(\frac{\ln(-\ln(1-F))}{\beta}\right)} \cdot e^{\left(\frac{E_a}{kT}\right)} \quad (1)$$

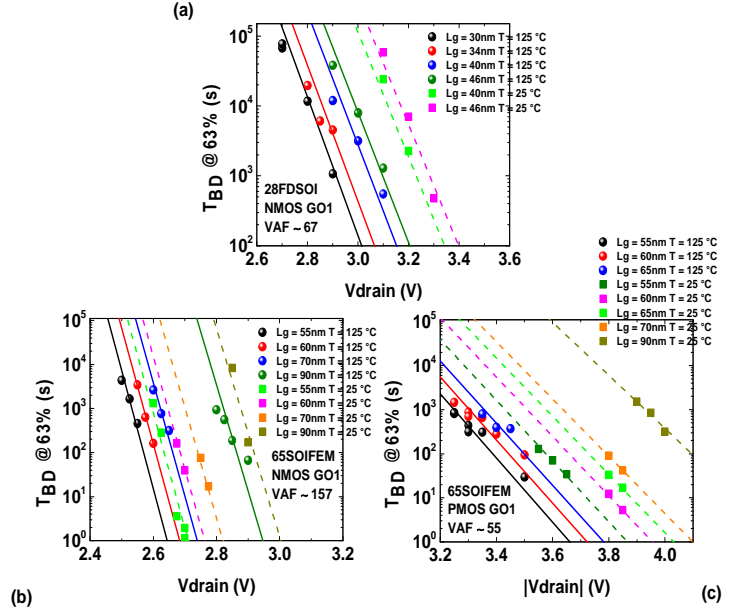
Experimental data for each technology can be characterized with the same VAF power law, independently of geometry and stress conditions. The BD voltage range is extremely tight (**Figs. 6a-d**) that it is susceptible to not detecting dielectric failure which can be masked by high avalanche current. This leads us to the point that Off-state breakdown might not be

	28FDSOI		65SOI		130nm node	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
$E_a$ Off	0.4	0.1	0.1	0.1		
$E_a$ On	0.6	0.54	0.62	0.62		
$\beta$ off	1.83	2.52	3.71	1.36	4.04	
$\beta$ on	0.9	1.59	1.51	1.09	2.52	
VAF off	67	157	55	78	32	
VAF on	43	40	33	44	30	
LAF	8	20	14			

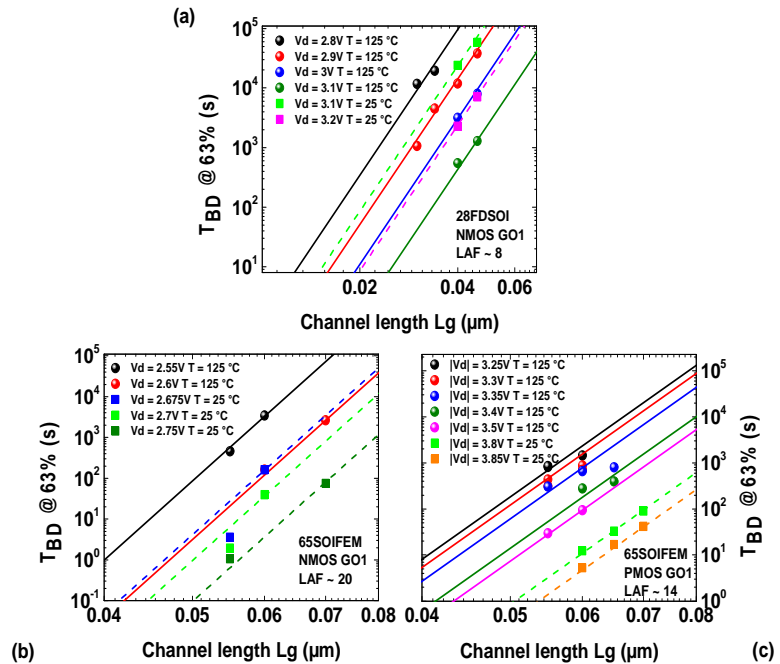
**Table 1:** Illustration of  $t_{BD}$  laws according to (1) with  $E_a$ ,  $\beta$ , VAF and LAF parameters.  $\beta$  and VAF are higher under Off-state TDDb in contrast to  $E_a$  related to the largest  $\beta$  extracted in PMOS device and VAF in NMOS device.

occurring only into the gate-drain overlap region, but eventually extends from the drain edge with the spread of space-charge zone (SCZ) towards the source at high  $V_{DS}$  [4, 5, 6]. Moreover, we observe a strong  $L_G$  effect in **Figs. 10a-c** which suggests that gate-oxide damage is correlated to HC injections into the gate-oxide. We show that shorter TDDBs are obtained at higher stressing temperature that enables the

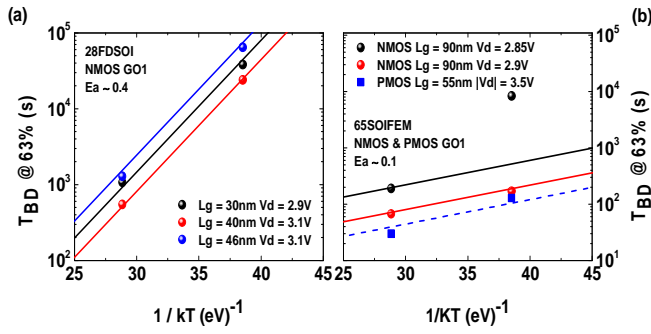
extraction of an apparent temperature activation energy ( $E_a$ ) from **Figs. 11a,b** which gives similar values (0.1 to 0.4eV) than the one obtained in other technologies [26] under similar stressing condition. In contrast to  $\beta$  and VAF effects, thermal activation is found lower during Off mode TDDb than under On mode TDDb (see Table 1).



**Figure 9:**  $t_{BD}$  time to failure in GO1 28FD and 65FEM obtained at 63% vs. drain voltage with various channel length  $L_G$  in order to extract acceleration factors VAF at 125°C (solid lines) and 25°C (dashed lines). (a) 28nm NFETs, (b) 65nm NFETs and (c) 65nm PFETs. A common VAF can be extracted independently of gate channel length and temperature. VAF is found to be higher in Off-state than On-state (Table 1).



**Figure 10:** TDDb in GO1 28FD and 65FEM obtained at 63% vs. channel length  $L_G$  with various drain voltage (reverse case of **Fig. 8**) in order to extract acceleration factors LAF at 125°C (solid lines) and 25°C (dashed lines). (a) 28nm NFETs, (b) 65nm NFETs and (c) 65nm PFETs. A common LAF is extracted independently of drain bias and temperature.



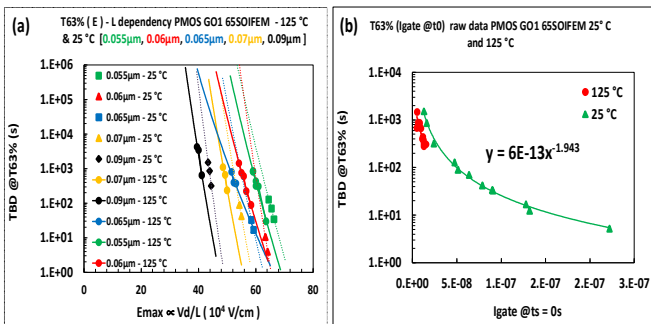
**Figure 11:** Temperature dependence of  $T_{BD}$  (63%) under Off-state stressing (a) in 28FDSOI NMOS GO1 and (b) in 65SOI P- and N- FETs extracted from 125 °C to 25 °C. The activation energy ( $E_a$ ) remains constant for different gate channel length.

#### IV. MODELING FROM ELECTRICAL FIELD TO LEAKAGE CURRENTS

To investigate the potential role of HC injection under Off-mode till breakdown event, we firstly modeled TDDB as a function of average lateral field  $E_{max} \equiv V_{DS}/L_G$  giving the peak value of electrical field at the drain edge. We found out that it does not give a satisfactory modeling of  $V_{DS}$  and  $L_G$  effects as we see in **Fig. 12a** and **Fig. 13a** that different slopes vs.  $E_{max}$  are observed for devices with different  $L_G$  stressed at various or same  $V_{DS}$ . As a matter of fact, under On-state stressing, charge trapping, and scatterings lead to band diagram deformation and modifies the electrical field profile which becomes non-uniform while the currents remain roughly constant. Under Off-state, electrical field is far less uniform. Therefore, we analyzed TDDB results as a function of drain leakage current  $I_{D,Off}$  ( $V_{GS} = 0$ ) corresponding to the point bias of  $I_{gate,Off}$ . We found with (2) that various  $V_{DS}$  and  $L_G$  stress configurations lie on same dependence with gate current in **Fig. 12b** and **Fig. 13b**.

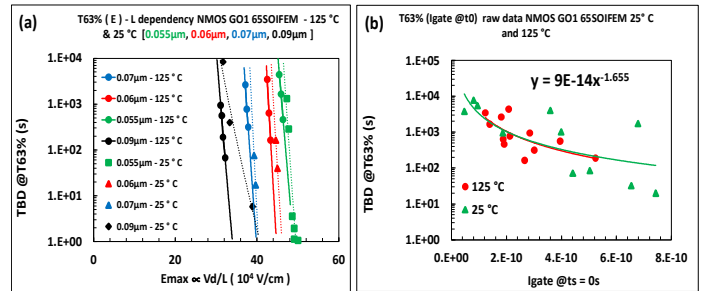
$$t_{BD63\%} = B \cdot I_{g,off}^p \cdot \exp\left(\frac{E_a}{kT}\right) \quad (2)$$

The same trend is shown for different technologies in **Fig. 14a**, as a function of drain leakage current in **Figs. 14b**. As observed in **Fig. 12b** and **Fig. 13b**, the power exponent  $p$  is much smaller than VAF. We believe that  $I_{D,Off}$  and  $I_{g,Off}$  are relevant figure of merits for HC injection and non-conducting HC under Off-state stressing mode.

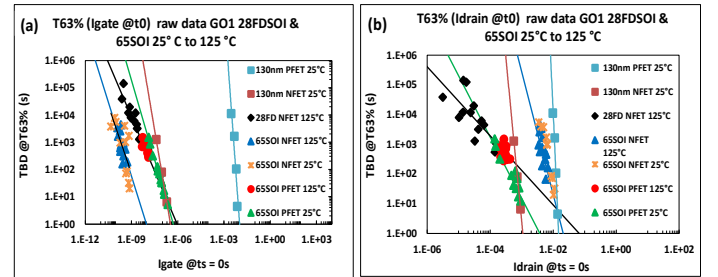


**Figure 12:** Lifetime plots as  $T_{BD}$  at 63% for 65nm PFET (a) vs. electrical field  $E_{max} \equiv V_{DS}/L_G$  enlightening  $L_G$  dependence between 25°C (dashed lines) and 125°C (solid lines) and (b) vs. gate oxide initial leakage current overcoming  $L_G$  dependence between 25°C and 125°C.

As shown in **Figs. 1a-d**, leakage currents vary initially with stress voltage  $V_{DS}$  and gate-length  $L_G$ , reflecting the evolution of volumetric defect density [31, 32]. This showed that created defects may be distributed over the entire surface of the dielectric and therefore can be used as a main tool for BD characterization and a global modelling of time to BD in Off-state mode. Indeed, only few investigations are given on effective electric field with  $V_{DS}$  only, and on the Off-state current with gate-length  $L_G$  [33-38]. Using the fact that applied electric field responsible for the oxide BD is strongly related to carrier energy and the amount of HC induced by II from the drain junction, we characterize roughly the impact of carrier energy by the peak electric field dependence  $E_{max} \approx V_{DS}/L_G$  in thin gate-oxide structures, with same  $W_G$  and variable gate-length.



**Figure 13:** Lifetime plots defined for  $T_{BD}$  at 63% in 65nm NFET (a) vs. electrical field  $E_{max} \equiv V_{DS}/L_G$  pointing out the  $L_G$  dependence between 25°C (dashed lines) and 125°C (solid lines) and (b) vs. gate-oxide initial leakage current overcoming  $L_G$  dependence between 25°C and 125°C.



**Figure 14:**  $T_{BD}$  at 63% lifetime model as a function of initial ( $t_0$ ) leakage current in 28nm, 65nm and 130nm N- and P- FETs (a) gate current and (b) drain current monitors, between 25°C and 125°C. This shows better lifetime monitoring using gate leakage and slightly more dispersion in NFETs.

The Off current characteristics are composed in **Fig.15** of two components, the first one related to junction leakage currents and the second one to avalanche departure once II has been involved. Thus,  $I_{DS}$  can be modeled with (3) similarly to a diode-like framework [39]. The voltage condition at which avalanche appears is obtained with (4) and depends mainly on  $L_G$  with constant  $D_1$  and  $D_2$  parameters (Table 2), for each CMOS node, that is exemplified in 28FDSOI here.

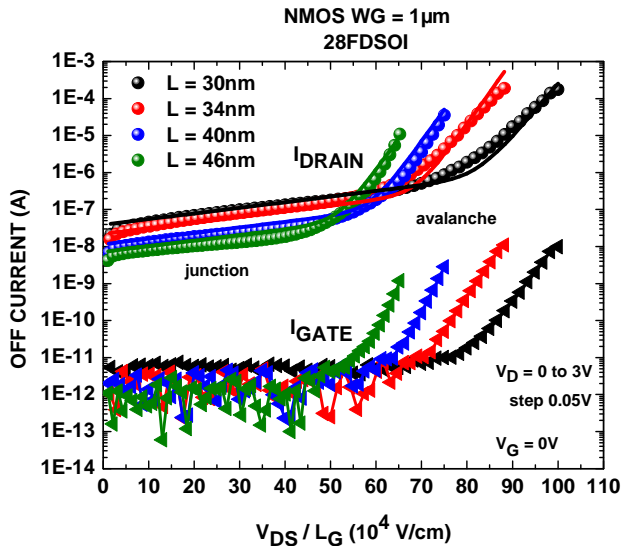
$$I_{D,off} = C \cdot I_0(T) \cdot \left( \exp\left(\alpha(T) \cdot \frac{V_{DS}}{L_G} + b(T)\right) \right) \left( \exp\left(\alpha(T) \cdot \frac{V_{DS} - V_{D_{avalanche}}}{L_G} + 1\right) \cdot \exp\left(\frac{E_a}{kT}\right) \right) \quad (3)$$

where  $\exp\left(\alpha(T) \cdot \frac{V_{DS}}{L_G} + b(T)\right)$  is related to junction component and  $\left(\exp\left(\alpha(T) \cdot \frac{V_{DS} - V_{D_{avalanche}}}{L_G} + 1\right)\right)$  to the avalanche current.

$$V_{D_{avalanche}} = \frac{D_1}{1 + \sqrt{1 + \frac{D_2}{L_G}}} \quad (4)$$

28FDSOI		
	125 °C	25 °C
$I_0$	$5.10^{-9}$	$3.10^{-11}$
$a$	35	70
$b$	146	200
$\alpha$	$3.6.10^2$	$2.4.10^2$
$C$	0.06	
$D_1$	5	
$D_2$	10	

**Table 2:** Summary of (3) and (4) parameters used for  $I_{D,Off}$  empirical modelling.



**Figure 15:**  $I_{DS}$  and  $I_G$  measurements and modeling at  $T = 125^\circ\text{C}$  under Off-state ( $V_{GS} = 0$ ) for  $L_G = 30\text{nm}$  to  $46\text{nm}$  NFETs as a function of peak lateral field approximated to  $E_{max} \approx V_{DS} / L_G$  showing a junction leakage and avalanche components in the diode currents. The modeling is shown in lines for  $I_{DS}$  monitoring with relatively good agreements as a function of gate-length  $L_G$ .

In **Fig.15** we observe that  $I_{D,Off}$  ( $V_{GS} = 0$ ) is composed by a junction currents which becomes higher with  $L_G$  reduction while gate current  $I_{gate,Off}$  and  $I_{D,Off}$  both increase with  $L_G$  due to tunneling contributions. This later is mainly dependent on surface band-to-band tunneling mechanism and drain induced gate leakage that both may be involved at medium electric field magnitude (0.2 to 1 MV/cm in **Fig.15**) in ultra-thin gate-oxide NFETs (FDSOI with EOT= 1.5nm). Therefore, the dependence with  $I_{D,Off}$  explains the  $t_{BD}(63\%)$  relationships with  $E_{max}$  proposed in (3)-(4) and shown in **Fig.12a** in P-channel and **Fig.13a**, in N-channel MOSFETs in the range of  $L_G = 55\text{nm}$  to  $90\text{nm}$  (SOI) at  $25^\circ\text{C}$  and  $125^\circ\text{C}$ .

## V. CONCLUSION

The Off-state TDDDB mechanisms involved in the degradation of distinct CMOS nodes have been investigated in detail for relevant conditions related to RF-mmWave applications. A  $t_{BD}$  lifetime model based on power law dependence has been developed as a function either of  $I_{D,Off}$  or  $I_{g,Off}$  leakage currents. Such approaches can account simultaneously for  $V_{DS}$  and  $L_G$  dependencies related to the diode current configuration that has been empirically modeled. Both modeling guaranties the lifetime extraction

in Off-state mode and enables us to identify the limits and sensitivity between Off-mode and hard breakdown events for ultra-short devices with ultra-thin gate-oxide.

## REFERENCES

- [1] T. Garba-Seybou, X. Federspiel, A. Bravaix, F. Cacho, "Analysis of the interactions of HCD under "On" and "Off" state modes for 28nm FDSOI AC RF modelling", Proc. Int. Reliability Phys. Symp. (IRPS) 2021, pp. 31–35.
- [2] T. Garba-Seybou, A. Bravaix, X. Federspiel, F. Cacho, "Modeling hot carrier damage interaction between on and off modes for 28 nm AC RF applications", Microelectronics Reliability, vol. 126, p. 114342, 2021.
- [3] D. Esseni, J.D. Bude, L. Selmi, "On Interface and oxide degradation in VLSI MOSFETs - part I: deuterium effect in CHE stress regime", IEEE Trans. on Elec. Dev., vol. 49 (2), p. 247, 2002.
- [4] S. Li, A. Bravaix, E. Kussener, D. Ney, X. Federspiel, F. Cacho, "Hot-carrier degradation in P- and N-channel EDMOS for smart power application", Microelectronics Reliability vol. 114, p. 113811, 2020.
- [5] D. Varghese, H. Kufluoglu, V. Reddy, H. Shichijo, D. Mosher, S. Krishnan, M. Ashraf Alam, "OFF-State Degradation in Drain-Extended NMOS Transistors: Interface Damage and Correlation to Dielectric Breakdown", IEEE Trans. on Elec. Dev., vol. 54, n°10, pp. 2669- 2678, 2007.
- [6] D. Varghese, V. Reddy, H. Shichijo, D. Mosher, S. Krishnan, M. A. Alam, "A Comprehensive Analysis of Off-State Stress in Drain Extended PMOS Transistors: Theory and Characterization of Parametric Degradation and Dielectric Failure", in Proc. Int. Reliability Physics Symp. (IRPS) 2008, pp. 566-574.
- [7] P. Moens, G. Van Den Bosch, C. De Keukeleire, R. Degraeve, M. Tack, G. Groeseneken, "Hot hole degradation effects in lateral nMOS transistors", IEEE Trans. Electron Devices, vol. 51 (10), p.1704, 2004.
- [8] S. Tyaginov et al. "Physics-Based Hot-Carrier Degradation Models". Electrochemical Society Transactions, vol. 35(4), 2011.
- [9] J. D. Bude, B. E.Weir, and P. J. Silverman, "Explanation of stress-induced damage in thin oxides", Int. Electron Devices Meeting (IEDM) 1998, pp. 179–182.
- [10] R. Degraeve, B. Kaczer, and G. Groeseneken, "Degradation and breakdown in thin oxide layers: Mechanisms, models, and reliability prediction," Microelectronic Reliability, vol. 39, no. 10, pp. 1445–1460, 1999.
- [11] M. A. Alam, B. Weir, P. Silverman, J. Bude, A. Ghetti, Y. Ma, M. M. Brown, D. Hwang, and A. Hamad, "Physics and prospects of sub-2 nm oxides," in Proc. Int. Symp. Phys. Chem. SiO2 Si-SiO2 Interface, 2000, pp. 365–376.
- [12] X. Federspiel, M. Rafik, M. Arabi, A. Cros and F. Cacho, "FDSOI MOSFET gate dielectric breakdown  $V_d$  dependency," 2018 International Integrated Reliability Workshop (IIRW) 2018, pp. 1-4.
- [13] D. Varghese, M. Nandakumar, S. Tang, V. Reddy and S. Krishnan, "Energy driven modeling of OFF-state and sub-threshold degradation in scaled NMOS transistors," 2014 IEEE International Reliability Physics Symposium (IRPS) 2014, pp. 4A.2.1-4A.2.4.
- [14] A. Bravaix, E. Kussener, D. Ney, X. Federspiel, F. Cacho, "Hot-carrier induced breakdown events from Off to On mode in NEDMOS", in: Proc. Int. Reliability Physics Symp. (IRPS) 2020, 3A4-1-6.
- [15] S.E. Rauch, G.La Rosa, The energy driven paradigm of NMOSFET hot carrier effects, in: Proc. Int. Reliability Physics Symp. (IRPS) 2005, pp. 708–709.
- [16] C. Guérin, V. Huard, A. Bravaix, General framework about defect creation at Si/ SiO2 interface, J. Appl. Phys. 105, p. 114513, 2009.
- [17] M. Denais, A. Bravaix, C. Parthasarathy, G. Ribes, Y. Rey-Tauriac, N. Revil, V. Huard, F. Perrier, On-the-fly characterization of NBTI in ultra-thin gate oxide PMOSFET's, Proc. Int. Electron Devices Meeting (IEDM) 2004, 109–112.
- [18] X. Federspiel, F. Cacho, D. Roy, Experimental characterization of interactions between HCI, off-state and BTI degradation modes, Proc. Int. Integr. Reliab. Work. (IIRW) 2011, 133–136.
- [19] E. Y. Wu, J. Sune and W. Lai, "On the Weibull shape factor of intrinsic breakdown of dielectric films and its accurate experimental determination. Part II: experimental results and the effects of stress conditions," in IEEE Transactions on Electron Devices, vol. 49, no. 12, pp. 2141-2150, Dec. 2002.
- [20] C. LaRow, Z. Chbili, S. F. Yap, A. Kerber and T. Nigam, "Fast TDDDB monitoring for BEOL interconnect dielectrics," 2017 IEEE International Integrated Reliability Workshop (IIRW) 2017, pp. 1-4.

- [21] M. Arabi, X. Federspiel, F. Cacho, M. Rafik, A.-P. Nguyen, X. Garros, et al., "New insights on device level TDDDB at GHz speed in advanced CMOS nodes", *IEEE Trans. Device Mater. Rel.*, vol. 19, no. 2, pp. 255-261, Jun. 2019.
- [22] M. Arabi, X. Federspiel, F. Cacho, M. Rafik, A.-P. Nguyen, X. Garros, G. Ghibaudo, "Temperature dependence of TDDDB at high frequency in 28FDSOI", *Microelectronics Reliability* 100-101 (2019) 113422.
- [23] E. Wu, E. Nowak and Wing Lai, "Off-state mode TDDDB reliability for ultra-thin gate oxides: New methodology and the impact of oxide thickness scaling," 2004 IEEE International Reliability Physics Symposium. Proceedings (IRPS) 2004, pp. 84-94.
- [24] D. Varghese and M. A. Alam, "Charge Pumping as a Monitor of off-State TDDDB in Asymmetrically Stressed Transistors," in *IEEE Electron Device Letters*, vol. 30, no. 9, pp. 972-974, Sept. 2009.
- [25] S. Kupke, S. Knebel, S. Rahman, S. Slesazeck, T. Mikolajick, R. Agaiby and M. Trentzsch, "Dynamic off-state TDDDB of ultra short channel HKMG nFETS and its implications on CMOS logic reliability," 2014 IEEE International Reliability Physics Symposium, (IRPS) 2014, pp. 5B.1.1-5B.1.6.
- [26] M. Toledano-Luque, P. Paliwoda, M. Nour, T. Kauerauf, B. Min, G. Bossu, M. Siddabathula and T. Nigam, "Off-state TDDDB in FinFET Technology and its Implication for Safe Operating Area," 2021 IEEE International Reliability Physics Symposium (IRPS), 2021, pp. 1-6.
- [27] J. D. Bude, M. R. Pinto, and R. K. Smith, "Monte Carlo simulation of the CHISEL flash memory cell," *IEEE Trans. on Electron Devices*, vol. 47, pp. 1873-1881, 2000.
- [28] D. Varghese, H. Kufluoglu, V. Reddy, H. Shichijo, D. Mosher, S. Krishnan, and M. A. Alam, "Multi-probe Two-Dimensional Mapping of Off-State Degradation in DeNMOS Transistors: How and Why Interface Damage Predicts Gate Dielectric Breakdown," in *Proc. Int. Electron Device Meeting (IRPS) 2007*, pp. s19.4.
- [29] R. Degraeve, G. Groeseneken, R. Bellens, M. Depas, and H. E. Maes, "A consistent model for the thickness dependence of intrinsic breakdown in ultra-thin oxides," in *Int. Electron Devices Meeting (IEDM) 1995*, pp. 863-866.
- [30] J. Sune, "New physics-based analytic approach to the thin-oxide breakdown statistics," *IEEE Electron Device Letters*, vol. 22, pp. 296-298, 2001.
- [31] A. Cattaneo, S. Pinarello, J.-E. Mueller, R. Weigel, "Impact of DC and RF non-Conducting Stress on nMOS Reliability", in *Proc. Int. Reliability Physics Symp. (IRPS) 2015*, XT.4.1-4.4.
- [32] B.A. Buchanan, D.J. DiMaria, C-A. Chang, Y. Taur, "Defect generation in 3.5nm silicon dioxide films", *Appl. Phys. Lett.*, vol. 65, pp. 1820-1822, 1994.
- [33] A. Bravaix, C. Guérin, D. Goguenheim, V. Huard, D. Roy, C. Besset, S. Renard, Y. Mamy Randriamihaja, E. Vincent, "Off state incorporation into the 3 energy mode device lifetime modeling for advanced 40nm CMOS node," 2010 IEEE Int. Reliability Physics Symposium (IRPS) 2010, pp. 55-64.
- [34] P. Devoge, H. Aziza, P. Lorenzini, F. Julien, A. Marzaki, A. Malherbe, M. Mantelli, T. Cabout, J. Delalleau, S. Haendler, A. Regnier, S. Niel, "Hot-carrier evaluation of a zero-cost transistor developed via process optimization in an embedded non-volatile memory CMOS technology", *Microelectronics Reliability*, vol. 126, p. 114265, 2021.
- [35] A. O. Adan, Y. Fukushima, K. Higashi, "The off-state leakage current in ultra-thin SOI MOSFET's", *Proc. Int. Conference on Solid State Devices and Materials (SSDM) 1998*, pp. 318-319.
- [36] G. -B. Lee, C. -K. Kim, M. -S. Yoo and Y. -K. Choi, "Low-Frequency Noise Characteristics Under the OFF-State Stress," in *IEEE Transactions on Electron Devices*, vol. 67, no. 10, pp. 4366-4371, Oct. 2020.
- [37] X. Zhao, A. Vardi and J. A. del Alamo, "Excess Off-State Current in InGaAs FinFETs," in *IEEE Electron Device Letters*, vol. 39, no. 4, pp. 476-479, April 2018.
- [38] N. -H. Lee, J. Kim, D. Son, K. Kim and J. E. Seok, "Comprehensive Study for OFF-State Hot Carrier Degradation of Scaled nMOSFETs in DRAM," *Int. Reliability Phys. Symp. (IRPS) 2019*, pp. 1-4.
- [39] Taur and T. H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge University, 2<sup>nd</sup> Edition, 2009.



