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ELECTRICAL AND CHEMICAL INVESTIGATIONS OF Cu(In,Ga)Se₂ / CdS INTERFACES

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ABSTRACT: In thin film polycrystalline Cu(In,Ga)Se₂/CdS solar cells, the intrinsic and interface defect properties are of primary importance for their performance. In this paper, we have performed Capacitance Spectroscopy, XPS and Kelvin probe measurements in order to gain a better understanding of the heterointerface properties at different stages of its formation. All investigations were carried out on Cu(In,Ga)Se₂ co-evaporated samples elaborated in pilot-line conditions onto which CdS layers with different thickness were deposited by CBD. From the capacitance measurements versus frequency and temperature, the gap states density evolution was derived using the Walter et al. method [1]. A shallow interface defect was identified with a strong evolution of its density of states with the CdS layer thickness. XPS profiles of the heterojunction were obtained by sputter-etch so as to study the composition at the buried interface. Kelvin probe measurements under dark and illumination showed that the interface is not built until ZnO is deposited and that significant charge is trapped in CdS under illumination. The results obtained by these different characterization techniques at different stages of the heterojunction formation were correlated to the evolution of the solar cells electrical performances.

Keywords : Cu(In,Ga)Se₂ - 1: Capacitance - 2: XPS - 3.

1. INTRODUCTION

Cu(In,Ga)Se₂ (CIGS) provides today the most efficient way for thin film photovoltaic devices, as shown by its remarkable performance in laboratory-sized cells, and more significantly on large area [2]. Yet, one of the main challenges to progress in that technology rests on the control of interfacial properties. This problem is common to many semiconductor devices, and is especially crucial in heterojunction devices. Due to the chemical complexity of the interface in devices, the causes for the high performance of the devices or the performance degradation are not yet well understood. In the present work we aimed at finding relationships between electrical and chemical properties of the CIGS/CdS interface in CIGS based solar cells and how these appear as the junction is built. In this perspective, we have investigated interfaces by Admittance Spectroscopy, XPS profiles and Kelvin Probe measurements under dark and illumination. Co-evaporated CIGS samples of technologically relevant elaboration underwent various CdS thickness deposition. Admittance measurements have been proposed as a powerful method for the identification of bulk and interface traps in semiconductor devices. For thin film devices we have extensively used this technique to investigate the gap states spectroscopy of hydrogenated amorphous silicon and related materials ([3-6]). In this paper, this technique was performed to study CIGS solar cells using a method proposed by Walter et al. [1] to derive the gap states distribution from the

capacitance spectra. Kelvin probe can be used to assess the performances of the device prior to or after ZnO deposition [7]. XPS of buried CIGS/CdS interface was carried out to correlate the chemistry of the interface to its electrical properties.

2. EXPERIMENTAL

The CIGS thin films (thickness around 2 μm) were prepared by co-evaporation of the elements on Mo-coated glass (thickness around 0.5 μm) at the Zentrum für Solarenergie und Wasserstoff, Stuttgart as described in [1]. Their nominal composition, measured by EDX, was: Cu 21.5%, In 17.9%, Ga 8.8% and Se 51.8%. After deposition, they had been packed and sealed under Ar, and kept in dry ambient until the experiments were carried out.

Using the model developed by Walter et al. [1], the gap states spectroscopy is derived from the capacitance spectra versus temperature and frequency. Temperature varies from 80 K to 380 K and the frequency ranges from 40 Hz to 1 MHz. Three different cells were investigated in this study. All these cells have the same CIGS absorber layer and differ (a) by the thickness of the buffer layer (CdS), or (b) by the contact on the CdS (none, sputtered ZnO, or evaporated Al). For all samples the CdS buffer layer was directly deposited by CBD on the absorber with various deposition time and then different thickness according to the standard recipe [8]. The deposition time was eight minutes for sample 1, two times

eight minutes for sample 2 and four times eight minutes for sample 4. These three samples are ZnO free, the top aluminum contact was directly deposited on CdS layer. To distinguish between the contributions of CdS/CIGS and Al/CdS interfaces to the admittance spectra, we compared our results with those of another serie that underwent ZnO window layer deposition (sample 2' which is equivalent to sample 1).

The same samples without the ZnO layers or without the Al layer (i.e. with bare CdS) were investigated by Kelvin probe to measure the evolution of the barrier height. The second set of samples (after ZnO layer deposition) was tested under AM1.5 100mW/cm² ELH equivalent illumination for performance evaluation (samples 1', 2', 3' and 4').

XPS measurements were performed using a VG 220i XL system. High-resolution XPS conditions have been set e.g. constant analyzer energy mode with 20 eV as pass energy, and monochromatic Al K_α X-Ray excitation giving high-resolution spectra. Ar⁺ ion gun has been used to perform the CdS/CIGS interface profiling through a very thin remaining CdS layer (d<1nm).

3. RESULTS AND DISCUSSION

3.1 Admittance spectroscopy studies

As an example, Figure 1 shows for sample 1 the capacitance spectra versus frequency and temperature. The same kind of spectra were obtained for samples 2 and 4. Figure 2 shows the Arrhenius plot of the quantity ω/T^2 where ω is the emission frequency of the main defect level, as derived from the inflexion point of the capacitance spectra and Figure 3 shows the corresponding derived density of states. The derived gap states of the three samples are reported in Table I along with their respective CdS time deposition.

We observe from Figure 2 that samples 1 and 2 exhibit a defect (defect A) with an activation energy around 50 meV below the conduction band. The same defect A was observed on sample 2' with an activation energy around 50 meV and a peak density of states of $3 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$. Defect A is a CdS/CIGS interface defect [9].

Sample 4 exhibits a defect (defect B) with an activation energy around 150 meV.

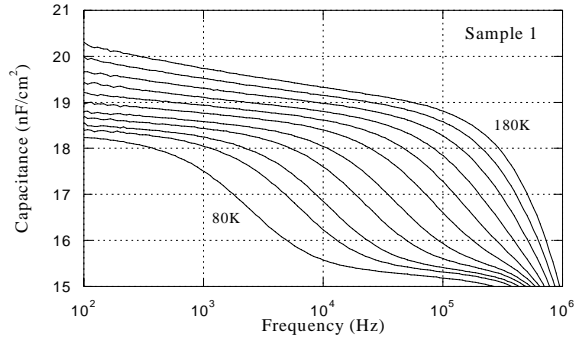


Figure 1 : Capacitance spectra versus frequency and temperature for sample 1. The temperature varies from 80 K to 180 K with 10 K step : the signature of one defect level is derived from numerical processing of these spectra.

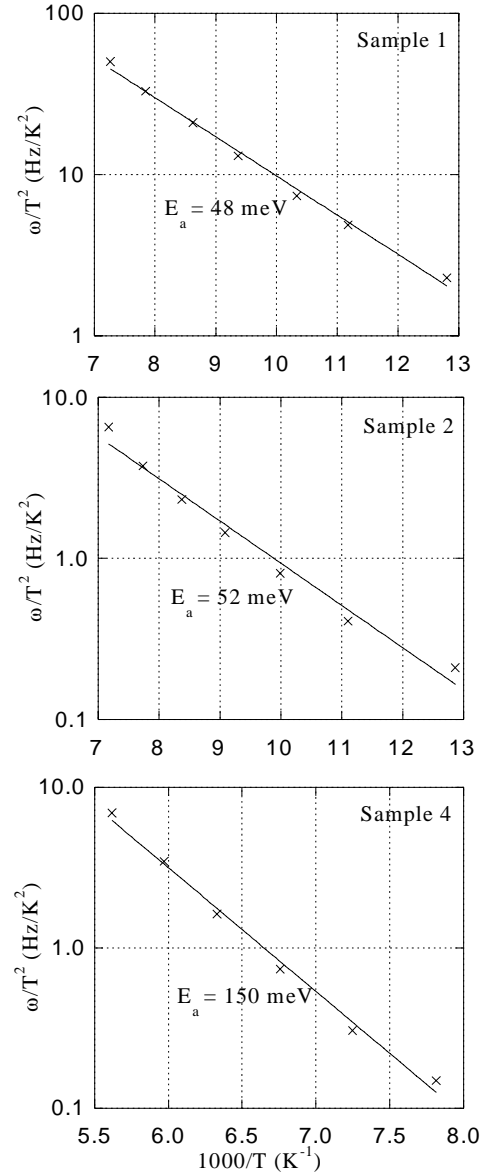


Figure 2 : Arrhenius plots of ω/T^2 for samples 1, 2 and 4. $\omega(T)$, emission frequency of the main defect level, is derived from the inflexion point of the capacitance spectra.

We note from Figure 3 and table I that the defect A density of states strongly decreases from sample 1 to sample 2 and that the defect B density of states in sample 4 is a little bit lower than that of defect A in sample 2. For defect A, the density of states strongly decreases with CdS layer thickness which we explain by the enhanced passivation for this defect. The defect B is probably located within a slightly extended CdS interface layer of about 7 nm inside the CIGS layer and newly formed after increasing the CdS layer thickness (see section 3.3).

Sample	DT (min.)	Activation energy (meV)	Peak density ($\text{cm}^{-3} \text{eV}^{-1}$)
1	8	48	7×10^{17}
2	2×8	52	3.5×10^{15}
4	4×8	150	1.5×10^{15}
2'	6	54	3×10^{17}

Table I : CdS deposition time (DT) and gap states parameters of the investigated samples.

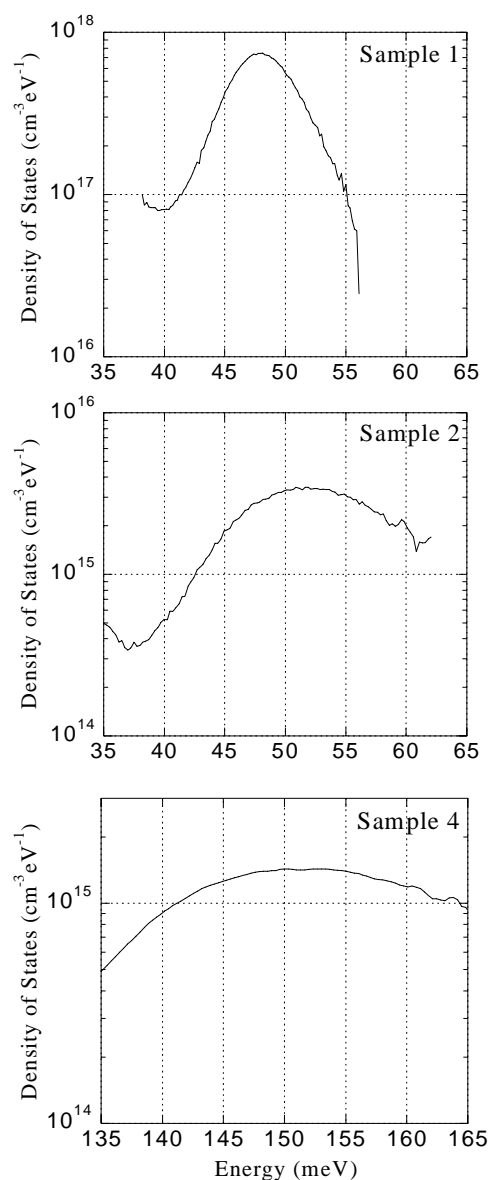


Figure 3 : Defect density of states versus energy for samples 1, 2 and 4.

3.2 Electrical characteristics under illumination

In the two series of samples, the same trends were observed. The photopotential was found to increase with the thickness of CdS, both under red (i.e. wavelength above 800 nm) and white light illumination. The results for the first series of samples are reported in table II.

Consistently with the results discussed elsewhere [10], the photopotential was found lower with white light due to the surface barrier of CdS and to trapping in CdS.

Both photopotentials exhibit an increasing trend when the CdS deposition time increases showing the influence of trapped charge at CdS/CIGS interface and in the CdS layer.

The increased photopotential can be attributed to an increased barrier at the CIGS/CdS interface and/or to an improved passivation of this interface.

A change in barrier height means that the Fermi level is not pinned at that interface, after CdS CBD deposition.

Sample	DT (min.)	Ph. white (meV)	Ph. red (meV)
1	8	125	130
2	2×8	260	320
3	3×8	265	340
4	4×8	255	370

Table II : comparison of Photopotentials (Ph.) of samples 1-4 under white light and filtered red light (>800nm).

In a second series of experiments, ZnO was deposited on top of the CdS layers, and device performances were measured under 100 mW/cm^2 (ELH) illumination. Results are reported in table III. Again the same trend is observed where V_{oc} increases rapidly and then flatten off with CdS thickness.

Under 100 mW/cm^2 illumination, the photocurrent of the devices made with samples 1' to 4' was found to decrease slightly (from 32.4 mA/cm^2 for sample 1' to 30.5 mA/cm^2 for sample 4') as expected from an increasing absorption in the CdS layer.

3.3 High resolution XPS studies

XPS profiling of CdS/CIGS structure has been performed on system obtained without initial treatment of the CIGS surface. The CdS layer deposition time was 6 minutes i.e. corresponding to a thickness close to 50 nm. Attention has been brought to the surface preparation and to the buried interface CIGS/CdS. Buried interfaces were studied after gradual Ar^+ sputtering. The interfacial profile is given in Figure 4.

Sample	DT (min.)	V _{OC} (meV)	FF (%)
1'	3	480	40
2'	6	550	69
3'	12	550	70
4'	18	550	67

Table III : comparison of the cell performances under white light for samples of the second serie.

The interface composition presents a variation corresponding to a gradual interface, close to 7 nm. At the interface, we observe an increasing oxygen quantity, probably due to the presence of a Cd(OH)₂ compound. We can note that we do not observe diffusion of Cu, In, Ga or Se elements in the CdS layer. However, at the interface, we obtain a In/Se ratio close to 1, indicating a strong depletion of Se, probably due to an exchange between Se and S of CdS layer. This is further supported by the shift of the In3d_{5/2} peak to 445.5 eV for the buried interface to 445.0 eV in the CIGS bulk. It is noteworthy that the binding energy of 445.5 eV corresponds to In₂S₃ compound. We observe also a significant shift of the Cu2p_{3/2} peak from 933.2 eV (buried interface) to 932.8 eV (bulk) indicating a modification of the Cu chemical environment, probably related to the formation of a Cu-S compound.

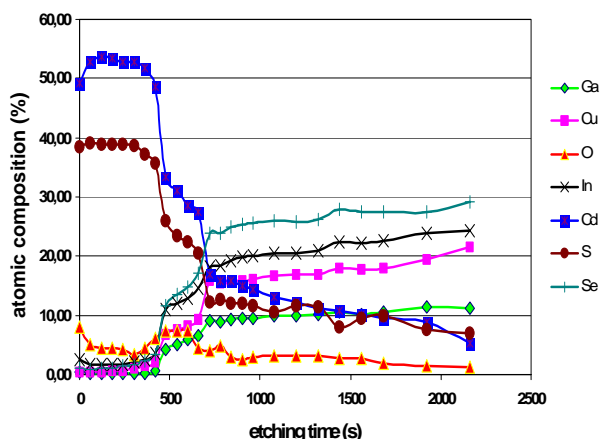


Figure 4 : XPS profile of the buried CIGS/CdS interface of sample 2'.

4. CONCLUSION

We have presented Capacitance Spectroscopy, XPS and Kelvin probe measurements of CdS/CIGS structures with various CdS thickness. Admittance spectroscopy shows two CdS/CIGS interface defects. The density of states of the first one decreases with increasing CdS layer thickness. The second defect is probably located within a slight extended CdS interface layer of about 7 nm, newly formed after the increasing CdS layer thickness according to XPS results. Admittance Spectroscopy and Kelvin Probe measurements show that the CdS thickness has an important influence on device performances.

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