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# Extraction of small-signal equivalent circuit for de-embedding of 3D vertical nanowire transistor

Bruno Neckel Wesling<sup>1</sup>, Marina Deng<sup>1</sup>, Chhandak Mukherjee<sup>1</sup>, Magali de Matos<sup>1</sup>, Abhishek Kumar<sup>2</sup>, Guilhem Larrieu<sup>2</sup>, Jens Trommer<sup>3</sup>, Thomas Mikolajick<sup>3</sup>, Cristell Maneux<sup>1</sup>

<sup>1</sup> IMS, University of Bordeaux, UMR CNRS 5218, Bordeaux INP, Talence, France, email: bruno.neckel-wesling@u-bordeaux.fr

<sup>2</sup> LAAS-CNRS, UPR 8001, CNRS, University of Toulouse, Toulouse, France

<sup>3</sup> NaMLab gGmbH, 01187, Dresden, Germany

## 1. Abstract

In this paper, we present an improved methodology to extract the small-signal electrical equivalent circuit of the parasitic elements using RF test structures for a 3D vertical nanowire transistor technology. The methodology is based on the extraction of the distributed parasitic elements from an open structure for which on-wafer S-parameter measurements were carried out up to 40 GHz. The electrical equivalent circuit of the passive device was then used for de-embedding of the transistor S-parameters for extraction of intrinsic small-signal parameters such as the gate capacitances.

## 2. Introduction

In the context of emerging technologies for new computing paradigms such as neural networks, vertical nanowire field effect transistors (VNWFET) are a promising technology owing to their naturally 3D architectures [1]. For the circuit design using such a 3D emerging technology, it is necessary to build new and accurate compact models to capture the static and dynamic behavior of the device [2]. However, on-wafer test structures of the devices contain parasitic elements introduced by the RF pads and interconnects that are necessary to probe the devices under test (DUT). The standard procedure to characterize the parasitic effects of a device at high frequencies can be divided into two parts. Firstly, the measurement system needs to be calibrated so that the reference plane is at the probe tips. This can be done using standard calibration techniques such as SOLT (Short-Open-Load-Thru). At this point, all the parasitic elements associated with the pads and interconnects are still included in the measurements. In the second step, S-parameters of the open and short structures are measured which are then used to remove the parasitic elements external to the DUT, through a subtraction process known as de-embedding [3].

Although the process of parasitic extraction is widely used in technologies targeted for high frequency applications, this process can also be applied for technologies such as the VNWFET that are mainly designed for computing applications to improve the modeling accuracy, which normally just relies on DC measurements [1]. Moreover, an accurate modeling of the parasitic elements allows the designer to optimize the 3D layout of the logic circuits and interconnects, thereby improving performance metrics such as compactness and energy-delay product of the technology.

In this paper, we present an elaborate methodology for extracting the extrinsic interconnect parasitic network associated with the unconventional vertical and inherently 3D test structures of the VNWFETs. In the rest of the paper, results from the RF measurements and electro-magnetic (EM) simulations are used for the extraction

of parasitic elements of the electrical equivalent circuit of an open test structure. Finally, we show the small-signal capacitances of a VNWFET extracted using two different de-embedding processes.

### 3. Methodology

For de-embedding, open structures were fabricated using the same process and on the same wafer as the VNWFETs [4]. The open device consists of all interconnects except for the vertical nanowires. Fig. 1(a) shows the open structure containing the RF pads, where the absence of the active device can be observed. For the demonstration of the de-embedding process, a VNWFET consisting of 81 nanowires in parallel with a diameter of 17 nm each was selected. A drawing of a full transistor can be seen on Fig 1(c).

#### 3.1. On-wafer S-parameter measurements

The on-wafer S-parameters were measured using a Vector Network Analyzer (VNA) from Rohde & Schwarz up to 40 GHz, and a source monitor unit, Agilent 4142B, connected via a bias-tee. The DUTs were contacted using Ground-Signal-Ground (GSG) probes with a pitch of 100  $\mu\text{m}$  following a SOLT calibration. A second test bench that allows S-parameter measurements up to 110 GHz, Agilent® E8361 PNA, was used for the open device to ascertain the credibility of the measurements.

#### 3.2. Electromagnetic simulation

The 3D view of the open device constructed for EM simulations is shown in Fig. 1(b). The ADS-Momentum EM simulator was used for the computation of the S-parameters of the provided layout. To eliminate manual errors, the layout was imported into ADS using the same GDSII file that was used for the fabrication process. The electrical properties of the material layers were set based on the fabrication process [4]. A cross-section of the materials stack is shown in Fig. 1(c). In Fig. 3, a comparison between the measured and the EM simulated S-parameters of the open device is shown. The EM simulation results exhibit very good agreement with the measured data up to 40 GHz. Considering that an open structure can be represented by a  $\pi$ -network consisting of three capacitors, the values of these capacitances were extracted from the Y parameters, which were obtained using the standard S to Y parameter transformation method. The capacitances are presented in Fig. 4 for both measurements and EM simulation. The capacitances obtained from the second measurement setup that reaffirmed the measurement results are presented as C1\_MEAS\_110G, C2\_MEAS\_110G and C12\_MEAS\_110G respectively. The capacitance C1 extracted from the EM simulation showed good agreement with the measurements beyond 10 GHz. Below 10 GHz, discrepancies can be observed that might be related to the limitation of EM simulation in reproducing all the details of the fabricated structures. This indicated that the measurement of the open device below 10 GHz cannot be modeled as a simple  $\pi$ -network. A more complete and lumped model was then investigated taking into account the EM simulation of different sections of the complete open structure.

#### 3.3. Distributed equivalent circuit of the transistor interconnects

To construct the small-signal equivalent circuit (SSEC) of the open device, EM simulations of different sections of the complete structure were performed to estimate their individual contributions. The pad was considered as an LC network in series with a contact resistance and a  $\pi$ -network was used to model the coupling capacitances between the gate, drain, and the source accesses. The pad capacitance and impedance are estimated from the

EM simulations of the virtual OPEN\_PAD and SHORT\_PAD structures presented in Fig. 5 (a) and (b), respectively. The coupling capacitances are obtained from the OPEN\_DUT shown in Fig. 5 (c). A figure of the substrate used on ADS for the EM simulation is shown on Fig. 5 (d). The extracted elements are then combined to construct the distributed circuit ‘model1’.

The capacitance C1\_MODEL1 in Fig. 6, extracted from ‘model1’, does not match well with the measurement data. This means that not all parasitic effects were accounted for, and a more detailed circuit is needed [5]. Analyzing the device layout and the fabrication process one can identify that substrate parasitic effects might be present due to (i) a low silicon substrate resistivity [4] and (ii) the absence of a ground shield metal underneath the signal pads [6]. The substrate parasitic elements introduce a lossy path,  $C_{\text{pad2}}\text{-}R_{\text{sub}}\text{-}C_{\text{pad3}}$ , shown in Fig. 7 along with a fringe capacitance  $C_{\text{pad1}}$  [7]. The final SSEC is presented in Fig. 7, denoted as ‘model2’. The values of the components in the distributed circuit were a mix of values estimated mathematically from the physical dimensions and material properties of the device as well as from EM simulations. Finally, the capacitance C1\_MODEL2 extracted from the SSEC ‘model2’, presented in Fig. 6, shows an excellent agreement with the measurement.

### 3.4. Transistor de-embedding

Two different de-embedding methods were used in this work. The first one is a simple open de-embedding process where the Y parameters of the open device are subtracted from those of the transistor, referred to as OPEN\_deemb. The second approach is based on the methodology described in [8], referred to as the access-modeling based de-embedding (AM\_deemb) henceforth. For this, ABCD matrices were used to remove the gate and drain parasitic access contributions, for which the matrix  $[A_{\text{transistor\_meas}}]$  of the complete transistor measurement was multiplied by the inverse of MATRIX  $A_{\text{gate}}$  and MATRIX  $A_{\text{drain}}$ , obtained from the equivalent circuit in Fig. 8,

$$[A_{\text{transistor1}}] = [A_{\text{gate}}]^{-1} \times [A_{\text{transistor\_meas}}] \times [A_{\text{drain}}]^{-1} \quad (1)$$

The Y-parameters of the  $C_{\text{GD\_access}}$  (Fig. 8) were then subtracted from the Y parameters obtained from the ABCD-to-Y transformation of matrix  $[A_{\text{transistor1}}]$  in (1) as,

$$[Y_{\text{transistor2}}] = [Y_{\text{transistor1}}] - [Y_{C_{\text{GD\_access}}}] \quad (2)$$

Y-to-Z parameter transformation is then performed on  $[Y_{\text{transistor2}}]$  and subsequently the impedance  $L_{\text{S\_access}}$  (Fig. 8) was removed by subtracting its Z-parameters:

$$[Z_{\text{transistor\_deemb}}] = [Z_{\text{transistor2}}] - [Z_{L_{\text{S\_access}}}] \quad (3)$$

The final transistor S parameters were obtained from the transformation of the  $[Z_{\text{transistor\_deemb}}]$  parameters obtained from eq. (3).

## 4. De-embedding results

The gate and drain capacitances,  $C_{\text{GS}}$  and  $C_{\text{DS}}$ , obtained from the de-embedded Y-parameters of the transistor at a  $V_{\text{GS}}$  of -1 V and a  $V_{\text{DS}}$  of -0.1 V are shown in Fig. 9. The data was truncated at 20 GHz since the VNWFET has no RF gain at higher frequencies and the measurement noise becomes dominant. The  $C_{\text{GS}}$  obtained from the AM\_deemb has a mean value of 37 fF compared with 48 fF for the OPEN\_deemb. The  $C_{\text{DS}}$  shows a flat value between 5 and 12 GHz for the AM\_deemb, while an unphysical negative value was obtained from the OPEN\_deemb. The  $C_{\text{DS}}$  frequency increase above around 12 GHz is a indicator of the limitation in the de-

embedding method, even though the new proposed method provides more physical results compared with the conventional method.

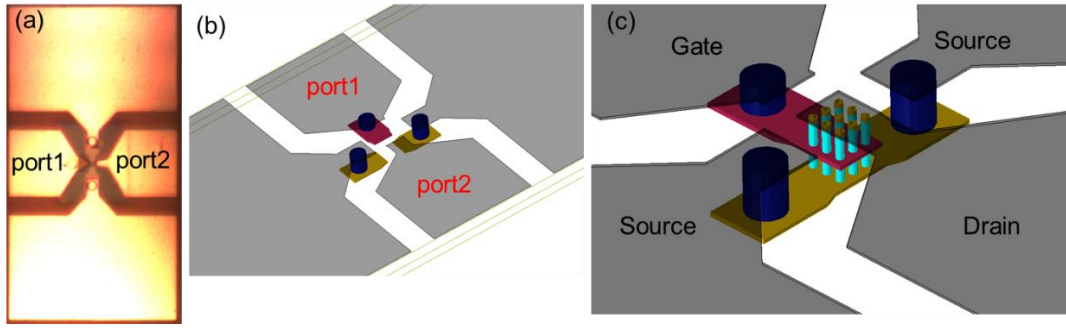
## 5. Conclusions

In this work, the small-signal equivalent circuit of the VNWFET interconnects was achieved by using the measurements from the open structure and predictive EM simulation. Adding the substrate parasitic network to the distributed SSEC is crucial for higher accuracy of de-embedding since the capacitance of the open device is more than the intrinsic capacitance of the transistor. The extraction of capacitances could be achieved up to 20 GHz, demonstrating a promising efficiency of our proposed method. In the future scope of this work, the extracted values of the gate capacitances will be verified from 3D TCAD simulation of the transistors.

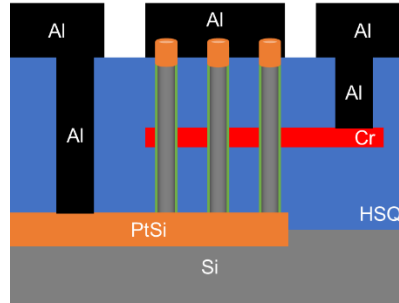
## Acknowledgments

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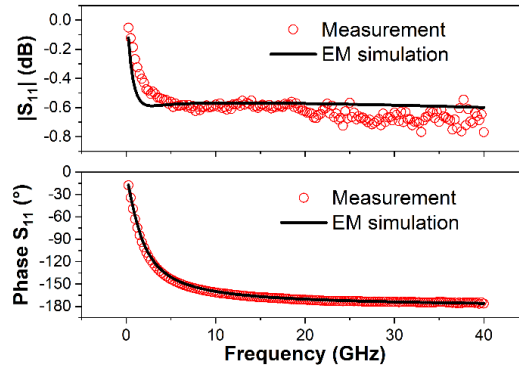
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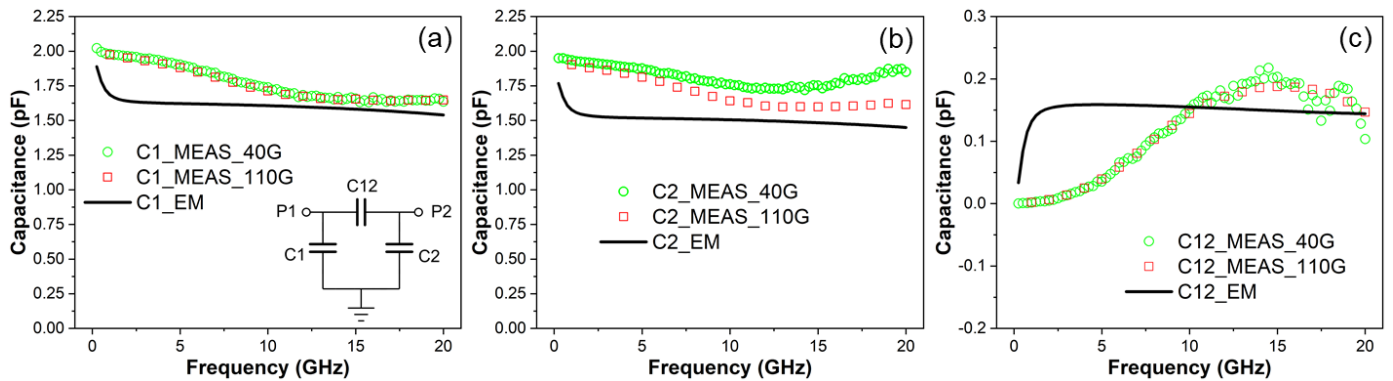
**Figure 1:** (a) Open structure for S-parameters measurements, (b) a 3-D view of the open structure created using ADS MOMENTUM and (c) the drawing of the VNWFETs showing the nanowires.



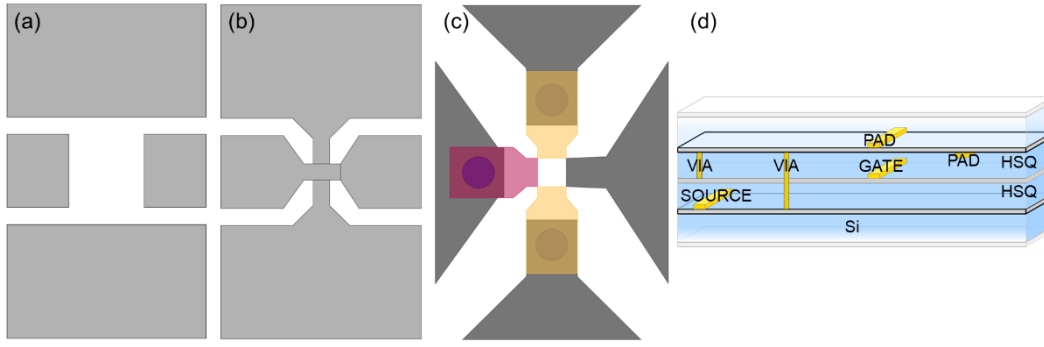
**Figure 2:** Drawing of the cross-section of the transistor presenting the stack of materials.



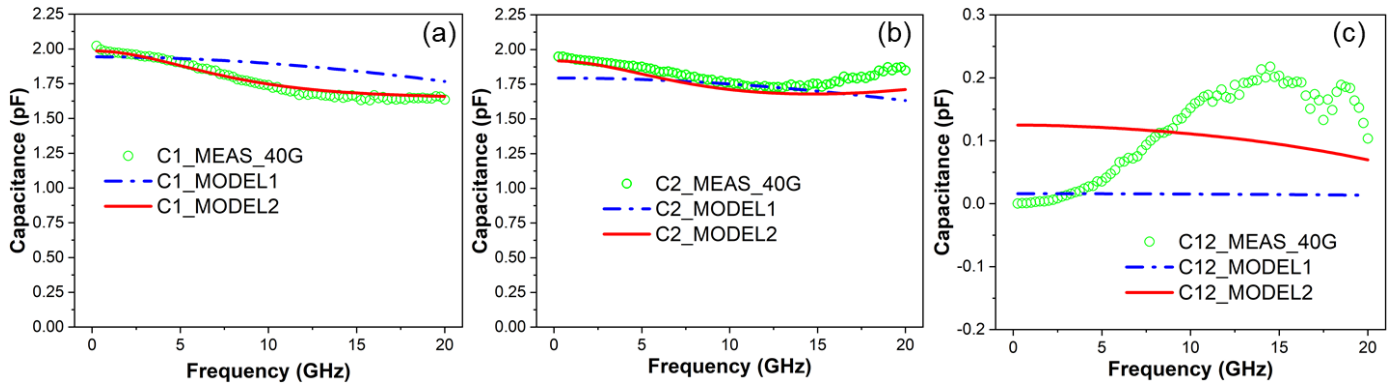
**Figure 3:** Comparison of S-parameters from measurements and electromagnetic simulation for the open test structure.



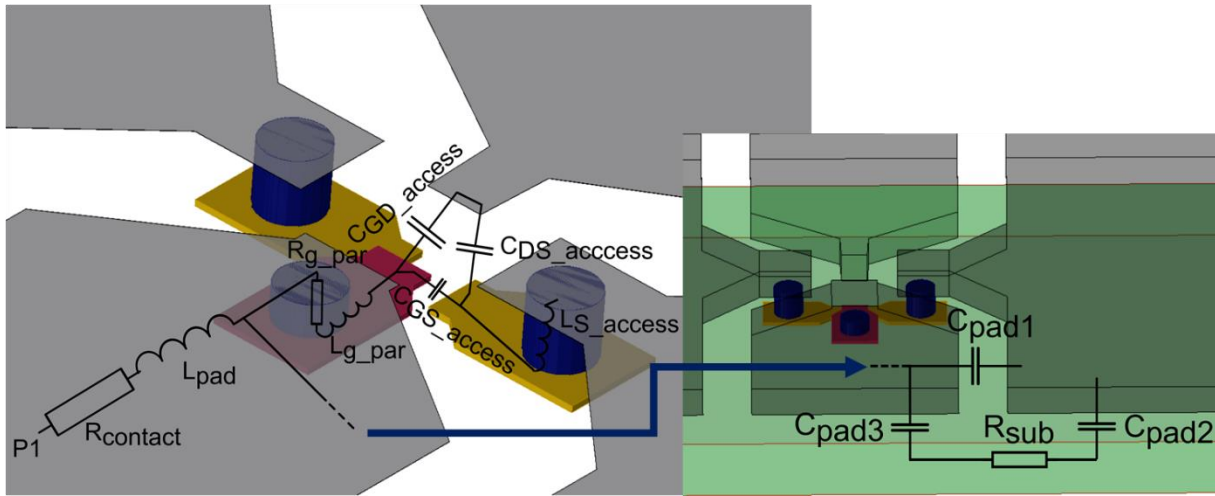
**Figure 4:** Open structure capacitances extracted from measurements and EM simulation up to 20 GHz. (a) C1, (b) C2 and (c) C12. The inset in (a) shows the equivalent  $\pi$ -network.



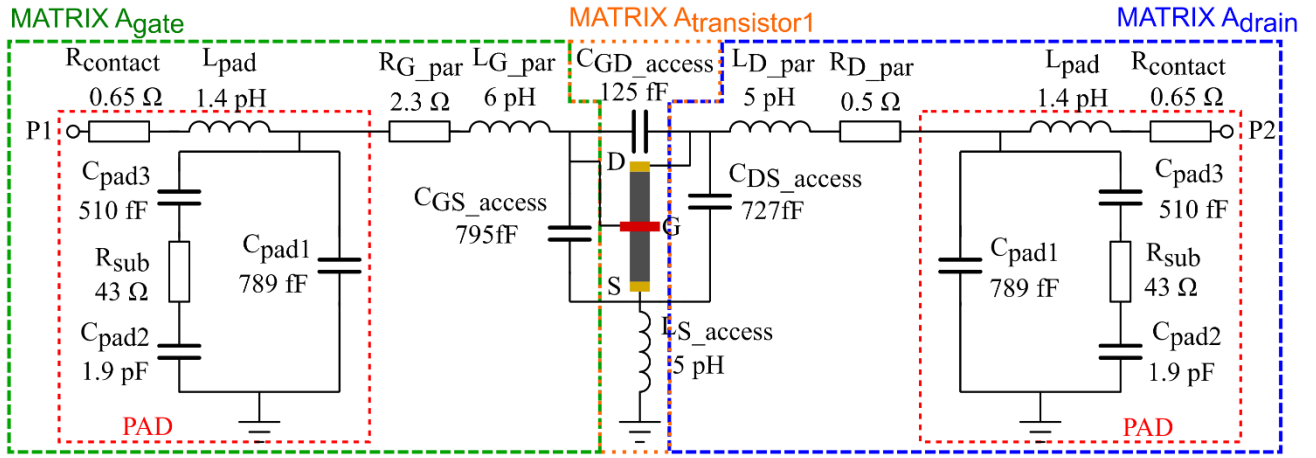
**Figure 5:** Virtual structures for the EM simulation, a) OPEN\_PAD, b) SHORT\_PAD, c) OPEN\_DUT and (d) the substrate definition on ADS for EM simulation.



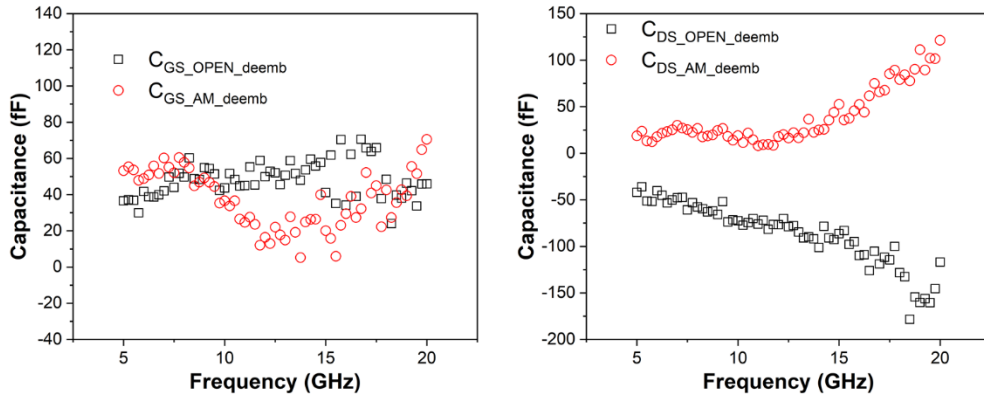
**Figure 6:** Capacitances as a function of frequency extracted from measurements and electrical simulation up to 20 GHz. (a) C1, (b) C2 and (c) C12.



**Figure 7:** 3D view of the distributed model.



**Figure 8:** Electrical equivalent circuit representing the parasitic elements obtained from the open test structure that is used for the de-embedding of VNWFET.



**Figure 9:** Small signal capacitances as a function of frequency for the de-embedded transistor at a  $V_{GS} = -1V$  and  $V_{DS} = -0.1V$ .