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# Multiscale compact modelling of UTC-photodiodes enabling monolithic terahertz communication systems design

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**Abstract:** Due to the continuous increase in data traffic, it is becoming imperative to develop communication systems capable of meeting the throughput requirements. Monolithic Opto-Electronic Integrated Circuits (OEICs) are ideal candidates to meet these demands. With that in mind, we propose a compact and computationally efficient model for Uni-Traveling Carrier Photodiodes (UTC-PDs) which are a key component of OEICs for their high bandwidth and RF output power. The developed compact model is compatible with existing SPICE design software, enabling the design of beyond 5G and terahertz (THz) communication circuits and systems. By introducing detailed physical equations describing, in particular, the dark current, the intrinsic series resistance, and the junction capacitance, the model accurately captures the physical characteristics of the UTC-PD. The model parameter extraction follows a scalable extraction methodology derived from that of the bipolar and CMOS technologies. A detailed description of the de-embedding process is presented. Excellent agreement between the compact model and measurements has been achieved, showing model versatility across various technologies and scalability over several geometries.

**Keywords:** uni-traveling carrier photodiode; compact model; SPICE; terahertz; de-embedding; on-wafer characterization; bandwidth.

## 1. Introduction

Data traffic is surging with the emergence of new applications such as virtual and augmented reality, autonomous driving and Internet of Things (IoT) [1]. To meet these new requirements in terms of bandwidth and power level, new high-speed communication technologies must be developed. Indeed, the minimum required bandwidth for a high-speed communication system must reach several tens of GHz, which requires an even higher carrier frequency in the THz range (0.1-10 THz). To manage this data traffic, monolithic integration of Opto-Electronic Integrated Circuits (OEICs) (see Figure 1) is a viable solution and very promising among the new emerging THz technologies [2]. The monolithic integration of optical and high-speed electronic devices on the same InP substrate minimizes the signal propagation losses between the two device

types. The use of a common substrate could also offer a more compact footprint, simplified testing and reduced costs [3,4].

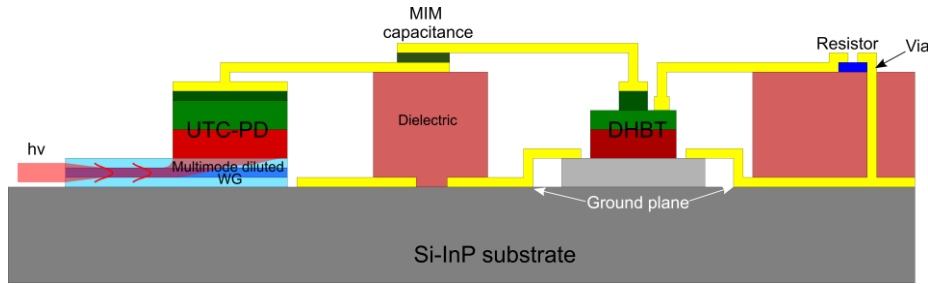


Figure 1. Schematic view showing future monolithic integration of the Uni-traveling-Carrier photodiodes (UTC-PD) with Double Hetero junction Bipolar Transistors (DHBT) to be used, for instance, in integrated THz transceivers.

The architecture of OEI circuits and systems varies across application types and can rapidly become complex. The need for a co-design and verification infrastructure for such systems capable of supporting billions of devices has therefore become imperative. In addition, co-design is highly dependent on the accuracy of compact models of each block. The compact models are in fact complete physical models converted into simpler and easy-to-solve analytical equations through reasonable assumptions and approximations. These models are commonly transcribed into programming languages such as Verilog-A, compatible with SPICE circuit design tools and software (Cadence, Mentor Graphics, etc.). In electronics, compact models have already reached a significant degree of maturity and computational efficiency over the last few decades. To enable design of high-speed integrated communication technologies, the photonics community has also started to develop compact models for optoelectronic devices, in order to unify electrical, photonic and electromagnetic modeling using the same existing software design tools [5-7]. It is important to note that a scalable compact model offers two-fold benefit. At the device level, a scalable compact model is a powerful tool for predicting performances for varying device geometries, it also provides a quick feedback on the impact of each technological and physical parameter. At the circuit/system level, compact models enable optimization of bias points and interconnections between photonic and electronic components, providing guidelines for predicting the performances of new OEIC designs.

One of the key components capable of bridging these two worlds of optics and electronics is a photodiode. It allows to recover the information carried by an optical signal in the form of electrical information. There are several photodiode technologies such as conventional PIN photodiodes and avalanche photodiodes. The uni-traveling carrier photodiodes (UTC-PD) represent the most promising one. In particular, UTC-PDs have been widely studied for ultrafast optoelectronic applications, especially for the generation of THz signals [8]. High performances have been reported demonstrating bandwidths of more than 600 GHz reached with good power levels [8]. By relying mainly on electron transport, this architecture significantly improves the bandwidth and the power of the UTC-PDs compared to the conventional PIN photodiodes. As a result, UTC-PDs have become a key element in the convergence of electronic and photonic technologies in the millimeter wave band [9,10].

With the intention of developing a SPICE compatible model for UTC-PDs, a first compact modeling effort was presented in [11]. This compact model has been validated on type-I heterostructure UTC-PDs. Moreover, it is compatible with the Verilog-A design tools. In a previous study, a validation of the HiCuM/L2 compact model, developed mainly for SiGe HBT, on III-V type I (InGaAs/InP-based) and type II (GaAsSb/InP-based) double heterojunction

bipolar transistors (DHBTs) [12,13] has also been presented in a first attempt to combine the two technological paradigms. Since UTC-PDs and DHBTs could share the same InP substrate and possibly base-collector epitaxial heterostructure, this combined modeling approach can pave the way for the design of monolithic integrated OEICs.

In continuation of previous works, this study presents improvements of the first UTC-PD compact model. We have introduced more physical equations describing, in particular, the dark current, the intrinsic series resistance and the junction capacitance as well as their dependence on the applied bias. As a consequence, the new model now takes into account more material parameters such as doping, mobility and permittivity. Scaling laws have also been implemented by analyzing the geometry of the UTC-PDs. In addition, new accurate de-embedding methods are proposed to overcome the limitations of conventional methods. A scalable parameter extraction methodology is presented for type I and type II heterostructure UTC-PDs, i.e. InGaAs/InGaAsP and GaInAsSb/InP, respectively, providing very good results over several geometries, bias points and frequencies. It is important to note that the model validation does not focus primarily on the type of heterostructure but on the design of the UTC-PDs, test structures as well as the frequency used in the study.

This paper is organized as follows: section 2 provides the formulation of the improvements that have been implemented in the new model and presents the parameter extraction methodology. Section 3 reports the compact model validation and the results, including the extraction of the junction capacitances, intrinsic series resistances, current parameters, and the bandwidths. Finally, Section 4 concludes the study and discusses future perspectives.

## 2. Compact model development

### 2.1. Model description

The UTC-PD compact model can be represented by an equivalent circuit with three terminals. Among these terminals, two are for the electrical part and one for the optical input signal. The model translates the analytical equations based on the physics of UTC-PDs into an equivalent electrical circuit representation. Figure 2a shows a SEM micrograph taken after the UTC-PD mesa formation. Figure 2b illustrates the schematic of an intrinsic UTC-PD mesa structure, showing different epitaxial layers. On this schematic, the small signal electrical model is superimposed depicting different electrical elements of the equivalent circuit representation. The active region consists principally of the epitaxial p-doped absorption layer and a slightly n-doped collection layer. The electrical representation of this region is composed of a junction capacitance,  $C_j$ , which describes the absorber-collector junction. In parallel to this capacitance, three current sources model the forward current, the reverse current and the photocurrent [14], respectively. Note that here the photocurrent implementation in Verilog-A is more complex than simple current source representations since it includes transfer functions (Figure 2c). In series with the active region, there are resistances representing the resistive contribution of the non-depleted part of the collector, the sheet resistances and the resistances of the metal contacts. The device can be biased via the doped P+ and N+ contacts at the top and the bottom, respectively. On both sides of the mesa, there are the access lines, which are connected to the Ground-Signal-Ground (GSG) pads (Figure 2d).

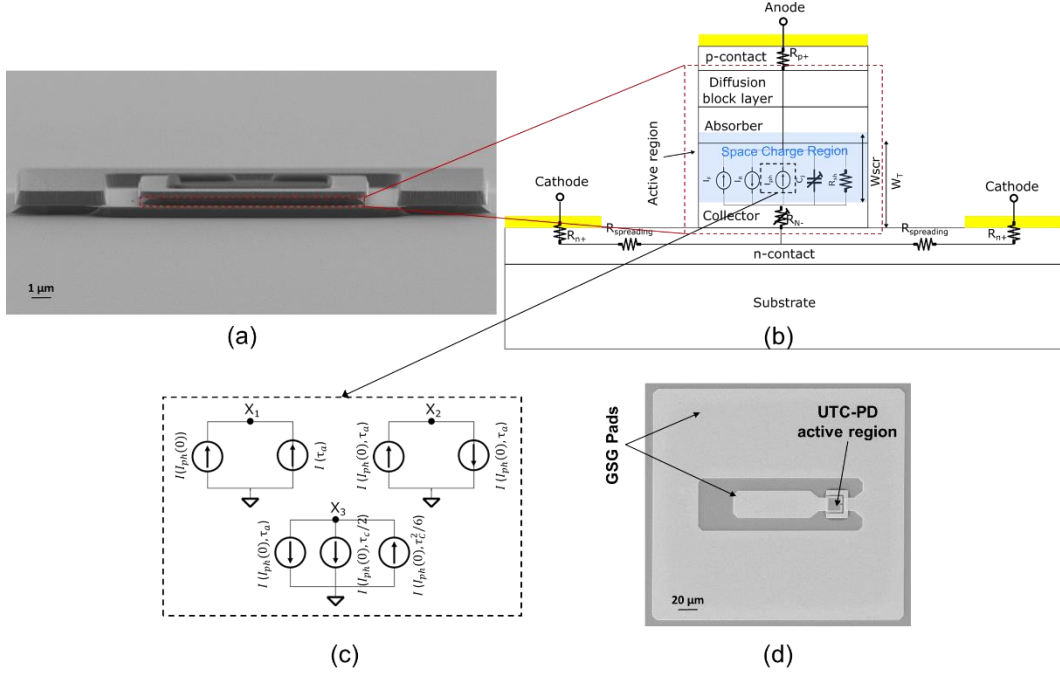


Figure 2. (a) SEM micrograph of a GaInAsSb/InP UTC-PD (b) Schematic of the intrinsic mesa UTC-PD showing the location of the equivalent circuit elements (c) the Verilog-A topology of the UTC-PD photocurrent transfer function (d) Top-view SEM micrograph of a GaInAsSb/InP UTC-PD connected to the GSG pads.

## 2.2. Model formulation

The first compact model developed in [11] serves as the starting point of the modeling framework presented in this work. In order to make the model versatile across different technologies and geometries, improvements in model equations and implementations have been made. In the following sections, the details of the principal improvements are presented.

Firstly, the direct current contribution,  $I_F$ , has been slightly modified to take into account the two operating regimes: low and high injections [15]. Thus, the direct current equation becomes the following:

$$I_F = \frac{I_D}{1 + \sqrt{\frac{I_D}{I_K}}} \quad (1)$$

Here  $I_D$  is the classic diode equation [16] and  $I_K$  is the knee current parameter that signifies the transition between the medium and high injection regimes.

Among other improvements, we incorporate a more detailed description of the series resistances through decorrelation of the resistive contributions as functions of the applied bias and device geometry. In the first version of the model, only one series resistance, independent of the bias voltage, was considered. It reflects the resistance of the contacts and the spreading resistance. However, the thickness and the doping level of the collector varies from one technology to another (usually  $N^-$  doped). When the collector is not fully depleted, an additional bias-dependent resistance appears which, when the collector is fully depleted, becomes negligible. In our new model, therefore, these two contributions are separated. The dependence of the resistance of the active region,  $R_{N^-}$ , on the applied voltage,  $V_d$ , can be expressed as follows:

$$R_{N^-}(V_d) = R_{N^-}(0) \frac{w_T - w_{scr}(V_d)}{w_T - w_{SCR0}} \quad (2)$$

Where  $R_{N^-}(0)$  is the resistance of the undepleted collector at *zero* bias,  $w_T$  is the width of the collector and  $w_{SCR0}$  is the width of the space charge region at *zero* bias.  $w_{scr}(V_d)$  and  $R_{N^-}(0)$  can be expressed with the following set of equations [17]:

$$w_{scr}(V_d) = w_{scr0} \left(1 - \frac{V_d}{V_j}\right)^{M_{mr}} \quad (3)$$

$$R_{N^-}(0) = \frac{w_T - w_{SCR0}}{q \cdot \mu \cdot N^- \cdot A} \quad (4)$$

Where  $V_j$  is the junction potential and  $M_{mr}$  is the grading coefficient at medium reverse bias of the  $P-N^-$  junction,  $q$  is the electronic charge,  $\mu$  is the electron carrier mobility in the collector,  $N^-$  is the doping concentration in the collector and  $A$  is the UTC-PD active area.

The classical model of the bias-dependence of the junction capacitance has evolved into a more mature form in the HiCuM/L2 model. We refer here mainly to the formulation for the base-collector junction. Considering different thicknesses, the collector may not be completely depleted at equilibrium. In this case, the junction capacitance follows the conventional model [17] until the collector is completely depleted, the voltage drop becomes small due to the high doping level of the waveguide (or n-contact). In reverse bias, the model of the junction capacitance thus consists of two contributions:

$$C_{jT}(V_d) = C_{jm}(V_d) + C_{jl}(V_d) \quad (5)$$

Where the first contribution,  $C_{jm}(V_d)$ , represents the contribution at medium reverse bias, described by the classical equation:

$$C_{jm}(V_d) = C_{jom} \left(1 - \frac{V_d}{V_j}\right)^{-M_{mr}} \quad (6)$$

The second part,  $C_{jl}(V_d)$ , represents the contribution around and beyond the condition of complete depletion of the collector. It can be expressed as follows:

$$C_{jl}(V_d) = C_{jol} \left(1 - \frac{V_d}{V_j}\right)^{-M_{lr}} \quad (7)$$

Where  $C_{jol}$  and  $M_{lr}$  can be calculated internally from the punch-through bias,  $V_{PT} = \frac{qN^-}{2\epsilon_{collector}} \cdot W_{collector}^2$  and  $M_{mr}$  respectively [18].

In standard compact modeling practices, the time derivatives of the charges are used for the capacitance model. Thus, in our case, the two contributing charges of the capacitance model are multiplied by smoothing functions (or weights) that allow a continuously differentiable transition across the two adjacent bias regions.

Moreover, in our model we also calculate the electric field,  $E_{max}(v_d)$ , at the input of the collector which is included in the expressions of the tunneling currents. We can then use these expressions to calculate the transit time of electrons in the collector,  $\tau_c$ , from their drift velocity, which can be expressed by the following empirical expression [19]:

$$v(E) = v_{sat} \left(1 + \frac{\frac{E}{E_{scale}} - 1}{1 + A \left(\frac{E}{E_{scale}}\right)^t}\right) \quad (8)$$

Where  $v_{sat}$  is the saturation velocity,  $E_{scale} = \frac{v_{sat}}{\mu}$ ,  $A$  and  $t$  are parameters to be determined from the material used. The parameters of eq. (8) can be determined from a fit on the data of each material used.

### 2.3. Parameter extraction methodology

The extraction method has been developed in accordance with the standard extraction flow used for bipolar transistor technologies. To begin the extraction process, an initialization of the physical and technological parameters is necessary. Next, a sequence of measurements and parameter extractions are followed that leads to the extractions of the intrinsic and extrinsic parameters as shown in the flowchart in Figure 3.

The measurement of one-port  $S$ -parameters of the test structures are first measured to extract the electrical equivalent circuit elements of the RF pads and access lines. It is important to note that the design of the test structures can vary from one technology to another. Therefore, the de-embedding method must be adapted to the available test structures. Subsequently, one-port  $S$ -parameter measurements at various biases followed by a de-embedding process allow accessing the intrinsic  $S$ -parameters of the UTC-PDs. By converting these  $S$ -parameters to  $Y$  or  $Z$ -parameters, the elements of the UTC-PD equivalent electrical circuit can be extracted. The parameters of the junction,  $C_{j0}$ ,  $V_j$  and  $M_{mr}$  can be extracted by taking the logarithm on both sides of Equation (6) in order to linearize it and then by performing an iteration on  $V_j$ , at low reverse voltage to obtain the best linear regression. Once  $C_{j0}$  is determined, the set of parameters:  $W_{SCR0}$ ,  $E_{max}(v_d = 0)$  and  $R_N(0)$  can be calculated. An optimization on the  $V_{PT}$  value, at high voltage, allows to determine  $C_{j0l}$ . After determining the junction parameters, forward and reverse current measurements without illumination are used to extract the DC characteristics of the UTC-PD junction as well as the reverse current parameters (band-to-band tunnel current and trap assisted tunnel current parameters) [17,20].

Finally, static photocurrent and bandwidth measurements are exploited to determine the optical parameters such as responsivity,  $R$ , and the transit times. The expression of the photo current includes two transit times [14]: the transit time in the absorber,  $\tau_a$ , and the transit time in the collector,  $\tau_c$ . The calculation of  $\tau_c$  via the electric field,  $E_{max}(v_d)$ , at the collector input, leaves only one transit time,  $\tau_a$ , to be extracted, which can be determined using the bandwidth measurements. It is important to note that, unlike conventional one-port  $S$ -parameter measurements that can be de-embedded, the bandwidth measurements still include the contributions from the pads and access lines. The extracted values of these extrinsic parasitic contributions are therefore re-injected into the final model to obtain realistic results.

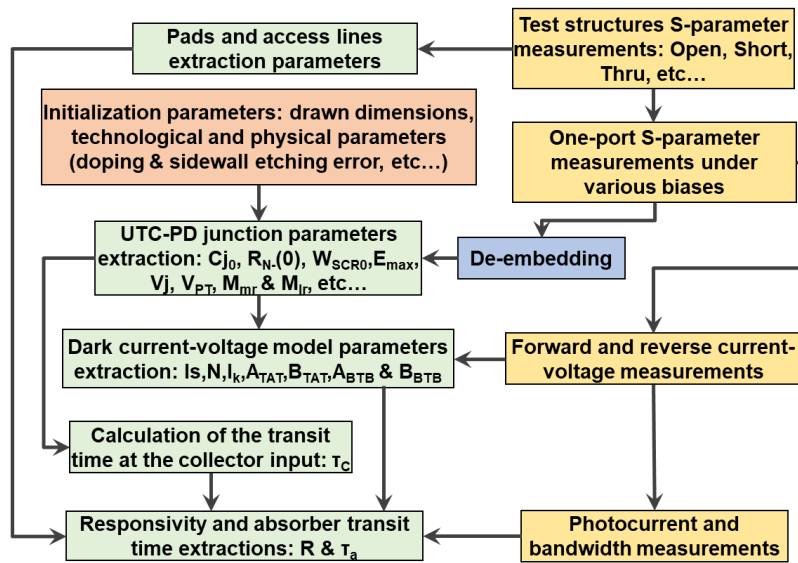


Figure 2. Methodology flow of the measurements and the parameter extraction of the UTC-PD.

### 3. Compact model validation

For the validation of the model scalability and affirming model versatility, both type I and II [21] UTC-PDs were measured. More specifically, two varieties of type I UTC-PDs have been characterized: (i) an InGaAs/InGaAsP UTC-PD with rectangular waveguides, through which the light is guided evanescently into the active region [22]; (ii) an InGaAs/InP UTC-PD with a simple top-illuminated structure. The type II device consist of a GaInAsSb/InP UTC-PD also with a simple top-illuminated structure [23]. Several geometries of the UTC-PDs were investigated in the study, with their active areas listed in Table 1. Dedicated test structures associated with the UTC-PDs were available for extraction of their intrinsic parameters.

Table 1. Geometries of the UTC-PDs under study.

| UTC-PD technology |                | Drawn active area ( $\mu\text{m}^2$ ) |
|-------------------|----------------|---------------------------------------|
| UTC-PD type I     | InGaAs/InGaAsP | 100, 125 and 150                      |
|                   | InGaAs/InP     | 13                                    |
| UTC-PD type II    | GaInAsSb/InP   | 64, 79 and 113                        |

#### 3.1. De-embedding procedure

##### InGaAs/InGaAsP UTC-PD de-embedding

At high frequencies (high data rates), the impact of the parasitic interconnects becomes even more important and must be accurately modelled. In our compact modelling work, this step is thus very important. Accessing the intrinsic physical parameters of the UTC-PD requires careful modeling of the RF pads and access lines. To achieve this goal, test structures reproducing the pads and access lines are required, such as the Open and the Short test structures presented in Figure 4. Indeed, there are several de-embedding techniques that can be applied to on-wafer devices, as reported in the literature [24]. A comprehensive investigation of the validity of these methods has been reported in [25]. The de-embedding methods are generally based on on-wafer  $S$ -parameter measurements of different dedicated test structures, which are then subtracted from the global  $S$ -parameter measurements of the devices under test. The number of test structures and the complexity of the de-embedding method mainly depend on the frequency at which the device operates. In this article, we show the limitations of the basic Open-Short de-embedding method at high frequencies (110 GHz). We then introduce a new de-embedding method that we have developed, which can be adapted to different designs of test structures and the frequency range of use.

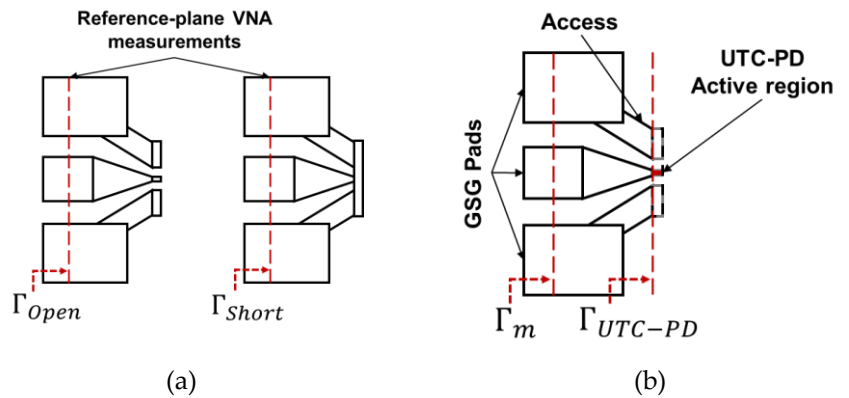


Figure 4. Schematic of: (a) Open and Short test structures (b) schematic of the UTC-PD connected to the pads and access lines.

In order to apply the de-embedding method on the InGaAs/InGaAsP UTC-PDs, one-port S-parameter measurements were performed up to 110 GHz on dedicated test structures, which consist of an Open, a Short and some other complementary test structures that are presented later. The S-parameter measurements were preceded by an off-wafer SOLT calibration on a CS-5 substrate, in order to bring the measurement reference planes at the probe tips (Picoprobe tips). The One-port S-parameter measurements were performed using an Agilent E8361 PNA, with a frequency extender for the 67-110 GHz frequency range.

The Open and Short test structures are usually modeled by a single capacitance, an inductance and a resistance. Due to the specific design of the InGaAs/InGaAsP UTC-PDs, this representation at high frequency is no longer valid as shown by the frequency-dependent behaviors shown in Figure 5a. Consequently, complementary structures have been designed (Figure 5b), that reproduce the pads and the access lines. Along with these, an on-wafer characterization and a step-by-step reconstruction of the distributed network allows to extract the intrinsic characteristics of the UTC-PDs. With the equivalent circuits of the pads and access lines determined, the S-parameter matrix can be simulated and the reflection coefficient of the UTC-PD can therefore be calculated by the following expression:

$$\Gamma_{UTC-PD} = \frac{S_{11} - \Gamma_M}{S_{11}S_{22} - S_{22}\Gamma_M - S_{12}S_{21}} \quad (9)$$

Where,  $S_{ij}$  are the S- matrix elements of the pads and access lines and  $\Gamma_M$  is the measured total reflection coefficient.

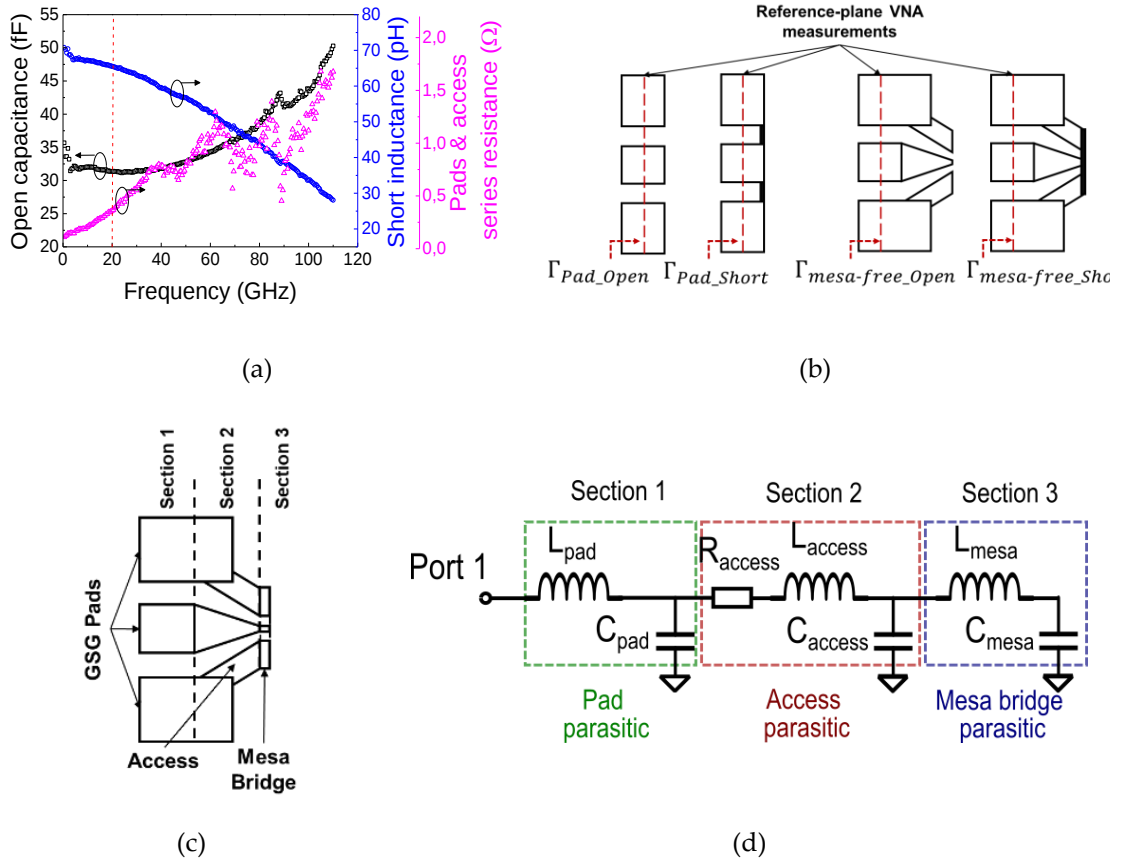


Figure 5. (a) Extraction of capacitive, inductive and resistive parasitic equivalents to the pads and access lines (b) schematic of the complimentary test structures (c) schematic of the UTC-PD depicting the three parasitic sections (d) global electrical circuit equivalent to the pads and access lines.

The overall equivalent circuit of the pads and access lines has three sections, as shown in Figure 5c,d. The first section represents the equivalent electrical circuit of the pads. It includes an inductance,  $L_{pad}$ , and a capacitance,  $C_{pad}$ , of the pads. The lumped parasitic elements of the pads can be determined from measurements of the reflection coefficients of the Pads-Short,  $\Gamma_{pad\_short}$ , and Pads-Open,  $\Gamma_{pad\_open}$ , test structures. Extracting the inductive element,  $L_{pad}$ , from  $\Gamma_{pad\_short}$ , yields an overestimated value (Figure 6a), as it actually includes a ground return inductance. A correction in the value of  $L_{pad}$  can be made by optimizing the simulation on the imaginary part of  $Y_{pad\_short}/\omega$  extracted from measurement at high frequency. The capacitance of the pads,  $C_{pad}$ , can be extracted from  $Y_{pad\_open}/\omega$  at low frequency (Figure 6a).

The same process was performed to reconstruct the other two sections using the mesa-free Open and Short test structures and the earlier test structures (Open and Short) that include the mesa accesses. The equivalent capacitances of the mesa-free access,  $C_{access}$ , and mesa access,  $C_{mesa}$ , can be determined at low frequency from the imaginary part of  $Y_{mesa-free\_open}$  and  $Y_{open}$ , respectively (Figure 6b). The equivalent inductance of the mesa-free access,  $L_{access}$ , and the mesa inductances,  $L_{mesa}$ , were determined by optimization on the high frequency region of the measured  $Y$ -parameters. The access resistance,  $R_{access}$ , can be determined by averaging over the real part of  $Z_{mesa-free\_short}$ . The complete set of parasitic lumped elements are summarized in Table 2.

Table 2. Extracted values of the lumped electrical elements, equivalent to the pads and access lines for the InGaAs/InGaAsP UTC-PDs.

| $L_{pad}$ | $C_{pad}$ | $R_{access}$  | $L_{access}$ | $C_{mesa}$ | $L_{mesa}$ | $C_{mesa}$ |
|-----------|-----------|---------------|--------------|------------|------------|------------|
| 18.0 pH   | 15.0 fF   | 0.83 $\Omega$ | 28.0 pH      | 11.0 fF    | 5.0 pH     | 5.0 fF     |

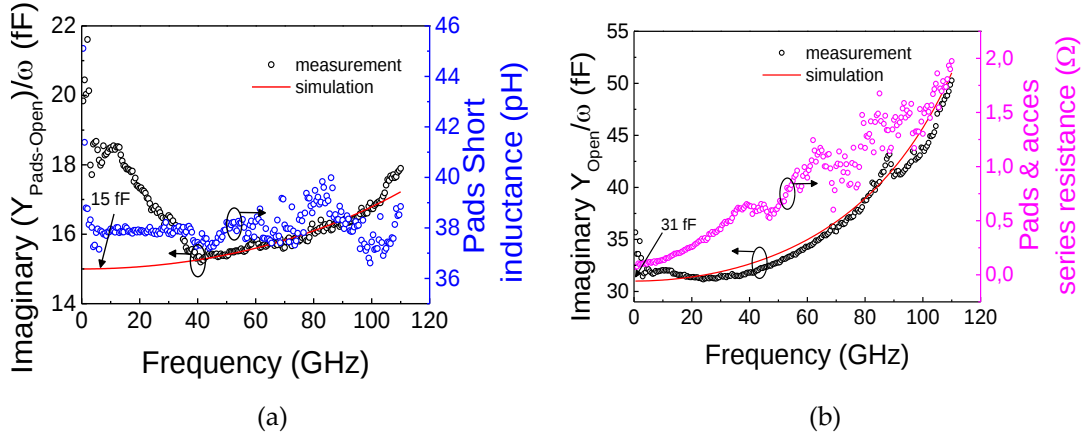


Figure 6. Extraction of parasitics equivalent for: (a) the Pad Open and the Pad Short (b) the mesa-free access lines.

It is worth noting that this contribution was accepted at the EuMW 2022 conference [26].

#### GaInAsSb/InP UTC-PD de-embedding

In order to apply de-embedding on the GaInAsSb/InP UTC-PDs, one-port  $S$ -parameter measurements were performed up to 67 GHz on Open and Short test structures. The  $S$ -parameter measurements were preceded by an off-wafer LRRM (line/reflection/match) calibration [27] in order to bring the measurement reference plane up to the RF probe tips. For the GaInAsSb/InP UTC-PDs, the electrical elements equivalent to the Open and Short test structures (Figure 7a) are found to be almost frequency independent in the frequency range of study

(up to 67 GHz) (Figure 7b). The use of the classical Open-Short/Short-Open de-embedding methods allows extraction of the junction capacitance, but they do not provide reliable results for the compact model validation over the entire frequency range. This is because of the fact that the use of the Short test structure leads to an under/over de-embedding at high frequency, which in turn results in an intrinsic junction capacitance that depends on the frequency as shown in Figure 7c. This is an unphysical behavior and cannot be captured by the UTC-PD compact model.

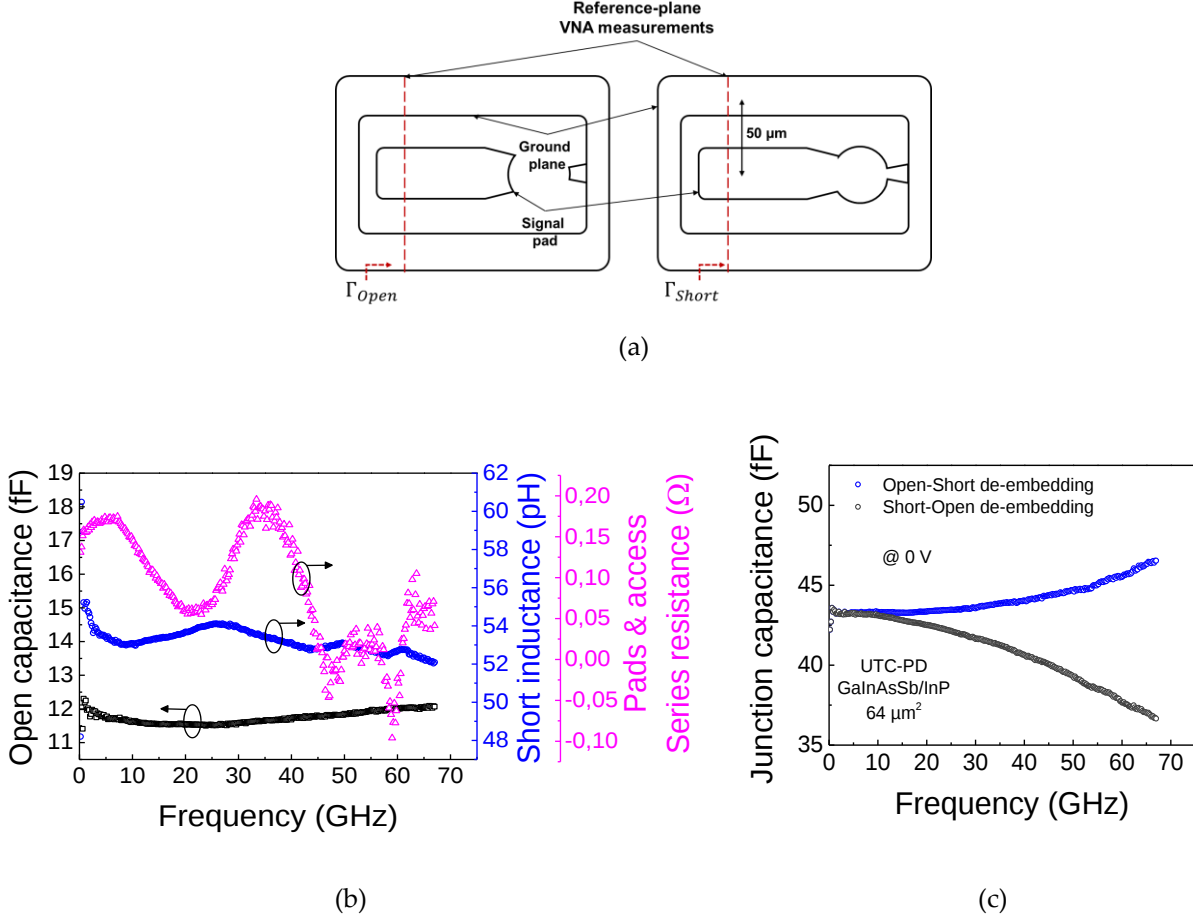


Figure 7. (a) Open and Short test structures (b) Extraction of parasitic capacitance, inductance and resistance equivalents to the Open and Short test structures (b) Extraction of the UTC-PD junction capacitance.

Modeling the pads and access lines using only single  $RLC$  network (Open-Short case) is not adequate enough to capture the actual frequency dependence of the UTC-PDs. Therefore, the pads and access lines were modeled by a cascaded  $R_n L_n C_n$  network consisting of  $N$  sections as shown in Figure 8a. Such implementation has been demonstrated up to 40 GHz in [28]. In the present study, three cascaded  $R_n L_n C_n$  elements were identified and this was achieved by ensuring that the resulting intrinsic junction capacitance of the UTC-PDs does not exhibit a frequency dependence. The  $R$  value was extracted from the real part of  $Z_{Short}$ .  $L$  and  $C$  values were determined by optimization on the imaginary part of  $Y_{Open}$  as shown in the Figure 8b, leading to three cascaded  $R_n L_n C_n$  elements. As presented in Figure 8b, the sum of the capacitances,  $\sum_{i=1}^N C_i/N$ , tends to  $Y_{Open}/\omega$  at low frequencies and the sum of the inductances,  $\sum_{i=1}^N L_i/N$ , was determined through an optimization at high frequency. The extracted parameter values are listed in Table 3. Once the equivalent network is accurately modeled, two-port  $S$ -parameter simulations of the cascaded network are used to determine the intrinsic parameters of the UTC-PD using eq. (9). Figure 8c shows

the UTC-PD junction capacitance de-embedded using the cascaded network. The results clearly reflect an improvement through the correction for the over de-embedding discussed earlier.

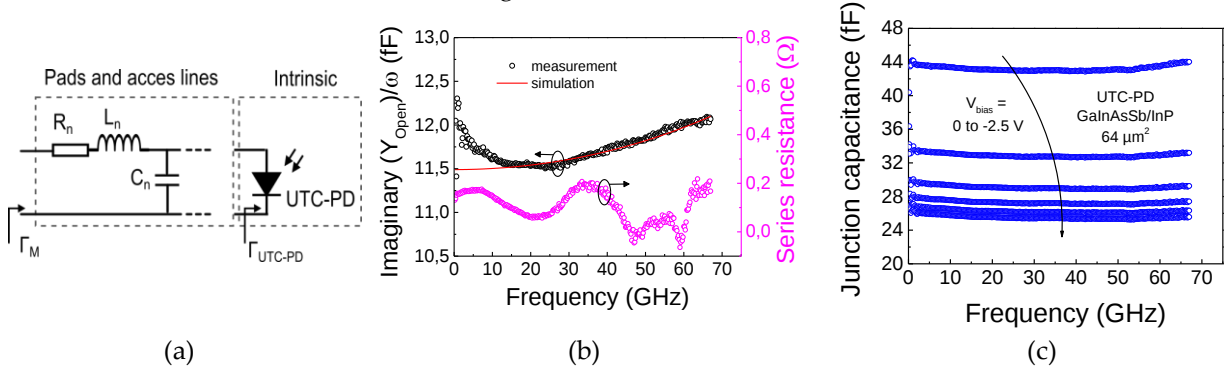


Figure 8. (a) Equivalent circuit of the UTC-PD connected to cascaded pads and access lines (b) extracted parasitic elements associated with the Pads and access lines (c) extracted UTC-PD junction capacitances at various reverse bias.

Table 3. Extracted RLC lumped elements values from GaInAsSb/InP UTC-PD Open and Thru test structures.

| <b>R</b>      | <b>L</b> | <b>C</b> |
|---------------|----------|----------|
| 0.19 $\Omega$ | 47.55 pH | 11.49 fF |

#### InGaAs/InP UTC-PD de-embedding

The method of de-embedding therefore can be generalized and extended to a wide range of frequency and various Open test structure designs. Taking advantage of this methodology, a dedicated InGaAs/InP UTC-PD Open test structure was characterized using the same setup and measurement procedure as the one used for the test structures of the InGaAs/InGaAsP UTC-PDs. The Open test structure (Figure 9a) was modelled by a  $R_n L_n C_n$  cascade of nine sections. This was achieved by optimizing the  $\sum_{i=1}^{N=9} C/N$  and  $\sum_{i=1}^{N=9} L/N$  values on the imaginary part of  $Y_{Open}/\omega$ , as shown in Figure 9c. Note here that since we did not have a Short test structure, we used a Thru test structure (Figure 9b) to determine the series resistance,  $\sum_{i=1}^{N=9} R/N$ . This was achieved by converting the measured two-port S-parameters into the transfer matrix  $ABCD$ , then by determining the complex propagation constant,  $\gamma = \alpha + j\beta$ , and the characteristic impedance of the Thru test structure,  $Z_c$ , from the  $ABCD$  matrix (Figure 9d). Finally, the linear series resistance,  $R_{Thru}$ , (Figure 9e) can be determined from the real part of the product  $\gamma \cdot Z_c$  [29]. By multiplying the  $R_{Thru}$  by the length (278  $\mu\text{m}$ ) of the pads and the access lines of the InGaAs/InGaAsP UTC-PD, we obtain  $\sum_{i=1}^{N=9} R/N$ . The number of the  $R_n L_n C_n$  cascade is a bit high in this case since, on the one hand, we work at higher frequencies (up to 110 GHz), and on the other hand, the access lines of the test structures are relatively longer than the previous case. The values of these elements are reported in Table 4. Once the electrical equivalent network is accurately modeled, two-port S-parameter simulations of the distributed  $RLC$  network are used to determine the intrinsic parameters of the UTC-PDs by applying eq. (9).

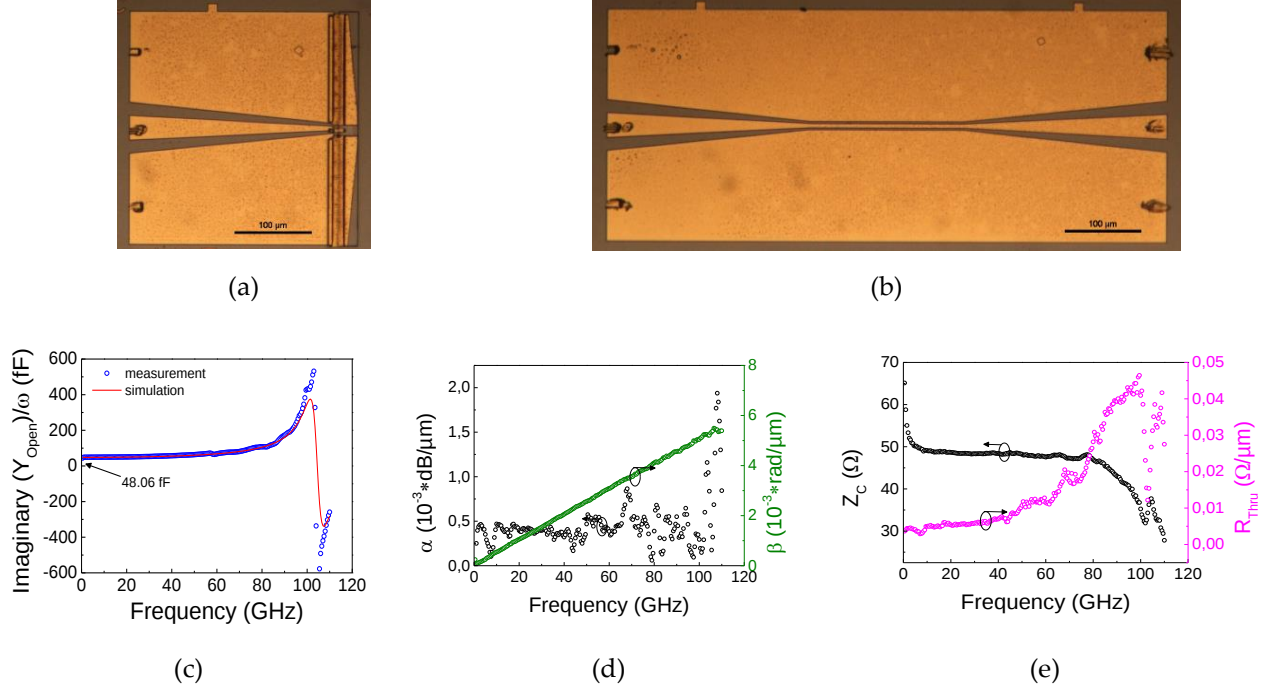


Figure 9. (a) Microscope image of the Open test structure (b) microscope image of the Thru test structure (c) extracted  $LC$  parasitics of the equivalent circuit for the InGaAs/InP UTC-PD Open test structure (d) extracted attenuation constant  $\alpha$ , and phase constant  $\beta$  of the Thru test structure (e) extracted characteristic impedance,  $Z_C$ , and calculated linear series resistance  $R_{Thru}$ , of the Thru test structure.

Table 4. Extracted RLC lumped element values for InGaAs/InP UTC-PD Open test structure.

| $R$          | $L$       | $C$      |
|--------------|-----------|----------|
| 1.5 $\Omega$ | 106.74 pH | 48.06 fF |

### 3.2. Validation of RF Characteristics

#### 3.2.1. Intrinsic junction Capacitance extraction

In order to validate the dynamic behavior of the UTC-PD compact model, one-port  $S$ -parameter measurements were performed. Measurements up to 110 GHz under a reverse bias ranging from 0 to  $-2V$  were carried on the InGaAs/InGaAsP and InGaAs/InP UTC-PDs. Measurements up to 67 GHz under reverse bias ranging from 0 to  $-2.5 V$  were performed on the GaInAsSb/InP UTC-PDs. After applying the suitable de-embedding method for each UTC-PD, following the procedure explained in Section 2, we can validate the compact model on the intrinsic  $S$ -parameters.

Figures 10 and 11 show scalable compact model validation against  $S$ -parameter measurements of the amplitude and the phase of the different intrinsic UTD-PDs under study. Excellent agreement is observed for all geometries and all UTC-PD technologies affirming the scalability and versatility of the compact model.

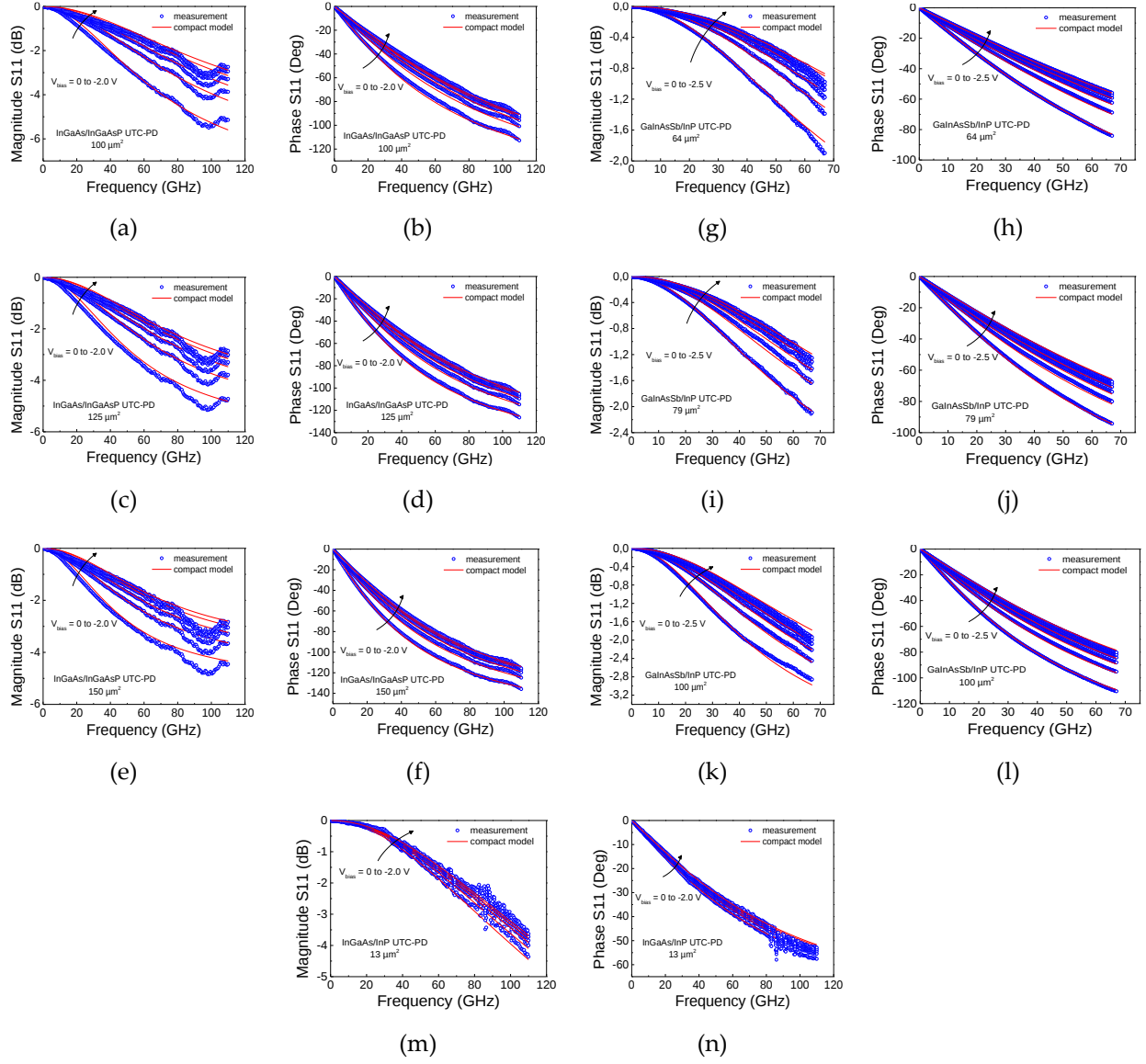


Figure 10. Measured (symbol) and simulated (lines) intrinsic S11-parameter for all the UTC-PDs technologies: (a-c-e) magnitude in dB of InGaAs/InGaAsP UTC-PD with active areas of 100, 125 and 150  $\mu\text{m}^2$  (b-d-f) phase in degree of InGaAs/InGaAsP UTC-PD with active area of 100, 125 and 150  $\mu\text{m}^2$  (g-i-k) magnitude in dB of GaInAsSb/InP UTC-PD with active area of 64, 79 and 100  $\mu\text{m}^2$  (h-j-l) phase in degree of GaInAsSb/InP UTC-PD with active area of 64, 79 and 100  $\mu\text{m}^2$  (m) magnitude in dB of InGaAs/InP UTC-PD with a 13  $\mu\text{m}^2$  active area (n) phase in degree of InGaAs/InP UTC-PD of 13  $\mu\text{m}^2$  of active area.

The new implementation of the junction capacitance model (eqs. (5)-(7)) captures the physics of UTC-PDs much better than the conventional model and thereby offers excellent scalability and agreement with measurement results as depicted in Fig. 11.

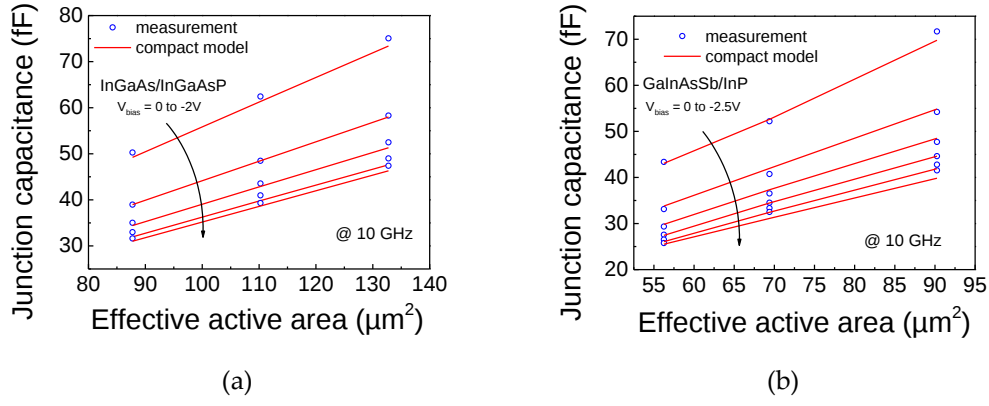


Figure 11. UTC-PD junction capacitance as functions of the active device area and the applied reverse bias: (a) InGaAs/InGaAsP UTC-PD (b) GaInAsSb/InP UTC-PD.

### 3.2.2. Intrinsic series resistance extraction

The overall series resistance can be extracted from the real part of the intrinsic  $Z_{11}$ -parameter. In the case of the rectangular InGaAs/InGaAsP UTC-PDs, the contact covers the entire mesa, which makes it easy to determine the scaling law by analyzing the effective area of the device geometry. Figure 12 shows the overall series resistance extracted at 80 GHz for the three geometries at various biases. Since the collector is 425 nm thick, it is not completely depleted. As the reverse voltage increases, the collector resistance decreases until it disappears at full collector depletion.

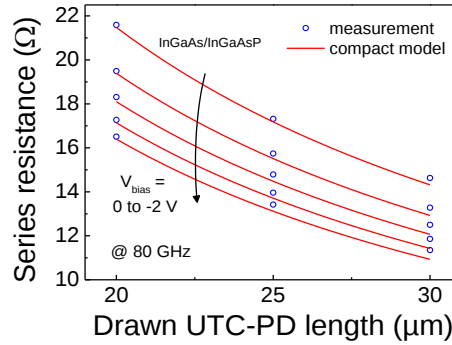


Figure 12. The extracted total series resistance at various reverse biases and for several lengths of the InGaAs/InGaAsP UTC-PDs.

The resistance values are extracted for the GaInAsSb/InP UTC-PDs from the real part of  $Z_{11}$ -parameter at a frequency of 60 GHz. The extracted values are: 11.6  $\Omega$ , 10.7  $\Omega$  and 12.4  $\Omega$  for the UTC-PD geometries of 64  $\mu\text{m}^2$ , 79  $\mu\text{m}^2$  and 113  $\mu\text{m}^2$  active area respectively. Contrary to the rectangular waveguide InGaAs/InGaAsP UTC-PDs, the metallic contacts of the GaInAsSb/InP UTC-PDs are located at the edge of the mesa. In addition, the contact width varies for each geometry. It is therefore not surprising that the resistance does not scale with the mesa area. It is important to note that no bias dependence was observed as the collector is already fully depleted at zero bias, due to the small thickness of the collector.

The InGaAs/InP UTC-PDs have a structure similar to the one of the GaInAsSb/InP UTC-PDs where the metal contact is located at the edge of the mesa. A series resistance of 51.3  $\Omega$  was extracted at 80 GHz from the real part of  $Z_{11}$ -parameter.

### 3.3. Validation of DC Characteristics

The validation of the compact model against the dark current characteristics was performed following the extracting of relevant model parameters from the forward and reverse current measurements. These measurements were performed in the bias range of (-3, 1) V, and (-5, 1) V for InGaAs/InGaAsP and GaInAsSb/InP UTC-PDs, respectively. All measurements were performed at room temperature. Figure 13a,b compare the measured DC characteristics and the compact model simulation, demonstrating good accuracy of the model over the entire forward and reverse bias ranges. All UTC-PDs under test show very low dark current levels (below 25 nA at -2V). The low values of the dark current implies a higher quality of the passivation of the junction in the UTC-PDs. We note here that a study of the dark currents at different temperatures along with compact model validation has been presented in a previous study where the model also showed excellent results [3].

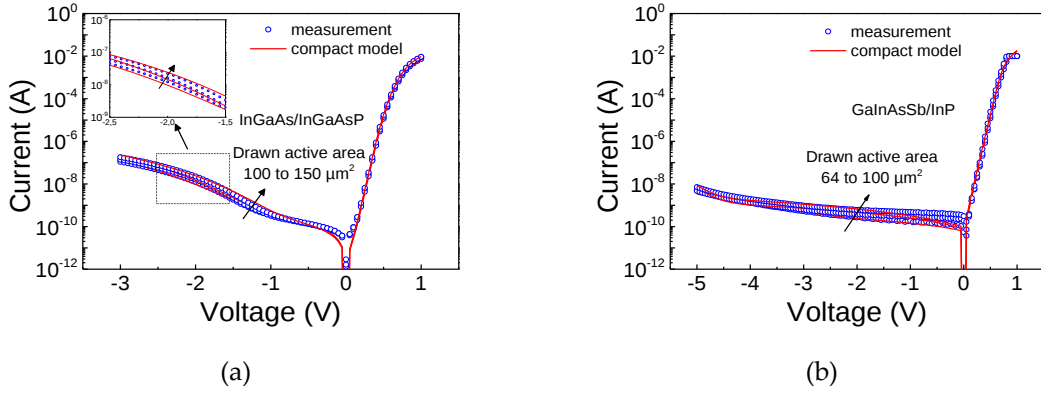


Figure 13. Measured (symbol) and simulated (lines) dark current-voltage characteristics of UTC-PDs with several active areas for (a) InGaAs/InGaAsP UTC-PD (b) GaInAsSb/InP UTC-PD.

#### 3.4. Bandwidth validation

Once the validation of the compact model of the UTC-PD and electrical model parameter extraction have been performed on the DC and RF characteristics under non-illuminated operating conditions, the dynamic photo-response of the compact model has then been verified for both types of UTC PD technologies, for all available geometries under different applied bias conditions. For the InGaAs/InGaAsP UTC-PDs, the optical frequency response of the photodiodes was measured with a heterodyne measurement bench. A high responsivity of 0.79 A/W, at  $\lambda = 1550$  nm, has been reported for these devices [3]. The optical frequency response of the UTC-PDs are measured at -2V bias under an optical power of 3 dBm. -3dB extrinsic bandwidths ranging from 40 GHz to 47 GHz for all geometries studied can be observed in Figure 14a. The intrinsic bandwidth can be determined using the calculated/extracted transit times using the compact model. In addition, intrinsic bandwidths ranging from 45 GHz to 56 GHz are determined, indicating the detrimental impact of the pads and access lines on the bandwidth.

For the optical characterization of the GaInAsSb/InP UTC-PDs, an optical signal ( $\lambda = 1550$  nm), of 3 dBm power, modulated by a Mach Zehnder modulator (MZM) nm was used. Measurements were performed with a bias ranging from 0 to -2.5 V. Figure 14b shows an excellent agreement between the measurements and the model predictions over the entire frequency and voltage ranges. It should also be noted that the measured bandwidths of the UTC-PDs do not change significantly compared to their intrinsic bandwidth of the component since the values of the junction capacitances are much higher than those of the pads and the access lines. In other words, the pad parasitic elements are less significant for these type of UTC-PDs.

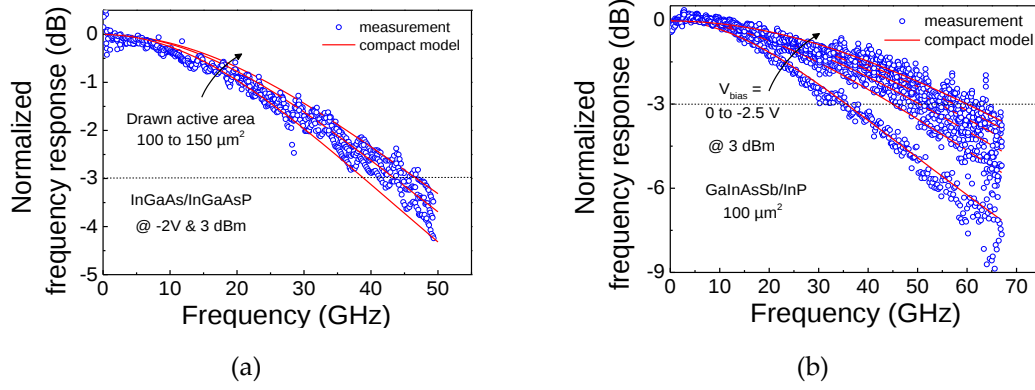


Figure 14. Bandwidths of the UTC-PDs: (a) InGaAs/InGaAsP UTC-PDs (b) GaInAsSb/InP UTC-PD.

#### 4. Conclusion

In this work, we presented improvements on the first compact model developed for the UTC-PDs. The model now incorporates more physical parameters and scaling laws. This is particularly important for predictive design and optimization of emerging optoelectronic integrated circuits. An extraction method has been developed based on the parameter extraction strategy for bipolar electronic technologies. A new and improved de-embedding methodology that provides access to the intrinsic parameters of the UTC-PD has been demonstrated and incorporated within the parameter extraction flow. The static and dynamic behavior of the model have been validated against on-wafer measurements up to 67 GHz and 110 GHz on three UTC-PD technologies developed on the InP substrates. The model has demonstrated excellent versatility and scalability with respect to two types of UTC-PDs and several geometries under study under a wide range of bias conditions. These results appear very promising, laying an extensive groundwork for the design of OEIC systems. Model compatibility with existing EDA framework also marks an important step for realizing a single simulator based optoelectronic system design. Further advancements through multi-physics co-simulation and design optimization of the two technological modules will be the subject of future work.

**Author Contributions:** D.G. mainly contributed to InGaAs/InGaAsP UTC-PDs characterization, compact modeling, de-embedding, parameter extraction and investigations, as well as manuscript conceptualization, organization, writing—review and editing. C.M. (Chhandak Mukherjee) mainly contributed to compact modeling, organization, as well as manuscript conceptualization, writing—review and editing. M.D. mainly contributed to de-embedding, organization, as well as manuscript conceptualization, writing and review. M.D.M. contributed to the measurement support as head of the IMS characterization platform. C.C. mainly contributed to InGaAs/InGaAsP UTC-PDs photodiode conceptualization and characterization. H.B., A.B., N.V., and K.M. mainly contributed to InGaAs/InGaAsP UTC-PDs process development, epitaxy and fabrication. A.M.A., R.C. and O.O. mainly contributed to GaInAsSb/InP UTC-PDs conceptualization, process development, epitaxy, fabrication and characterization. C.B. mainly contributed to the GaInAsSb/InP UTC-PDs conceptualization, review and supervision. P.M. mainly contributed to funding acquisition, project administration, review and supervision. C.M. (Cristell Maneux) mainly contributed to funding acquisition, project administration, review, editing and supervision. All authors have read and agreed to the published version of the manuscript.

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