



# Architecture optimization of SPAD integrated in 28 nm FD-SOI CMOS technology to reduce the DCR

D. Issartel<sup>a</sup>, S. Gao<sup>a</sup>, P. Pittet<sup>d</sup>, R. Cellier<sup>b</sup>, D. Golanski<sup>c</sup>, A. Cathelin<sup>c</sup>, F. Calmon<sup>a,\*</sup>

<sup>a</sup> Univ Lyon, INSA Lyon, CNRS, INL, UMR5270, Villeurbanne, France

<sup>b</sup> Univ Lyon, CPE Lyon, CNRS, INL, UMR5270, Villeurbanne, France

<sup>c</sup> STMicroelectronics, Crolles, France

<sup>d</sup> Univ Lyon, UCBL, CNRS, INL, UMR5270, Villeurbanne, France

## ARTICLE INFO

The review of this paper was arranged by "Bogdan Cretu".

### Keywords:

SPAD  
FD-SOI CMOS  
TCAD simulation  
Avalanche process  
Dark Count Rate – DCR  
Shallow Trench isolation – STI

## ABSTRACT

This article presents a study of Single Photon Avalanche Diodes (SPAD) implemented in 28 nm Fully Depleted Silicon-On-Insulator (FD-SOI) CMOS technology based on transient TCAD simulations and Dark Count Rate (DCR) measurements. The integration of SPAD in this technology is currently being studied. This work allows for a better understanding of the mechanism behind the quite high DCR measured at relative low excess bias voltages with the initial FD-SOI SPAD design ( $\approx 500 \text{ Hz}/\mu\text{m}^2$  at 5% excess bias voltage). In this study, a TCAD transient simulation methodology is introduced to better understand SPAD behavior during the avalanche process. TCAD simulations revealed that Shallow Trench Isolation (STI) structures within the active area have a negative effect on avalanche quenching, because of slower carrier evacuation with possible occurrence of secondary avalanches in series. Based on this analysis and on previous optimization works, we propose a new architecture of the FD-SOI SPAD combining several modifications to achieve a lower DCR ( $\approx 20 \text{ Hz}/\mu\text{m}^2$  at 5% excess bias voltage measured with passive quenching).

## 1. Introduction

Single Photon Avalanche Diodes (SPAD) are photodetectors appreciated for their weak intensity light detection, thanks to high avalanche gain and fast response time [1,2]. SPAD are used in various application domains such as 3D imaging (self-driving vehicles, facial recognition), biomedical imaging, visible light communications, cryptography, and quantum communications [3,4].

SPAD pixels include photo-sensing area associated to the addressing, quenching and recharging electronics [5]. Avalanche cycles occurring in SPAD consist mainly of an exponential current increase followed by i) a quenching step where the avalanche is stopped allowing for current reduction and ii) a recharging step for the restoration of the initial reverse biasing condition  $V_{rev}$  above breakdown voltage  $V_{BD}$  ( $V_{rev} = V_{BD} + V_{ex}$  where  $V_{ex}$  is denoted as the excess voltage). Quenching can be implemented either by connecting an equivalent high resistance in series with the diode (passive quenching) or by using more complex circuits (active quenching) allowing the control of the dead time before SPAD recharge [6–8].

In addition, in the last few years, another active field of research was focused on the integration of SPAD in advanced CMOS technologies [10], including in a Silicon-On-Insulator (SOI) platform [11]. Recent work focuses on the design of small SPAD cells with a better collection of photogenerated carriers thanks to the charge focusing concept [12]. Moreover, two-tier 3D integration of SPAD arrays and associated electronics has been developed to obtain higher fill factors and Photon Detection Probability (PDP) for the Near Infrared light (NIR). However, 3D SPAD architecture relies on complex Wafer-to-Wafer bonding techniques [13]. Other researches aim to maximize the SPAD PDP for NIR wavelengths with a more efficient absorption layer (using SiGe or Ge) separated from the silicon multiplication layer [14].

In this paper, we focus on SPAD designed and fabricated in 28 nm Fully Depleted Silicon-On-Insulator (FD-SOI) CMOS technology [15] (Fig. 1) for an intrinsic 3D pixel featuring optimized fill factor with back side illumination (BSI). We analyze the impact of the Shallow Trench Isolation (STI) structures on the avalanche cycle of SPAD FD-SOI and Dark Count Rate (DCR) thanks to transient TCAD simulations [16] associated with DCR measurements. The article is organized as follows.

\* Corresponding author.

E-mail addresses: [dylan.issartel@insa-lyon.fr](mailto:dylan.issartel@insa-lyon.fr) (D. Issartel), [shaochen.gao@insa-lyon.fr](mailto:shaochen.gao@insa-lyon.fr) (S. Gao), [patrick.pittet@univ-lyon1.fr](mailto:patrick.pittet@univ-lyon1.fr) (P. Pittet), [remy.cellier@cpe.fr](mailto:remy.cellier@cpe.fr) (R. Cellier), [dominik.golanski@st.com](mailto:dominik.golanski@st.com) (D. Golanski), [andrea.cathelin@st.com](mailto:andrea.cathelin@st.com) (A. Cathelin), [francis.calmon@insa-lyon.fr](mailto:francis.calmon@insa-lyon.fr) (F. Calmon).

<https://doi.org/10.1016/j.sse.2022.108297>

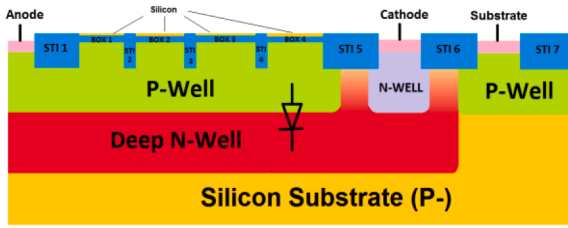


Fig. 1. Schematic view of the SPAD implemented in FD-SOI CMOS technology – half structure with cylindrical symmetry is considered (not to scale) [9].

In section 2, the layout of the studied SPAD FD-SOI cell is described, while in section 3, process and device TCAD simulation methodology is presented (section 3.1). The results of the TCAD study are reported and discussed in sections 3.2 and 3.3 for the original and modified SPAD architectures, respectively. In section 4, we describe the optimized FD-SOI SPAD architecture combining the previous TCAD study relative to STI trenches locations and a softened diode doping profile already studied in [17]. In section 5, we present the DCR characterization for the SPAD FD-SOI structure combining all optimization paths and we conclude in section 6.

## 2. SPAD implemented in FD-SOI CMOS technology

FD-SOI CMOS technology is schematically based on two silicon layers electrically insulated by a thin oxide layer, i.e. the Buried Oxide (BOX). The addition of this BOX layer enables the reduction of junction parasitic capacitances and a better electrostatic control of the channel of transistors for lower short channel effects and leakage currents.

In this technology, electronic circuits are implemented in the thin upper silicon layer while the silicon substrate contains P and N wells (PW, NW), allowing for body-biasing of transistors, and Deep N-wells (DNW), which permit isolation between different PW.

The SPAD implementation in this technology takes benefit of the two silicon layers. The associated electronics (quenching and addressing) is integrated in the upper thin silicon layer, while, the SPAD cell relies on the PW-DNW junction [18–19] below the BOX, as shown in Fig. 1. The design of SPAD FD-SOI has been studied in previous works [9,15,17]. Thus, it allows an intrinsic 3D implementation, at die level, of the SPAD and its associated electronics with BSI. Additionally, indirect SPAD event detection through the BOX and improved active quenching using body-biasing technique were also presented [8,15].

This cell has been fabricated in a standard 28 nm FD-SOI CMOS process and characterized. This cell shows a relatively high DCR for low excess bias voltages (less than 1 V) as compared to the state of the art. We have shown recently that a decrease of the DNW doping level can be used to increase the breakdown voltage ( $V_{BD}$ ) by several volts [17], and may reduce the DCR (section 4.1). We have also analyzed to push the Shallow Trench Isolation (STI) blocks entirely on the edges of the active zone to reduce premature edge breakdown [9–20–21] (section 4.2). With such optimizations, it was possible to reduce DCR but not sufficiently compared to state-of-the-art. Then, additional TCAD simulations have been carried out for a better understanding of the origins of this high DCR in order to make further cell optimizations.

## 3. Avalanche transient TCAD simulations

### 3.1. TCAD simulation methodology

Process and device level simulations for transient analysis using the TCAD Synopsys Sentaurus software workbench [22] are presented in this section. The cross section of the studied structure is shown in Fig. 2 (cylindrical symmetry) and the overall simulation flow is illustrated in Fig. 3.

We described and parametrized the main steps of the technological

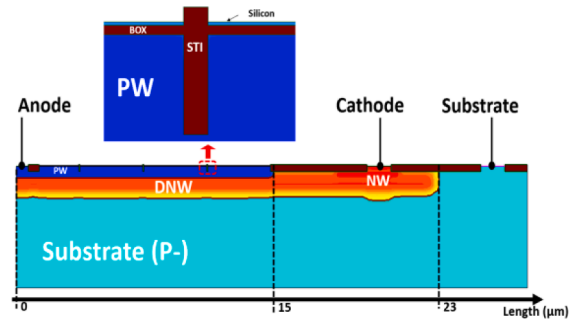


Fig. 2. TCAD view of the SPAD in FD-SOI CMOS technology after the process simulations (top: zoom on a STI trench).

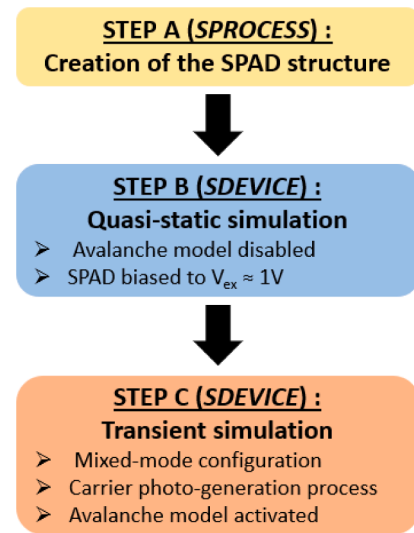


Fig. 3. TCAD transient simulation methodology.

process (especially relative PW, NW, DNW) in the simulation framework according to confidential data (Step A in Fig. 3).

For the device's electrical simulation, we started by calibrating our simulations using the static  $I-V$  characteristic of the diode [17]. In particular, the avalanche model and its parameters were determined to obtain a simulated breakdown voltage as a function of temperature,  $V_{BD} = f(T)$ , close to the measured one. The Van Overstraeten model [23], which gives consistent results, i.e. comparable with measurements, was chosen. In addition, the carrier lifetimes were adjusted in order to obtain a dark current in good agreement with measurements.

Then, transient electrical studies were carried out in two steps. The first one (Step B in Fig. 3) was an initialization phase in which i) the structure was biased to an excess voltage ( $V_{ex}$ ) of approximately 1 V and ii) the avalanche model was disabled (quasi-static simulation). From this unstable equilibrium point, we move to the second phase (Step C in Fig. 3), the mixed-mode transient simulation with a localized carrier photo-generation process to trigger the avalanche process [18]. In this last step, to trigger the avalanche process, the VanOverstraeten model is activated [24]. The electrical connections are shown in Fig. 4. The quenching circuit implements a 200k $\Omega$  external resistance ( $R_Q$ ) connected to the anode of the SPAD. The parasitic capacitance of 3fF ( $C_Q$ ), is also shown in Fig. 4.

We implemented a short optical stimuli (10 ps) to induce the photo-generation of electron-hole pairs inside the Space Charge Region (SCR). The transient TCAD simulation allows for a dynamic analysis of the avalanche process by monitoring over time some internal device data (e.g. current density).

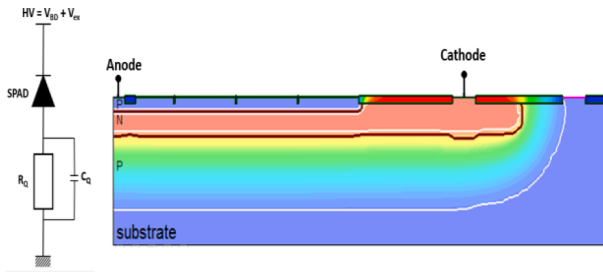


Fig. 4. TCAD view of the SPAD with electrical connections for the mixed-mode transient simulations.

### 3.2. Unexpected behavior of the reference SPAD structure

Our study on transient simulations, which was carried out on the reference (original) SPAD structure (see Figs. 1 and 2), reveals an unexpected behavior. As shown in Fig. 5, the initial current (marker A) is approximately at 0.1 nA (dark current). After the triggering of the avalanche, the current exhibits a steep increase and reaches  $\sim 1$  mA (marker B). Then, we observe a current decrease resulting from the passive quenching (region C). However, the avalanche current does not fully subside, and the diode current remains several orders of magnitude higher than its initial level (region D). The same behavior was observed for various quenching resistances  $R_Q$  of 20 k $\Omega$ , 200 k $\Omega$  and 2 M $\Omega$ .

Another representation of the SPAD avalanche cycle is given in Fig. 6. It plots the current as a function of the SPAD voltage. During phase 1 (region ①), the amount of impact ionizations increases in time and corresponds to the steep current observed in Fig. 5. The current decreases in phase 2 thanks to passive quenching (region ②). The cycle seems to halt after this quenching phase (at marker ③), but by examining this area up close, we observe some repetitions of the cycle corresponding to the triggering of secondary avalanches in series.

Cartography studies of the current density in the structure explain this behavior. As shown in Fig. 7, the localized light pulse induces the current density increase due to the avalanche process (marker A, Fig. 7i). After a short-elapsd time (a few nanoseconds), the current density spreads and a second avalanche appears. The latter is located below the STI trench closest to the illumination area (marker B, Fig. 7ii). Thereafter, a high current density remains present under this STI block, which acts as a funnel limiting the current flow and increasing the current density magnitude locally. It would then seem that these STI blocks, located within the active zone, caused multiple avalanches in series. To tackle this issue, several methods were considered, such as the displacement or enlargement of the anode contact. The next section studies the most simple and direct way to address this issue, i.e. by

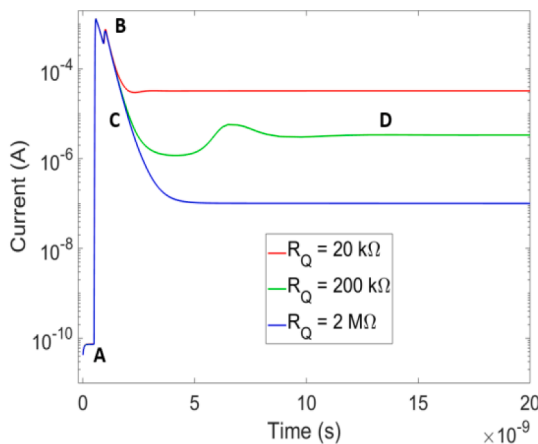


Fig. 5. SPAD current curves obtained with transient simulations on the reference structure for various values of  $R_Q$ .

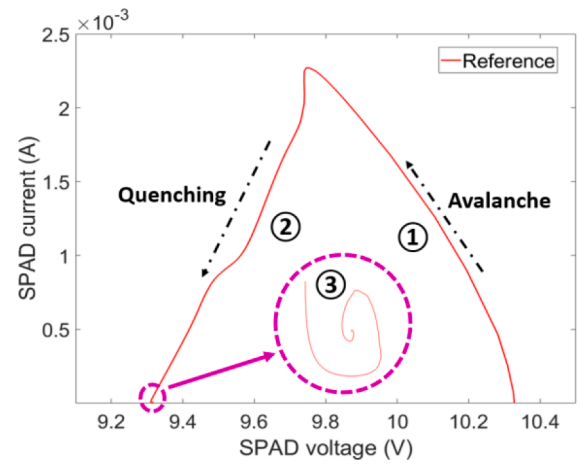


Fig. 6. Quenching cycle of the reference structure during transient simulations ( $R_Q = 200$  k $\Omega$ ).

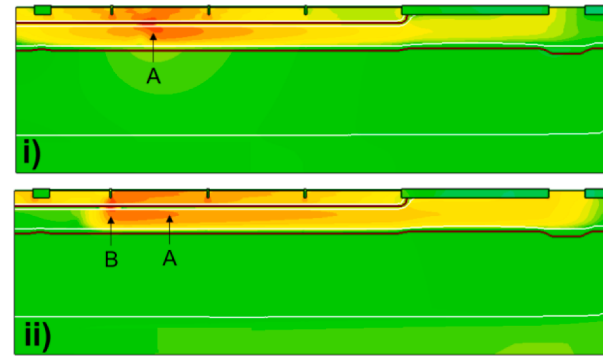


Fig. 7. Current density cartography during transient simulations for the reference SPAD structure: i) just after the light pulse, ii) few nanoseconds after i).

removing the STI trenches.

### 3.3. Simulations of the modified SPAD structure without STI trenches

In the physical design of SPAD in FD-SOI CMOS technology, these STI trenches, which border transistor active areas are required according to the Design Rules Manual (DRM). However, we designed a new SPAD cell with a drastic reduction of the number of STI blocks placed over the active area of the SPAD (as shown schematically in Fig. 8). Simulated static  $I-V$  characteristics of the SPAD are analyzed to evaluate the impact of this modification on the electrical behavior of the SPAD: no significant modification of the dark current and  $V_{BD}$  was observed. Next, we carried out a study of the electrical field in the SCR and found that the three electrical field peaks due to the STI blocks included in the initial SPAD cell are no longer present for this new structure (red and

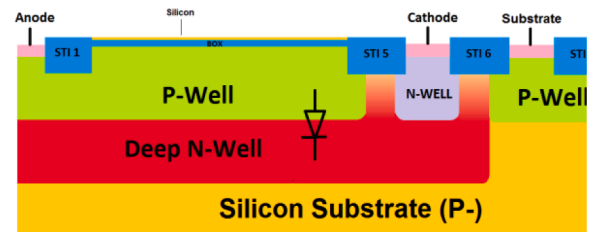


Fig. 8. Schematic view of the "Without STI trenches" SPAD structure (not to scale).

blue curves in Fig. 9). Moreover, we get same trends with the modified DNW presented in section 4.1 (purple and orange curves in Fig. 9). Note that the modification of the DNW results in a decrease of the average electric field in the SCR for the same relative excess voltage (i.e.  $V_{ex} \approx 10\%$  of  $V_{BD}$ ).

For transient simulations, we now observe that the current increases during the avalanche, collapses during the quenching phase, and recovers a value very close to its initial level (as shown in Fig. 10). In addition, since STI trenches were no longer present, the secondary avalanches do not occur, the charge density spreads along the p-region, and the current flows to the anode. Finally, the behavior of the quenching cycle corresponds to the one expected with three phases (as shown in Fig. 11): increase of the current during the avalanche (marker ①), decrease during the quenching (marker ②), and recharge to return to the metastable initial state (marker ③).

#### 4. Various approaches to improve SPAD FD-SOI behavior

Previous studies have been published with the objective to minimize, as much as possible, the relatively high DCR level measured in the native technology ( $\approx 500 \text{ Hz}/\mu\text{m}^2$  at 5% excess bias voltage i.e.  $V_{ex} \approx 0.5 \text{ V}$ ) and moreover to prevent the Premature Edge Breakdown (PEB).

In this section, firstly we introduce the modification of the DNW [17], then we detail the STI offset on the periphery of the active area [9]. Finally, we present a design of a structure combining all of these modifications.

##### 4.1. Deep N-well modification

The first optimization aims at increasing the breakdown voltage (reducing band-to-band tunneling) and relies on a deeper and less doped DNW [25] thanks to the modification of implantation conditions: 70% decrease of the dose and 25% increase of the energy [17]. Consequently, the PW/DNW junction is also deeper (as shown in Fig. 12), the SCR is expanded and the breakdown appeared for higher reverse bias voltage. TCAD simulation results and electro-optic characterization show similar trends. For the standard process with original DNW, at room temperature the breakdown voltage is approximately of 9.5 V, with the modified DNW,  $V_{BD}$  is now close to 16 V [17].

In addition, the enlargement of the SCR made possible to reduce the contribution of carriers generated by tunnel effect, resulting in a decrease of the measured DCR (as shown in Fig. 13). Note that all DCR measurements were performed thanks to an external transimpedance amplifier (passive quenching). With the modified DNW, we are able to extract, for the first time, a PDP value from our SPAD FD-SOI cell: 7% at 650 nm with 6% excess voltage (i.e.  $V_{ex} \approx 1.0 \text{ V}$  and  $V_{BD} \approx 16 \text{ V}$ ). Note

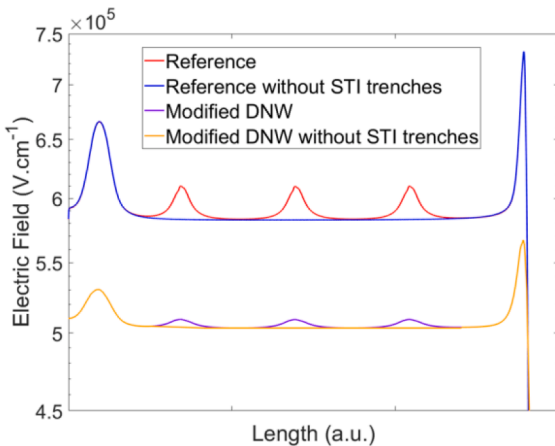


Fig. 9. Shape of the electric field in the SCR obtained with static simulations for different SPAD FD-SOI structures ( $V_{ex} \approx 10\%$  of  $V_{BD}$ ).

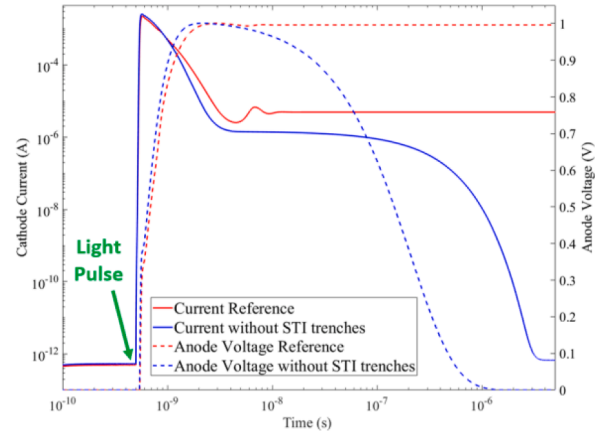


Fig. 10.  $I(t)$  and  $V(t)$  curves obtained with transient simulations on the reference and "Without STI trenches" SPAD structures.

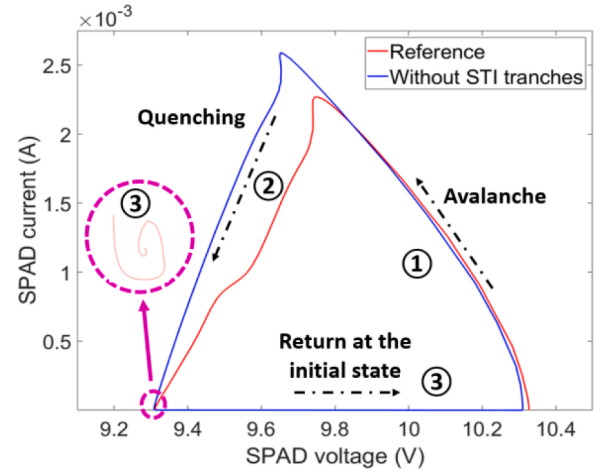


Fig. 11. Quenching cycles obtained with transient simulations on the reference and the "Without STI trenches" SPAD structures.

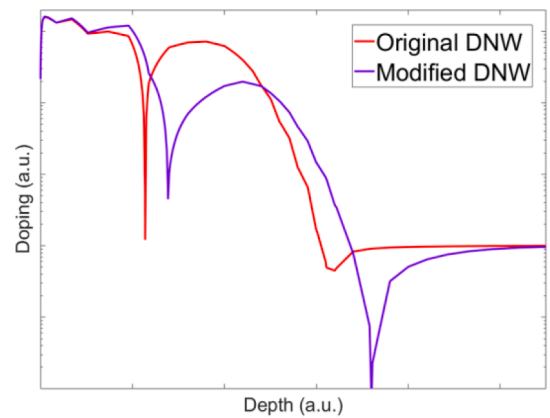
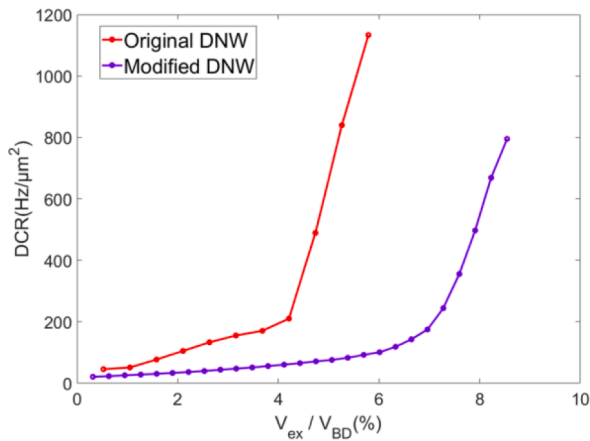


Fig. 12. Net doping profiles of the SPAD FD-SOI structure with the original DNW and the modified one.

that this relatively low PDP was obtained without any back-end of line modification (e.g. no antireflecting coating) and then is quite promising. Nevertheless, the DCR level remains very high in comparison with SPAD structures published in the literature.



**Fig. 13.** DCR measurements on SPAD FD-SOI structure with the original DNW and the modified one ( $\varnothing \approx 25 \mu\text{m}$ , measured at room temperature).

#### 4.2. STI offset on the edges of the active area

The realization of a SPAD structure in the native 28 nm FD-SOI CMOS technology presents a predominant breakdown on the edges of the active zone, and this despite the presence of a guard ring consisting of a retrograde DNW doping [8].

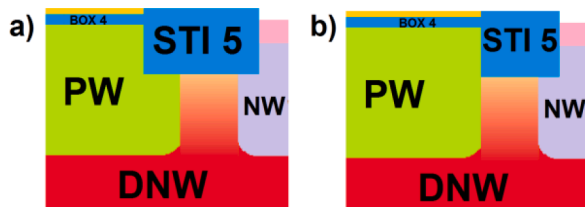
This problem seems to be related to the presence of the STI block on the edges of the active zone, which overlays the PW/DNW junction (as shown in Fig. 14a), and which could present a high defect concentration. Static TCAD simulations (with incorporation of defects at the Si/SiO<sub>2</sub> interface) revealed that the structure called “Aligned STI” (as shown in Fig. 14b) reduces the electric fields on the periphery of the space charge region and decreases the dark current [9].

The characterization of SPAD with this optimization has shown good agreement with simulation results [9]. The electroluminescence micro-cartography did not show a predominant breakdown on the edges of the active area,  $I$ – $V$  characteristics highlighted the decrease of the dark current, and the DCR measurements have shown an important decrease of the average level, with larger excess voltage range ( $>10\%$  of  $V_{BD}$ ). As shown in Fig. 15, this DCR improvement is achieved with both versions of the DNW. Moreover, the modified DNW associated with the alignment of the peripheral STI block (as shown in Fig. 14b), presents the best results: access to excess voltage of approximately 15–20% of  $V_{BD}$  ( $V_{ex} \approx 2.3$ – $3.1$  V) and an average DCR of  $\approx 100 \text{ Hz}/\mu\text{m}^2$  at 15% of  $V_{BD}$  (measured at room temperature).

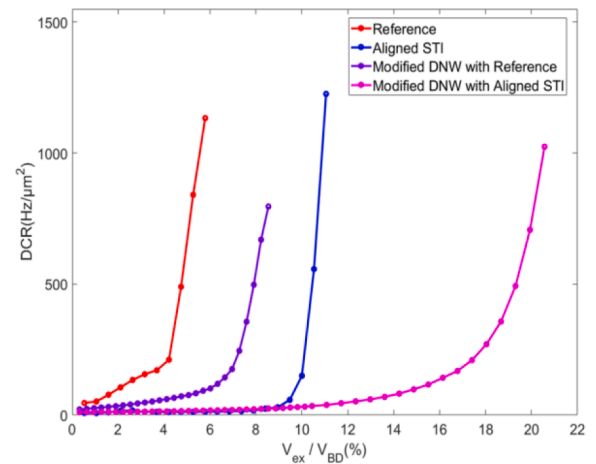
#### F. Combination of all optimization paths.

The native 28 nm FD-SOI technology requires the implementation of the SPAD with the original DNW, the presence of STI trenches over the active area, and the overlap of the peripheral STI block on the junction, in order to respect all design rules.

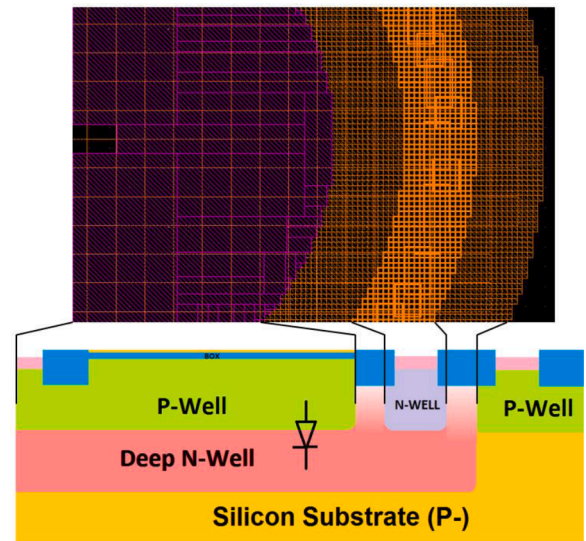
Regarding to the DNW modification, this does not require any violation of design rules while, the removal of STI trenches and the offset of the peripheral STI block result in changes on the SPAD layout with violation of at least three design rules. Fig. 16 shows a schematic view of the SPAD structure presenting these three modifications, associated with



**Fig. 14.** Illustration of the two studied STI layout configurations, a) reference and, b) Aligned STI (scales are not respected).



**Fig. 15.** DCR measurements on octagonal SPAD FD-SOI for the reference and the aligned STI structures with both versions of the DNW ( $\varnothing \approx 25 \mu\text{m}$ , measured at room temperature).



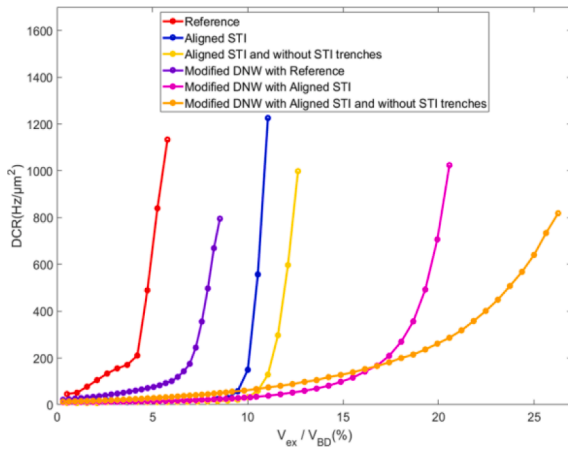
**Fig. 16.** Partial layout view of the quasi-circular SPAD FD-SOI with all optimizations and its correspondence with the schematic structure (scales are not respected).

its layout view. The manufacturing analysis indicates that local violations of the design rules should not impact the rest of the circuit so a test-chip including all optimization strategies (modified DNW, STI trenches removal onto active zone, STI trench alignment on the periphery) was fabricated, the measurements are presented in the following section.

#### 5. Dark Count Rate measurements

In this section, we present, in Fig. 17, the DCR measurements, at room temperature, for both versions of the DNW (original one for standard process and modified one) and various optimized SPAD FD-SOI architectures (with STI trenches removal above active zone, with STI trench alignment on the periphery).

For the original DNW (i.e. standard process), we confirm the results introduced in Fig. 15: the STI offset on the periphery of the diode allows DCR reduction as well as higher excess voltage operation (up to 10% of  $V_{BD}$ ). Considering the original DNW structure, the removal of all STI trenches above the active area makes possible some further significant improvement. Indeed, with the aligned STI structure, the DCR level at



**Fig. 17.** DCR measurements on octagonal SPAD FD-SOI for the reference, and the aligned with or without STI trenches structures, with both versions of the DNW ( $\varnothing \approx 25 \mu\text{m}$  and room temperature).

10% of  $V_{BD}$  (i.e.  $V_{ex} \approx 1.0 \text{ V}$ ) is about  $150 \text{ Hz}/\mu\text{m}^2$ , while SPAD combining aligned STI on the periphery and STI trenches removal above active zone gives a DCR level around  $35 \text{ Hz}/\mu\text{m}^2$ . In addition, this structure also allows DCR measurements up to an excess voltage of about 12% of  $V_{BD}$ .

For the modified DNW (detailed in section 4.1), same trends are observed with more pronounced improvements. Indeed, for the reference structure (modified DNW without STI optimization), the maximum excess voltage is close to 9% of  $V_{BD}$  ( $V_{ex} \approx 1.3 \text{ V}$ ). The implementation of the STI offset on the edges allows to operate up to 20% of  $V_{BD}$  ( $V_{ex} \approx 3.2 \text{ V}$ ). Finally, the removal of STI trenches above active zone further increases this value to 26% of  $V_{BD}$  ( $V_{ex} \approx 4.2 \text{ V}$ ). In addition, for this same structure, we also note a DCR decrease. At 20% of  $V_{BD}$  ( $V_{ex} \approx 3.1 \text{ V}$ ) and at room temperature, on the aligned STI structure, the DCR average level is close to  $700 \text{ Hz}/\mu\text{m}^2$ , while with the suppression of STI trenches, this level is only about  $260 \text{ Hz}/\mu\text{m}^2$ . Note that for lower excess voltages ( $<15\%$  of  $V_{BD}$ ), the DCR of the structure with aligned STI and trenches suppression is higher than the one of the structures with only the aligned STI. This appears to be mostly caused by measurement uncertainties (need more data for statistical analysis).

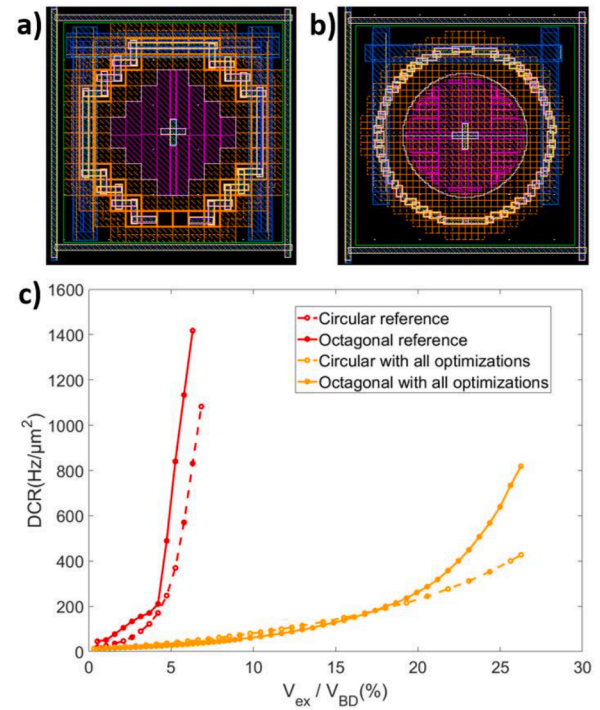
These differences highlight that optimizations are complementary to improve the dark count rate of SPAD implemented in 28 nm FD-SOI CMOS technology. The most efficient structure is the one with the modified DNW, the offset of the peripheral STI block, and the removal of STI trenches above the active zone.

Results, presented in Fig. 18, concern the DCR comparison for two SPAD shapes (octagonal and quasi-circular), highlighting that the quasi-circular SPAD FD-SOI features the best DCR performances by considering all optimization paths.

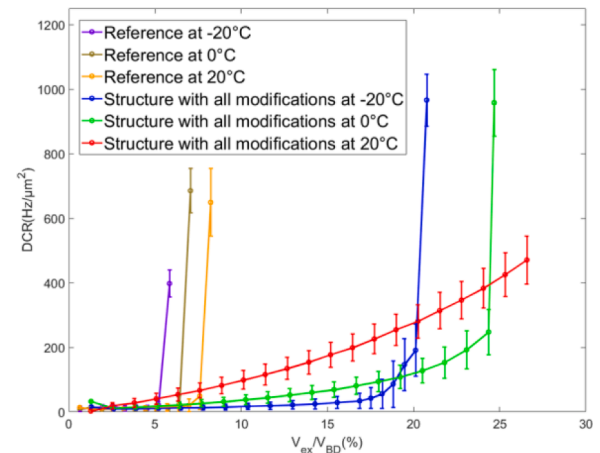
Last results, shown in Fig. 19, represent the DCR measured on a quasi-circular cell with the modified DNW for the reference structure and the one with all optimizations. These measurements are made for various temperatures, between 253 K and 293 K. The DCR improvement, due to layout modifications, is available for the entire temperature range tested.

## 6. Conclusion

In this study, we carried out transient TCAD simulations of avalanches for SPAD integrated in FD-SOI CMOS technology which considered the entire technological process. We showed that STI trenches localized above the SPAD's active area (imposed by the design rules) play a negative role during the avalanche quenching, because they prevent a fast carrier evacuation on the anode side, leading to possible multiple secondary avalanches in series. Thus, the removal of these STI



**Fig. 18.** Layout view of the SPAD in CMOS FD-SOI, a) octagonal cell and b) circular cell ( $\varnothing \approx 25 \mu\text{m}$ ). In c) DCR measurements on both cells for the reference structure and the one with all optimization paths (measured at room temperature).



**Fig. 19.** DCR measurements on the modified DNW for the reference structure and the one with all optimization paths (quasi-circular cell).

blocks allows for recovery of a correct avalanche quenching process.

We also reminded that various changes in the SPAD architecture such as the modification of the DNW implantation conditions, as well as the offset of the STI block located at the periphery of active zone, improve the electrical performance of the diode. These modifications reduce the dark current and the average DCR level, allow operating at higher excess voltages, and limit premature breakdown on the edges.

Based on these results, we have designed optimized SPAD structure implementing the modification of the DNW, the peripheral STI offset, and the removal of STI trenches located above the active zone. The first characterizations showed an important decrease in the dark count rate by the combination of these different optimization paths. Table 1 summarizes the main results obtained with optimized structures.

In addition, despite these DCR values are higher compared to the

**Table 1**

Summary of SPAD CMOS FD-SOI DCR performances for various architectures.

Structure		$V_{BD}(V)$ @20°C	Geometry	$V_{ex}^{max}$ (% of $V_{BD}$ )	DCR (Hz/ $\mu m^2$ )		
					5% of $V_{BD}$	10% of $V_{BD}$	20% of $V_{BD}$
Original DNW	Reference	9.5	Octagonal	$\approx 6$	$\approx 800$	–	–
			Circular	$\approx 7$	$\approx 200$	–	–
	Aligned peripheral STI		Octagonal	$\approx 11$	$\approx 15$	$\approx 150$	–
	Aligned peripheral STI without STI trenches		Octagonal	$\approx 13$	$\approx 10$	$\approx 35$	–
Modified DNW	Reference	15.8	Octagonal	$\approx 9$	$\approx 80$	–	–
			Octagonal	$\approx 20$	$\approx 15$	$\approx 30$	$\approx 700$
	Aligned peripheral STI		Octagonal	$\approx 26$	$\approx 25$	$\approx 60$	$\approx 260$
	Aligned peripheral STI without STI trenches		Circular	$\approx 26$	$\approx 20$	$\approx 60$	$\approx 230$

state of the art, the DCR improvement should allow us to carry out a full electro-optical characterization of SPAD integrated in 28 nm FD-SOI CMOS technology for a comprehensive study of the photon detection probability and the jitter. Current work will pursue focusing on  $I-V$  and DCR characterization varying temperature as well as micro-cartography of electroluminescence. Finally, a circuit integrating optimized SPAD FD-SOI structures and integrated advanced electronics (active quenching) was designed to assess the SPAD FD-SOI performances in real operating conditions.

### Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

### Acknowledgment

The authors would like to thank: the French National Research Agency (ANR-18-CE24-0010), the Nano2022 research program, CMP (Grenoble) for its IC prototyping service.

### References

- [1] Lee M-J, Charbon E. Progress in single-photon avalanche diode image sensors in standard CMOS: From two-dimensional monolithic to three-dimensional-stacked technology. *Jpn J Appl Phys* 2018;57(10):1002A3. <https://doi.org/10.7567/JJAP.57.1002A3>.
- [2] Henderson RK, Johnston N, Mattioli Della Rocca F, Chen H, Day-Uei Li D, Hungerford G, et al. A  $192 \times 128$  Time Correlated SPAD Image Sensor in 40-nm CMOS Technology. *IEEE J Solid-State Circ*, 2019, doi: 10.1109/JSSC.2019.2905163.
- [3] Charbon E. Single-photon imaging in complementary metal oxide semiconductor processes, *Philos Trans R Soc A: Math, Phys Eng Sci*, t. 372, p. 16.5.1-16.5.4, 2014, doi: 10.1098/rsta.2013.0100.
- [4] Acerbi F, Bisadi Z, Fontana G, Zorzi N, Piemonte C, Pavesi L. A Robust Quantum Random Number Generator Based on an Integrated Emitter-Photodetector Structure, In *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 24, no. 6, p. 1-7, Art no. 6101107, 2018, doi: 10.1109/JSTQE.2018.2814787.
- [5] Cova S, Ghioni M, Lacaita A, Samori C, Zappa F. Avalanche photodiodes and quenching circuits for single-photon detection. *Appl Opt* 1996;35:1956–76.
- [6] Tisa S, Zappa F, Tosi A, Cova S. Electronics for single photon avalanche diode arrays. *Sensors Actuators A/ Phys* 2007;140(1, 9):113–22. <https://doi.org/10.1016/j.sna.2007.06.022>.
- [7] Tisa S, Guerrieri F, Zappa F. Variable-Load Quenching Circuit for single-photon avalanche diodes. *Opt Express* 2008;16(3):2232–44. <https://doi.org/10.1364/OE.16.002232>.
- [8] Lakeh MD, Kammerer J-B, Aguinounon E, Issartel D, Schell J-B, Rink S, et al. An Ultrafast Active Quenching Active Reset Circuit with 50% SPAD Afterpulsing Reduction in a 28nm FD-SOI CMOS Technology using Body Biasing Technique. *MDPI Sensors* 2021;21(12):4014. <https://doi.org/10.3390/s21124014>.
- [9] Issartel D, Chaves de Albuquerque T, Clerc R, Pittet P, Cellier R, Golanski D, et al. SPAD FDSOI cell optimization for lower dark count rate achievement, 2020 Joint International EUROSIOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSIOI-ULIS), Caen, France, p. 1–5, 2020, doi: 10.1109/EUROSIOI-ULIS49407.2020.9365292.
- [10] Pellegrini S, Rae B, Pingault A, Golanski D, Jouan S, Lapeyre C, et al. Industrialised SPAD in 40 nm Technology, International Electron Devices Meeting (IEDM), p. 16.5.1–16.5.4, 2017, doi: 10.1109/IEDM.2017.8268404.

- [11] Lee M, Sun P, Charbon E. A first single-photon avalanche diode fabricated in standard SOI CMOS technology with a full characterization of the device. *Opt Express* 2015;23:13200–9. <https://doi.org/10.1364/OE.23.013200>.
- [12] Morimoto K. Megapixel SPAD cameras for time-resolved applications. Theses, EPFL 2021. <https://doi.org/10.5075/epfl-thesis-8773>.
- [13] Lee M-J, Ximenes AR, Padmanabhan P, Wang TJ, Huang KC, Yamashita Y, et al. A Back-Illuminated 3D-Stacked Single-Photon Avalanche Diode in 45nm CMOS Technology. International Electron Devices Meeting (IEDM). 2017. pp. 16.6.1-16.6.4. doi: 10.1109/IEDM.2017.8268405.
- [14] Vines P, Kuzmenko K, Kirdoda J, Dumas DCS, Mirza MM, Millar RW, et al. High performance planar germanium-on-silicon single-photon avalanche diode detectors. *Nat Commun* 2019;10. <https://doi.org/10.1038/s41467-019-08830-w>.
- [15] Chaves de Albuquerque T, Issartel D, Clerc R, Pittet P, Cellier R, Golanski D, et al. Indirect avalanche event detection of single photon avalanche diode implemented in CMOS FDSOI technology. *Solid-State Electron Elsevier* 2020;163:107636. <https://doi.org/10.1016/j.sse.2019.107636>.
- [16] Webster EAG, Grant LA, Henderson RK. Transient single-photon avalanche diode operation, minority carrier effects, and bipolar latch Up. *IEEE Trans Electron Devices* March 2013;60(3):1188–94. <https://doi.org/10.1109/TED.2013.2243152>.
- [17] Chaves de Albuquerque T, Issartel D, Clerc R, Pittet P, Cellier R, Calmon F. “Lowering the Dark Count Rate of SPAD Implemented in CMOS FDSOI Technology,” Conference EUROSIOI – ULIS 2019, pp. 1-4, 2019, doi: 10.1109/EUROSIOI-ULIS45800.2019.9041916.
- [18] Richardson JA, Grant LA, Henderson RK. Low dark count single-photon avalanche diode structure compatible with standard nanometer scale CMOS technology. *IEEE Photonics Technol Lett* 2009;21(14):1020–2. <https://doi.org/10.1109/LPT.2009.2022059>.
- [19] Richardson JA, Webster EAG, Grant LA, Henderson RK. Scaleable single-photon avalanche diode structures in nanometer CMOS technology. *IEEE Trans Electron Devices* 2011;58(7):2028–35. <https://doi.org/10.1109/TED.2011.2141138>.
- [20] Xu H, Pancheri L, Betta G-F-D, Stoppa D. Design and characterization of a p+n-well SPAD array in 150nm CMOS process. *Opt Express* 2017;25(11):12765–78. <https://doi.org/10.1364/OE.25.012765>.
- [21] Lu X, Law M-K, Jiang Y, Zhao X, Mak P-I, Martins RP. A 4- $\mu m$  diameter SPAD using less-doped N-well guard ring in baseline 65-nm CMOS. *IEEE Trans Electron Devices* 2020;65(5):2223–5. <https://doi.org/10.1109/TED.2020.2982701>.
- [22] *Sentaurus. Device User Guide*, 2018. [Online]. Available: <https://www.synopsys.com/silicon/tcad/device-simulation/sentaurus-device.html>.
- [23] Van Overstraeten R, De Man H. Measurement of the ionization rates in diffused silicon p-n junctions. *Solid-State Electron* 1970;13(5):583–608. [https://doi.org/10.1016/0038-1101\(75\)90099-4](https://doi.org/10.1016/0038-1101(75)90099-4).
- [24] Oussaiti Y, Rideau D, Manouvrier J-R, Wehbe-Alaouse H, Pellegrini S, Mamdy B, et al. “Behavior and Models for quench efficiency in Single-Photon Detection”, Single-Photon Workshop. Milan: Italy; Oct. 2019.
- [25] Gersbach M, Richardson J, Mazaleyrat E, Hardillier S, Niclass C, Henderson R, et al. A low-noise single-photon detector implemented in a 130nm CMOS imaging process. *Solid-State Electron* 2009;53(7):803–8. <https://doi.org/10.1016/j.sse.2009.02.014>.



**Dylan Issartel** (Eng. 2018, Ph.D. 2021) was attached to the Institut des Nanotechnologies de Lyon (INL UMR CNRS 5270, Université de Lyon, INSA Lyon, France), where he was a member of the “Electronics Devices” group. In the field of innovative concepts in 3D integrated devices and systems, he worked on the implementation of optimized SPAD structure in 28nm CMOS Fully Depleted Silicon on Insulator technology. He is now with STMicroelectronics, Crolles, France.