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Port characteristic and maximum power transfer for diode resistor circuits

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Abstract

This paper deals with the problems of computing port characteristics and maximum power transfer for 1–ports which contain (ideal) diodes, (positive) resistors and sources. The following are the main contributions.

1. An algorithm for solving circuits with (continuous positive slope) piecewise linear devices through repeated solution of circuits with primitive (single corner) versions of such devices. The number of repetitions is bounded above by the product of the number of devices and the product of the logarithms of the number of states (number of corners plus one) in the devices.
2. An adaptation of gradient descent methods for solving circuits with piecewise linear devices.
3. A linear time algorithm for the computation of port characteristic of a series parallel 1–port when the devices are piecewise linear and an approximation (of guaranteed level of accuracy) of the port characteristic when the device port characteristic is known approximately.
4. A simple algorithm for determining the region of validity and the maximum power transfer for a specified state of the diodes. When the number of states is polynomial in the number of diodes in the 1–port, this is used to give a polynomial time algorithm for the port characteristic.
5. An adaptation of efficient interior point methods for the solution of circuits with diodes, resistors and sources.

Keywords: Ideal diodes, Piecewise linear, Port characteristic, Maximum power, Interior point method.
2000 MSC: 94C05, 94C15

1. Introduction

The (ideal) diode is a powerful modelling tool in circuit theory. The simplest circuits which involve such devices are the circuits with sources, (positive) resistors and diodes. This class of circuits has come into prominence at the present time since they can be used to model solar cells ([1, 13]) to any required degree of accuracy.

In the late 50s, J.B.Dennis [5] showed that analysis of diode resistor source (DRS) circuits reduces to the solution of a quadratic programming problem. However, efficient algorithms for solving such problems were developed only in the 90s and later ([18], [15],[16]). Diode resistor 1–ports have continuous positive slope piecewise linear characteristics. The positive slope condition allows efficient methods of analysis. The study of the more general class of piecewise linear circuits without the positive slope condition has been undertaken by many workers (see [19], [12]).

In the case where these circuits are series parallel, their analysis can be performed extremely fast (linear time in the number of diodes). Series parallel graphs were studied in a fundamental way first by Duffin [6]. Panels of solar cells are series parallel combinations of such cells and therefore, in these cases, the online computations of port characteristics and power transfer can be performed accurately and fast.

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In this paper, we present a number of new methods for analysing diode resistor circuits keeping in mind present day needs and the state of the art of mathematical programming.

- We show that circuits with devices which have continuous positive slope piecewise linear characteristics, can be solved by repeatedly solving circuits, obtained by replacing these devices with ones which have only a single corner in their characteristics. Alternatively, we show that these circuits can be solved through a gradient descent algorithm which does not depend upon the number of corners in the device characteristics.
- We show that there is a linear time algorithm for computing the port characteristics of piecewise linear device 1– ports which have series parallel graphs. For such circuits, we also derive bounds on the error in the characteristics when the device characteristics are known only approximately.
- For a DRS 1– port, we give an algorithm for determining the region of validity and the maximum power transfer for a specified state of the diodes. When the number of states is polynomial in the number of diodes in the 1– port, this is used to give a polynomial time algorithm for computing the port characteristic.
- We adapt efficient interior point methods for the solution of DRS circuits.

In what follows, by DRS multiports, we mean diode resistor source circuits where the diodes and ports together contain no loops or cutsets and the sources are accompanied by positive resistors. The outline of the paper is as follows.

Section 2 contains the definition and the basic properties of DRS circuits. Among other things we show that DRS multiports have unique solution for a given port termination by voltage or current sources.

Section 3 contains a method for solving circuits with piecewise linear devices, as above, by repeated solution of appropriate DRS circuits with the same number of diodes as the number of the original devices. The number of repetitions is bounded by the product of the number of devices and the product of the logarithms of the number of states (number of corners plus one) of the devices.

Section 4 studies DRS circuits through the resistive multiport that results when the diodes are replaced by ports. We show that the port characteristic of DRS 1– ports has to be continuous piecewise linear with positive slope and with finite number of corners.

Section 5 is on the port connection graph for a 1– port built by connecting smaller 1– ports. The notion of a connection tree for series parallel graphs is defined.

Section 6 is on series parallel DRS 1– ports. A linear time algorithm for building the port characteristics of such 1– ports is given. It is shown that the port characteristic of a series parallel DRS 1– port has number of corners bounded by the number of diodes in the 1– port.

Section 7 is on approximate computation of port characteristic of series parallel 1– ports, when the port characteristic of the 1– ports composing them is only known approximately.

Section 8 deals with the computation of maximum power transfer for explicitly given piecewise linear characteristics and with the approximate computation when the port characteristic is not known explicitly.

Section 9 is on the region of validity and maximum power transfer for a specified state of diodes in the multiport. The ideas are used to give an algorithm for the explicit computation of port characteristics of DRS 1– ports. The algorithm requires solution of resistive networks corresponding to valid diode states. Given one valid state all states are successively computed by such solutions (twice for each diode state).

Section 10 is on the adaptation of gradient descent methods for solving circuits with piecewise linear devices.

Section 11 is on the quadratic programming formulation for DRS circuits and on an adaptation of polynomial time interior point methods for solving DRS circuits. It is shown that these methods essentially reduce to replacing the diode characteristic by hyperbolas close to the on-off voltage and current axes and moving from one hyperbola to another closer to the axes. Each step in the algorithm requires the solution of a resistive network obtained by replacing the diode by a suitable Thevenin circuit.

Appendix contains an informal derivation of necessary and sufficient conditions for optimality of convex programming problems.

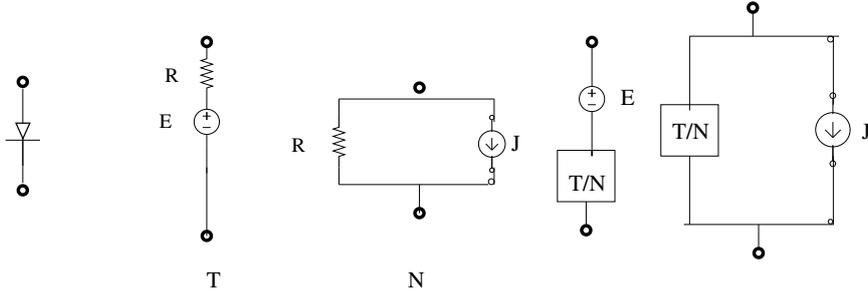


Figure 1: Basic components of a DRS network

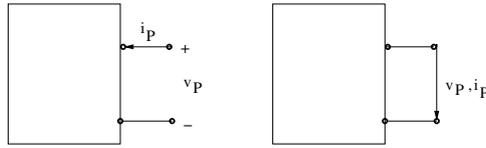


Figure 2: Port arrow convention

2. Diode resistor source (DRS) multiports

2.1. Preliminaries

Definition 1. An **ideal diode** has the $v - i$ characteristic $v \leq 0, i \geq 0, v \times i = 0$. We will call a multiport \mathcal{N}_P , (network \mathcal{N}) containing ideal diodes, positive resistors, current and voltage sources, a **DRS multiport (DRS network)** iff

1. there are no cutsets (minimal sets of edges which when deleted break up the graph) or loops of the graph of \mathcal{N}_P , containing only diodes and ports,
2. (see Figure 1) each current source occurs in parallel with a Norton circuit (positive resistor in parallel with a current source) or with a Thevenin circuit (positive resistor in series with a voltage source), each voltage source occurs in series with a Norton circuit or with a Thevenin circuit (in Figure 1, 'T/N' refers to 'Thevenin/Norton').

We will call a DRS 1– port primitive iff it contains only one diode and this diode occurs in series (parallel) with a Thevenin circuit or a Norton circuit with the combination in parallel (series) with a Thevenin or Norton circuit. (examples are in Figure B.7 (b) (c)).

Convention We take the current i_P in a port branch P to have direction opposite to the direction of the voltage v_P (see Figure 2).

The following result is from [5].

Theorem 2. Every DRS network has a solution.

The proof is by reducing the problem of solving the network to that of solving a convex quadratic programming problem (see Section 11).

Theorem 3. Let \mathcal{N}_P be a DRS multiport. Let some of the ports be terminated by voltage sources and others by current sources. Then the resulting network \mathcal{N} has a unique solution.

The proof is relegated to the appendix (see Appendix B).

An important method of determining port characteristic of DRS 1– ports involves computing characteristics of smaller DRS 1– ports which occur at intermediate stages, using these as devices in a reduced 1–

port (see Section 6 and 9.4). We prove later that $v - i$ characteristics of DRS 1- ports are piecewise linear with positive slope and a finite number of corners (Corollary 13). We now focus attention on such 1- ports treating them as devices. Theorem 4 assures us that the procedure is justified. The proof is given in the appendix (see Appendix B).

Theorem 4. *Let \mathcal{N}_P be a multiport with the ports containing no loops or cutsets and with devices whose $v - i$ characteristics are continuous piecewise linear with positive slope. Let some of the ports be terminated by voltage sources and others by current sources. Then the resulting network \mathcal{N} has a unique solution.*

For a piecewise linear characteristic, a **corner** refers to a point in the characteristic where the slope changes. Henceforth **piecewise linear** would mean continuous piecewise linear with positive slope and a finite number of corners.

The next result asserts that piecewise linear devices can be realized as DRS 1- ports. It is a straight forward application of the discussion of piecewise linear devices found in [3]. We omit the routine proof.

Lemma 5. *A piecewise linear device with $s - 1$ corners (s straight line segments) can be realized as a series parallel combination of $(s - 1)$ DRS 1- ports each with at most one diode. A piecewise linear device with 1 corner can be realized as a primitive DRS subcircuit.*

Example 29 in the appendix illustrates the idea behind the proof.

3. Solving networks with piecewise linear devices realized as DRS networks

We have seen that a network with piecewise linear devices can be solved as a DRS circuit (Lemma 5). However this would result in a network which has as many diodes as the sum of the number of line segments in the $v - i$ characteristics of all the devices. In this section we prove a result which states that repeated solution of networks with only as many diodes as the number of piecewise linear devices in the original network is sufficient. The number of such solutions to be computed is bounded by the number of devices times the product of the logarithms of the number of line segments in the $v - i$ characteristics of all the devices.

We call the straight line segments that make up the $v - i$ characteristic of a piecewise linear device, the **states** of the device. (In Figure 3(a), the piecewise linear device has 4 states, the segment to the left of (v_0, i_0) , the one between $(v_0, i_0), (v_1, i_1)$, the one between $(v_1, i_1), (v_2, i_2)$, and the segment to the right of (v_2, i_2) .) We call a piecewise linear device with only one corner (two states) in its $v - i$ characteristic, a **primitive piecewise linear device** and denote it by D . A primitive DRS subcircuit has such a $v - i$ characteristic (see Figure 3 (c)).

Definition 6. *Two piecewise linear devices agree over an open interval (v_1, v_2) ((i_1, i_2)) iff their $v - i$ curves are identical over (v_1, v_2) ((i_1, i_2)). We say a primitive piecewise linear device D **agrees** with a piecewise linear device L , iff its corner (v', i') is also a corner of the latter and the two agree with each other over an open interval containing v' (i'). (The primitive device in Figure 3 (c), agrees with the piecewise linear device in Figure 3 (a).)*

Definition 7. *Let \mathcal{N}_P be a multiport composed of piecewise linear devices L_1, \dots, L_n . We say a point (v'_j, i'_j) on the $v - i$ characteristic of L_j is to the **left of a corner** (**right of a corner**) $(v_j^{corner}, i_j^{corner})$ of the device L_j iff $v'_j \leq v_j^{corner}$ ($v'_j \geq v_j^{corner}$). Let v'_P (i'_P) be a port voltage (current) and let $(v'_P, i'_P), (v'_1, i'_1), \dots, (v'_n, i'_n)$ be the corresponding unique solution of \mathcal{N}_P (Theorem 4). We say the solution is to the **left of a corner** (**right of a corner**) $(v_j^{corner}, i_j^{corner})$ of the device L_j iff $v'_j \leq v_j^{corner}$ ($v'_j \geq v_j^{corner}$).*

We now have a result which reduces the solution of a network containing piecewise linear devices, to that of networks each of which has primitive piecewise linear devices, in place of the piecewise linear devices of the former.

Theorem 8. *Let \mathcal{N}_P be a multiport on graph \mathcal{G}_P , with its ports containing no loops or cutsets and composed of devices $L_1, \dots, L_k, T_{k+1}, \dots, T_n$, where the L_i are piecewise linear and the T_j , Thevenin circuits.*

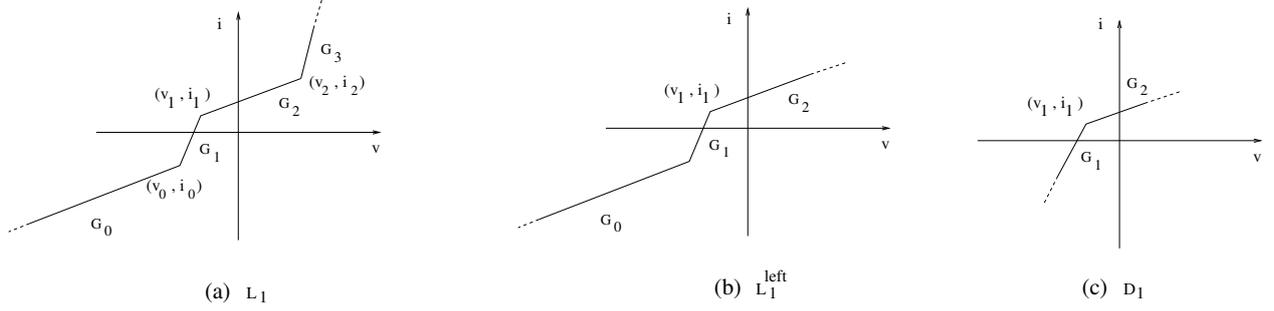


Figure 3: Devices L_1, L_1^{left}, D_1

1. Let $\mathcal{N}_P^{reduced}$ be the multiport on graph \mathcal{G}_P , composed of piecewise linear devices $D_1, L_2, \dots, L_k, T_{k+1}, \dots, T_n$, with the primitive piecewise linear device D_1 agreeing with L_1 . Let v'_P (i'_P) be a port voltage (current) of \mathcal{N}_P and $\mathcal{N}_P^{reduced}$ and let $(v'_P, i'_P), (v'_1, i'_1), \dots, (v'_n, i'_n), (v'_P, i'_P), (v_1^{reduced}, i_1^{reduced}), \dots, (v_n^{reduced}, i_n^{reduced})$, be the corresponding unique solutions of $\mathcal{N}_P, \mathcal{N}_P^{reduced}$, respectively. Let (v_1, i_1) be the common corner of D_1, L_1 . Then, (v'_1, i'_1) lies to the left (right) of (v_1, i_1) in \mathcal{N}_P iff $(v_1^{reduced}, i_1^{reduced})$ lies to the left (right) of (v_1, i_1) in $\mathcal{N}_P^{reduced}$.
2. Let L_j have s_j states for $j = 1, \dots, k$, and let $s^r := \Pi_r^k(\log_2(s_j))$. Then in the solution of \mathcal{N}_P for the given port voltage (current), the states of L_1, \dots, L_k , can be computed by solving $\Sigma_1^k s^r$ reduced multiports with the same input port voltage (current) and with L_1, \dots, L_k , replaced with either fixed Thevenin circuits or suitable primitive devices agreeing with them and with T_{k+1}, \dots, T_n as before.

Proof. 1. We use the fact that piecewise linear multiports with no loops or cutsets within their set of ports have unique solutions for any given v'_P (i'_P) (Theorem 4). In the following argument we use port voltage v_P as the input. Clearly the same argument is valid with port current i_P as the input.

Let L_1^{left} be a piecewise linear device which agrees with L_1 to the left of (v_1, i_1) and agrees with D_1 to the right of (v_1, i_1) (see Figure 3). Note that L_1^{left} has a continuous positive slope $v - i$ characteristic. Let \mathcal{N}_P^{left} be the multiport on graph \mathcal{G}_P , obtained by retaining all devices except L_1 but replacing L_1 with L_1^{left} (see Figure 3). Since all its devices are piecewise linear, \mathcal{N}_P^{left} has a unique solution when the port voltage is v'_P . In the unique solution of \mathcal{N}_P corresponding to v'_P , let the state of L_1 lie to the left of (v_1, i_1) . It is clear that this solution would also satisfy the constraints of \mathcal{N}_P^{left} and therefore, must be its unique solution corresponding to v'_P . Next let $\mathcal{N}_P^{reduced}$ be the multiport obtained by retaining all devices except L_1 but replacing L_1 with D_1 . Suppose in its solution, the state of L_1 lies to the right of (v_1, i_1) . But this solution would also satisfy the constraints of \mathcal{N}_P^{left} which violates the uniqueness of solution of \mathcal{N}_P^{left} . We conclude that the unique solution of $\mathcal{N}_P^{reduced}$ corresponding to v'_P lies to the left of (v_1, i_1) . By a similar argument it follows that if in \mathcal{N}_P the unique solution corresponding to v'_P lies to the right of (v_1, i_1) , the unique solution of $\mathcal{N}_P^{reduced}$ corresponding to v'_P also lies to the right of (v_1, i_1) .

2. In the following argument, the Thevenin circuits T_{k+1}, \dots, T_n , are left unchanged throughout.

To determine the state of L_1 , we can check whether the state lies to the left or right of the corner that is picked, each time solving a circuit with a suitable primitive piecewise linear device D_1 and devices L_2, \dots, L_k , as before. This binary search on the states, requires us to solve $\log_2(s_1)$ such circuits.

To obtain the state of L_k when L_1, \dots, L_{k-1} are replaced with fixed primitive devices $\hat{D}_1, \dots, \hat{D}_{k-1}$ and L_k , as before, we need to solve $\log_2(s_k)$ circuits with L_1, \dots, L_k replaced $\hat{D}_1, \dots, \hat{D}_{k-1}, D_k$, where D_k is a primitive device chosen appropriately for binary search.

Assume that to obtain the state of L_r when L_1, \dots, L_{r-1} are replaced with fixed primitive devices $\hat{D}_1, \dots, \hat{D}_{r-1}$ and L_r, \dots, L_k as before, we need to solve $\Pi_r^k \log_2(s_j)$ circuits with L_1, \dots, L_k replaced with $\hat{D}_1, \dots, \hat{D}_{r-1}, D_r, \dots, D_k$ where D_r, \dots, D_k are primitive devices chosen appropriately for binary search.

Therefore, to obtain the state of L_{r-1} when L_1, \dots, L_{r-2} are replaced with fixed primitive devices

$\hat{D}_1, \dots, \hat{D}_{r-2}$ and L_{r-1}, \dots, L_k as before, we need to solve $(\Pi_r^k \log_2(s_j)) \times \log_2(s_{r-1})$ circuits with L_1, \dots, L_k replaced with $\hat{D}_1, \dots, \hat{D}_{r-2}, D_{r-1}, \dots, D_k$ where D_{r-1}, \dots, D_k are primitive devices chosen appropriately for binary search.

It follows that to obtain the state of L_1 we need to solve $(\Pi_1^k \log_2(s_j))$ circuits with L_1, \dots, L_k replaced with D_1, \dots, D_k primitive devices chosen appropriately for binary search.

If we know the state l_1 of L_1 in \mathcal{N} , we can replace it by a Thevenin circuit T_1 whose $v - i$ characteristic is the straight line obtained by extending the straight line segment l_1 to $-\infty$ and $+\infty$. Finding the state of L_2 in the network with devices $T_1, L_2, \dots, L_k, T_{k+1}, \dots, T_n$ requires by the above argument, solution of $\Pi_2^k \log_2(s_j)$ circuits with L_1, \dots, L_k , replaced with T_1, D_2, \dots, D_k where D_2, \dots, D_k are primitive devices chosen appropriately for binary search. In general finding the state of L_r in the network with $T_1, \dots, T_{r-1}, L_r, \dots, L_k, T_{k+1}, \dots, T_n$ requires by the above argument solution of $\Pi_r^k \log_2(s_j)$ circuits with L_1, \dots, L_k replaced with $T_1, \dots, T_{r-1}, D_r, \dots, D_k$ where D_r, \dots, D_k are primitive devices chosen appropriately for binary search. This proves the result. \square

Example 9. Let \mathcal{N} be the network obtained by connecting a voltage source of value v_P at the port. Let \mathcal{N} have piecewise linear devices D_1, D_2, D_3, L_4, L_5 . Let us suppose that the corners of L_4 occur at $(v_1, i_1), (v_2, i_2), (v_3, i_3)$, and let the corresponding states moving from $v_P = -\infty$ to $v_P = +\infty$, be $s_{40}, s_{41}, s_{42}, s_{43}$. Let D_{41}, D_{42}, D_{43} , be primitive devices which have corners at $(v_1, i_1), (v_2, i_2), (v_3, i_3)$, respectively and agree with L_4 . Let us call the states of D_{41} , s_{40}, s_{41} *rightextended*, the states of D_{42} , s_{41} *leftextended*, s_{42} *rightextended*, and the states of D_{43} , s_{42} *leftextended*, s_{43} .

To solve the resulting network \mathcal{N} , the binary search starts with the network \mathcal{N}_{middle} obtained by replacing D_1, D_2, D_3, L_4, L_5 in \mathcal{N} , by $D_1, D_2, D_3, D_{42}, L_5$, respectively. Suppose the state of D_{42} in this solution is s_{42} *rightextended*. This means that the state of L_4 in the solution of \mathcal{N} is to the right of (v_2, i_2) . In general this means that we now have to move to the ‘middle’ corner to the right of (v_2, i_2) , and replace L_4 by the corresponding primitive device. In the present case the corner is (v_3, i_3) and the primitive device is D_{43} . So we replace D_1, D_2, D_3, L_4, L_5 in \mathcal{N} , by $D_1, D_2, D_3, D_{43}, L_5$, respectively. Suppose in the solution, D_{43} is in state s_{42} *leftextended*. We conclude that in the solution of \mathcal{N} , the state of L_4 is to the left of (v_3, i_3) , and to the right of (v_2, i_2) , i.e., in state s_{42} .

Next consider the problem of finding the state of L_5 in the circuit where the devices are $D_1, D_2, D_3, D_{4j}, L_5$. This we do by solving the circuits with devices $D_1, D_2, D_3, D_{4j}, D_{5i}$, keeping D_1, D_2, D_3, D_{4j} fixed but varying D_{5i} according to the requirement of the binary search. We have to do this $\log(s_5)$ times. Note that the states of L_5 that we compute with say D_1, D_2, D_3, D_{4j} and with $D_1, D_2, D_3, D_{4r}, r \neq j$, need have nothing to do with each other and also nothing to do with its state in the final solution.

Thus to determine the state of L_4 in \mathcal{N} (devices D_1, D_2, D_3, L_4, L_5) we have to solve $\log(s_4) \times \log(s_5) = 2\log(s_5)$ circuits with devices $D_1, D_2, D_3, D_{4j}, D_{5r}$, where D_{4j}, D_{5r} are chosen according to binary search.

4. Diode elimination multiport of a DRS multiport

Definition 10. Let D_1, \dots, D_k , be the diodes of a DRS multiport \mathcal{N}_P (network \mathcal{N}). By a **state** of the diodes we mean an ordered pair $(\mathcal{D}_1, \mathcal{D}_2)$ where $\mathcal{D}_1 \subseteq \{D_1, \dots, D_k\}$ and $\mathcal{D}_2 := \{D_1, \dots, D_k\} - \mathcal{D}_1$. The multiport is said to be at a state $(\mathcal{D}_1, \mathcal{D}_2)$ for a particular port condition iff for that port condition $i_{\mathcal{D}_1}$ is nonnegative, $v_{\mathcal{D}_1} = 0_{\mathcal{D}_1}$, and $v_{\mathcal{D}_2}$ is nonpositive, $i_{\mathcal{D}_2} = 0_{\mathcal{D}_2}$. A diode state that occurs for some port condition of \mathcal{N}_P is said to be a **valid state** of \mathcal{N}_P . The multiport $\mathcal{N}_P^{\mathcal{D}_1, \mathcal{D}_2}$ (network $\mathcal{N}^{\mathcal{D}_1, \mathcal{D}_2}$) at $(\mathcal{D}_1, \mathcal{D}_2)$ of \mathcal{N}_P (\mathcal{N}) is obtained by contracting \mathcal{D}_1 and deleting \mathcal{D}_2 . We will refer to the diode state at $v_P = -\infty$ as the **initial state** and that at $v_P = +\infty$ as the **final state**.

Definition 11. Let \mathcal{N}_P be a DRS multiport. We say $\mathcal{N}_{\mathcal{D}P}$ is the **diode elimination multiport** of \mathcal{N}_P iff $\mathcal{N}_{\mathcal{D}P}$ has ports in place of the diodes of \mathcal{N}_P with the resistors, sources and the ports P unchanged.

Theorem 12. Let $\mathcal{N}_{\mathcal{D}P}$ be the diode elimination multiport of a DRS multiport \mathcal{N}_P . Let $(\mathcal{D}_1, \mathcal{D}_2)$ be a state of the diodes of \mathcal{N}_P . Then $\mathcal{N}_{\mathcal{D}P}$ has a hybrid port representation

$$\begin{pmatrix} i_{\mathcal{D}_1} \\ v_{\mathcal{D}_2} \\ v_P \end{pmatrix} = \begin{pmatrix} g_{\mathcal{D}_1\mathcal{D}_1} & h_{\mathcal{D}_1\mathcal{D}_2} & h_{\mathcal{D}_1P} \\ h_{\mathcal{D}_2\mathcal{D}_1} & r_{\mathcal{D}_2\mathcal{D}_2} & r_{\mathcal{D}_2P} \\ h_{P\mathcal{D}_1} & r_{P\mathcal{D}_2} & r_{PP} \end{pmatrix} \begin{pmatrix} v_{\mathcal{D}_1} \\ i_{\mathcal{D}_2} \\ i_P \end{pmatrix} + \begin{pmatrix} J_{\mathcal{D}_1} \\ E_{\mathcal{D}_2} \\ E_P \end{pmatrix} \quad (1)$$

and $\mathcal{N}_P^{\mathcal{D}_1, \mathcal{D}_2}$ has the Thevenin representation

$$v_P = r_{PP}i_P + E_P, \quad (2)$$

where r_{PP} is a symmetric positive definite matrix.

Proof. Since \mathcal{N}_P is a DRS multiport, there are no loops or cutsets containing only diodes and ports. Therefore, the ports $\mathcal{D} \uplus P$ of $\mathcal{N}_{\mathcal{D}P}$ contain no loops or cutsets. Suppose the ports of multiport $\mathcal{N}_{\mathcal{D}P}$ are terminated by voltage sources at some of the ports and current sources at the others. The resulting network has only positive resistors, current and voltage sources. The voltage sources at the ports contain no loops and since each internal voltage source occurs in series with a Thevenin or Norton circuit, all the voltage sources together contain no loops. The current sources at the ports contain no cutsets and since each internal current source occurs in parallel with a Thevenin or Norton circuit, all the current sources together contain no cutsets. Therefore, this network has a unique solution and the currents and voltages at the ports of $\mathcal{N}_{\mathcal{D}P}$ are uniquely determined. Therefore $\mathcal{N}_{\mathcal{D}P}$ has every possible hybrid representation (corresponding to some ports as current input and others as voltage input ports). By the same argument $\mathcal{N}_P^{\mathcal{D}_1, \mathcal{D}_2}$ also has every possible hybrid representation including the Thevenin representation, $v_P = r'_{PP}i_P + E'_P$. Since the multiport $\mathcal{N}_P^{\mathcal{D}_1, \mathcal{D}_2}$ has only positive resistors and sources, we must have r'_{PP} as a symmetric positive definite matrix. The Thevenin representation of $\mathcal{N}_P^{\mathcal{D}_1, \mathcal{D}_2}$ can be obtained from the hybrid representation in Equation 1 by setting voltages $v_{\mathcal{D}_1}$ and currents $i_{\mathcal{D}_2}$, to zero. We conclude that $r'_{PP} = r_{PP}$, $E'_P = E_P$. The result follows. \square

Corollary 13. The $v - i$ characteristic of a DRS 1- port \mathcal{N}_P is continuous piecewise linear with positive slope and with the number of straight line segments bounded by 2^k , where k is the number of diodes in the 1- port.

Proof. By Theorem 3, we know that port voltage v_P is a function of the port current i_P . From Theorem 12, it is clear that the port voltage v_P is a positive slope affine function of the port current i_P for each valid diode state. We note that the solution space of Equation 1 is convex when the diode state is fixed, i.e., if $(i'_{\mathcal{D}_1}, v'_{\mathcal{D}_2}, i'_P, v'_P), (i''_{\mathcal{D}_1}, v''_{\mathcal{D}_2}, i''_P, v''_P), i_{\mathcal{D}_1} \geq 0, v_{\mathcal{D}_1} = 0_{\mathcal{D}_1}, v_{\mathcal{D}_2} \leq 0, i_{\mathcal{D}_2} = 0_{\mathcal{D}_2}$, are two solutions, their convex combination also is a solution of the inequalities. (To avoid confusion we have taken the diode port current direction the same as the diode voltage direction.) Since the circuit has a unique solution for any port current i_P this convex combination is the unique solution for the corresponding combination of port currents. Therefore if the diode states are the same at i'_P, i''_P , between the two currents also they would be the same.

The continuity of the function is clear as long as the diode state remains the same. We now examine the situation where the diode state changes. For a particular port current i'_P , let \mathcal{D}'_{11} (\mathcal{D}'_{22}) be the set of diodes where the current (voltage) in the diode is positive (negative) and let \mathcal{D}'_{12} be the set of diodes for which both the current and voltage are equal to zero. We will say the state $(\mathcal{D}_1, \mathcal{D}_2)$ is compatible with the partition $(\mathcal{D}'_{11}, \mathcal{D}'_{22}, \mathcal{D}'_{12})$ of the set of diodes iff $\mathcal{D}'_{11} \subseteq \mathcal{D}_1$ and $\mathcal{D}'_{22} \subseteq \mathcal{D}_2$. Note that the diode state for port current i'_P is in general non unique. A state for port current i'_P can be regarded as $(\mathcal{D}''_1, \mathcal{D}''_2)$ iff the latter is compatible with $(\mathcal{D}'_{11}, \mathcal{D}'_{22}, \mathcal{D}'_{12})$. It is clear from Equation 1, that for each diode state compatible with $(\mathcal{D}'_{11}, \mathcal{D}'_{22}, \mathcal{D}'_{12})$, the diode current (voltage) can be written as an affine function of the port current i_P . Let i'_d be the positive current in the diode $d \in \mathcal{D}'_{11}$ and let v'_d be the negative voltage in the diode $d \in \mathcal{D}'_{22}$.

Suppose we alter the port current to $i'_P + \Delta i_P$ in such a way that the current $i'_d + \Delta i_d$ in each diode $d \in \mathcal{D}'_{11}$ remains positive and the voltage $v'_d + \Delta v_d$ in each diode $d \in \mathcal{D}'_{22}$ remains negative. It follows that for the port current $i'_P + \Delta i_P$, the new diode state $(\mathcal{D}''_1, \mathcal{D}''_2)$ can be taken to be compatible with

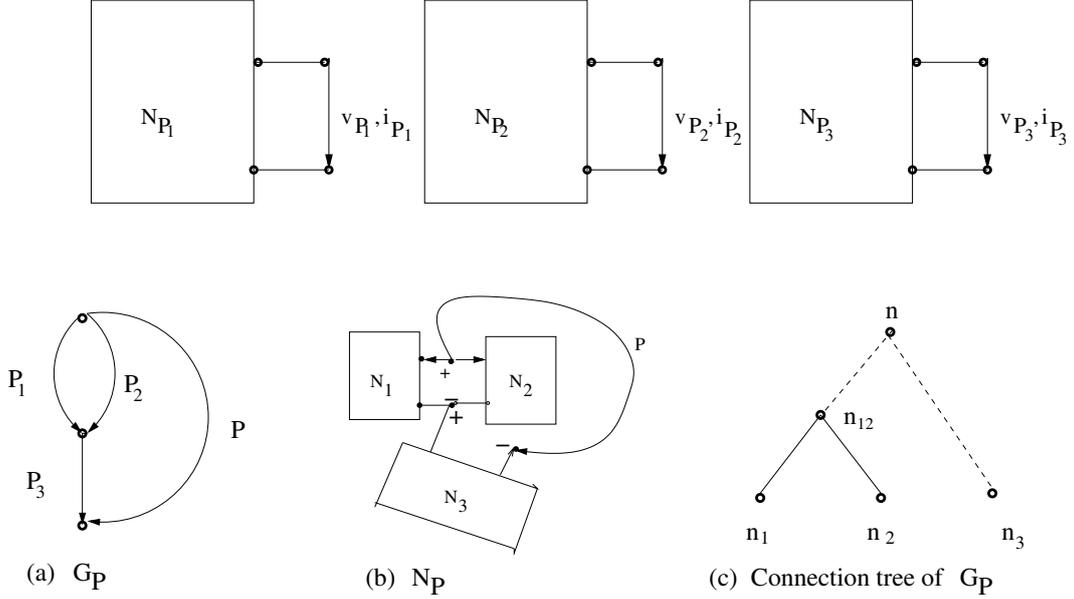


Figure 4: Connection of 1- ports according to port connection graph

$(\mathcal{D}'_{11}, \mathcal{D}'_{22}, \mathcal{D}'_{12})$. Because $(\mathcal{D}''_1, \mathcal{D}''_2)$ is compatible with $(\mathcal{D}'_{11}, \mathcal{D}'_{22}, \mathcal{D}'_{12})$, it can also be taken to be the diode state when the port current is i'_P . We then have the relationship $r^{(\mathcal{D}''_1, \mathcal{D}''_2)} \Delta i_P = \Delta v_P$ for the diode state $(\mathcal{D}''_1, \mathcal{D}''_2)$, where $r^{(\mathcal{D}''_1, \mathcal{D}''_2)}$ is positive. Let $r = \max_{\{(\mathcal{D}_1, \mathcal{D}_2)\}} r^{(\mathcal{D}_1, \mathcal{D}_2)}$, where $(\mathcal{D}_1, \mathcal{D}_2)$ is compatible with $(\mathcal{D}'_{11}, \mathcal{D}'_{22}, \mathcal{D}'_{12})$. If $v'_P + \Delta v_P$ is the port voltage corresponding to port current $i'_P + \Delta i_P$, we therefore have $|\Delta v_P| \leq r |\Delta i_P|$. Thus v_P is a continuous function of i_P .

From the above argument about convexity of the solution space when the diode state is the same, it follows that once the circuit has moved away from a diode state when $v_P(i_P)$ is increased, with a further increase, it cannot return to it. Thus the total number of diode states encountered between any port conditions $(v^1_P, i^1_P), (v^2_P, i^2_P), v^1_P < v^2_P, i^1_P < i^2_P$, cannot exceed 2^k , where k is the number of diodes in the DRS circuit. Each diode state is equivalent to one straight line segment and therefore the result follows. \square

Corollary 14. *The $v - i$ characteristic of a primitive DRS 1- port \mathcal{N}_P is piecewise linear with only two straight line segments.*

Proof. Connect a current source J to the single port of \mathcal{N}_P and vary its value from $-\infty$ to $+\infty$. Let the 1- port seen by the single diode, when it is pulled out, be denoted by P_D and let this have a Thevenin equivalent $v_{P_D} = r i_{P_D} + E_1 + \alpha J$, where E_1 depends on the sources within \mathcal{N}_P and is constant. (Note that r is positive and we must have $i_{P_D} \leq 0$ since this port current is opposite to the diode current.) Suppose, without loss of generality, $v_{P_D} = -\infty$ when $J = -\infty$ so that $i_{P_D} = 0$, and α is positive. It is clear that as J increases, the state of the diode remains the same till $E_1 + \alpha J = 0$. When J increases beyond this value, $E_1 + \alpha J$ becomes positive and we must have $i_{P_D} \leq 0, v_{P_D} = 0$. Thus as J increases from $-\infty$ to $+\infty$ the diode changes state only once so that the $v - i$ characteristic of \mathcal{N}_P is piecewise linear with only one corner and two straight line segments. \square

5. Connection of 1- ports according to port connection graph

The **port connection graph** \mathcal{G}_P is a directed graph with edge set $\{P, P_1, \dots, P_k\}$. Let the port edges of $\mathcal{N}_{P_1}, \dots, \mathcal{N}_{P_k}$, be identified with P_1, \dots, P_k , with the same orientation. The resulting graph has as edge

set, the union of the singleton set $\{P\}$ with the edge sets of the \mathcal{N}_{P_j} . Let the edges P_1, \dots, P_k be deleted and let the device characteristic of the internal devices of the 1- ports be as before. The resulting 1- port \mathcal{N}_P is said to be a connection of 1- ports $\mathcal{N}_{P_1}, \dots, \mathcal{N}_{P_k}$, according to port connection graph \mathcal{G}_P . (See Figure 4 (a) and (b).) To compute the port characteristic of \mathcal{N}_P we can first compute the port characteristics of $\mathcal{N}_{P_1}, \dots, \mathcal{N}_{P_k}$, and define a new 1- port $\mathcal{N}_P^{reduced}$ on graph \mathcal{G}_P . If the \mathcal{N}_{P_j} are DRS multiports, then the edges P_j of \mathcal{G}_P can be taken to have the piecewise linear port characteristic of \mathcal{N}_{P_j} as the device characteristic. These ideas are particularly relevant where \mathcal{G}_P is a series parallel graph. This case is discussed below.

Let $\mathcal{G}_{P_1}, \mathcal{G}_{P_2}$, have only the end points n_1, n_2 of P_1 and P_2 in common. A **parallel** connection \mathcal{G}_P of graphs $\mathcal{G}_{P_1}, \mathcal{G}_{P_2}$, is built as follows. We attach $\mathcal{G}_{P_1}, \mathcal{G}_{P_2}$, at n_1, n_2 and add the edge P between n_1, n_2 and then delete P_1, P_2 .

Let $\mathcal{G}_{P_3}, \mathcal{G}_{P_4}$, have a single node n in common which is an end point of both P_3 and P_4 . A **series** connection \mathcal{G}_P of graphs $\mathcal{G}_{P_3}, \mathcal{G}_{P_4}$, is built as follows. We attach $\mathcal{G}_{P_3}, \mathcal{G}_{P_4}$, at n and add the edge P between the other two end points of P_3, P_4 and then delete P_3, P_4 .

We say \mathcal{G}_P is **series parallel** iff it has a single edge and no isolated vertices **or** if it is a series or parallel combination of series parallel graphs with fewer edges. If the port connection graph \mathcal{G}_P on edge set $\{P, P_1, \dots, P_k\}$ is series parallel, we say \mathcal{N}_P is a **series parallel connection** of 1- ports $\mathcal{N}_{P_1}, \dots, \mathcal{N}_{P_k}$, according to port connection graph \mathcal{G}_P .

Definition 15. When 1- ports $\mathcal{N}_{P_1}, \mathcal{N}_{P_2}$, are connected in parallel or in series to result in 1- port \mathcal{N}_P , the direction of the port edges is said to be aligned, iff

- when in parallel, the port edges P_1, P_2, P , all leave or all enter the common nodes and
- when in series, P_1 enters the common node and P_2 leaves it, and P_1, P , both leave their common node and P_2, P , both enter their common node.

Remark 1. If the multiports being connected are not aligned, we have to reverse the port direction of one of the multiports, in order to align them. This would mean that the $v-i$ characteristic of that multiport has both $v-$ and $i-$ axis flipped. This would not change the slopes but would change the position of the corners ((v', i') becomes $(-v', -i')$). This alignment is required so that we can add the $v-i$ characteristics along the $v-$ or the $i-$ direction, as the case may be, in order to compute the characteristics of the resulting multiport.

Remark 2. Let \mathcal{N}_P be a series-parallel connection of primitive multiports with \mathcal{G}_P as its port connection diagram, but with its direction of edges unknown. There is a linear time algorithm [17] which decomposes \mathcal{G}_P into series-parallel combination of single edges. If at every level of series or parallel combination, we take care to align the corresponding multiports, for a specified direction of the port edge, all the edges of \mathcal{G}_P would be directed so that they correspond to aligned series-parallel connections.

Remark 3. We give a sketch of an algorithm for decomposing \mathcal{G}_P into series or parallel combination of smaller subgraphs, if such a combination exists.

We will suppose that \mathcal{G}_P does not have cut vertices, i.e., vertices whose deletion disconnects the graph. Let v_1, v_2 be the endpoints of P in \mathcal{G}_P . Delete P . Let \mathcal{G} be the resulting graph. Start a dfs tree at v_1 and proceed until you reach v_2 avoiding it as much as possible, back tracking if required. Let E_2 be all the edges covered when back tracking from v_2 up to v_1 . If $E_2 \neq E(\mathcal{G})$, let \mathcal{G}_2 be the subgraph on E_2 and let \mathcal{G}_1 be the subgraph on $E(\mathcal{G}) - E_2$. Add P_1, P_2 to $\mathcal{G}_1, \mathcal{G}_2$, respectively across v_1, v_2 and let $\mathcal{G}_{P_1}, \mathcal{G}_{P_2}$, be the resulting graphs. Then \mathcal{G}_P would be a parallel combination of $\mathcal{G}_{P_1}, \mathcal{G}_{P_2}$.

Suppose $E_2 = E(\mathcal{G})$. By examining the back edges of the above dfs tree, a cut vertex of \mathcal{G} would have been revealed, if it exists. Suppose v_3 is such a cut vertex. Let E_3 be the edges covered while backtracking from v_2 to v_3 , and let $E_1 = E(\mathcal{G}) - E_2$. Let \mathcal{G}_1 be the subgraph on $E(\mathcal{G}) - E_2$. Add P_1 across v_1, v_3 , to \mathcal{G}_1 and add P_2 across v_3, v_2 , to \mathcal{G}_2 . Let $\mathcal{G}_{P_1}, \mathcal{G}_{P_2}$, be the resulting graphs. Then \mathcal{G}_P would be a series combination of $\mathcal{G}_{P_1}, \mathcal{G}_{P_2}$.

Definition 16. The **connection tree** of a series parallel 1- port \mathcal{N}_P (graph \mathcal{G}_P) is defined as follows. The connection tree of a DRS 1- port \mathcal{N}_P , whose graph \mathcal{G}_P is a single edge is a node which is called its

root node. Let connection trees of DRS 1– ports $\mathcal{N}_{P_1}^1, \mathcal{N}_{P_2}^2$, be specified. If \mathcal{N}_P is a parallel connection of $\mathcal{N}_{P_1}^1, \mathcal{N}_{P_2}^2$, its connection tree is constructed by first defining a root node n_{12} for it and joining it to the root nodes n_1, n_2 of $\mathcal{N}_{P_1}^1, \mathcal{N}_{P_2}^2$, respectively by green edges. If \mathcal{N}_P is a series connection of $\mathcal{N}_{P_1}^1, \mathcal{N}_{P_2}^2$, its root node n_{12} is joined to the root nodes n_1, n_2 of $\mathcal{N}_{P_1}^1, \mathcal{N}_{P_2}^2$, respectively by red edges. Nodes of the connection tree which correspond to primitive 1– ports are called **leaf nodes**. Each node that is not a leaf node, is connected to exactly two nodes beneath it, which are called its children and atmost one node above it, called its parent, if it exists. The maximum length of a path from a node to a leaf node travelling from parent to child, is called its **level**. The level of the root node is called the **depth** of the connection tree.

Note that a series parallel DRS 1– port may have more than one connection tree.

Figure 4 (a) shows the port connection graph \mathcal{G}_P of a DRS multiport that is a series parallel connection of DRS 1– ports which are denoted by single edges and Figure 4 (c) shows its connection tree, representing green edges as bold lines and red edges as broken lines. We note that the algorithm of [17] (henceforth called **Algorithm (series-parallel)**) can build the connection tree of such port connection graphs in linear time.

6. Port characteristic of series parallel combination of piecewise linear 1– ports

We outline an application to DRS 1– ports which are models of solar cells through ideal diodes, resistors, voltage and current sources. In this case the procedure for computing the port characteristic is linear time on the sum of the number of states of the individual piecewise linear devices.

Even if the graph of our DRS 1– port is non series parallel, we may be able to regard it as a series parallel combination of 1– ports with piecewise linear characteristics. This we could do by pulling out non series parallel subgraphs, attached to the rest of the graph at a pair of nodes, as 1– ports (see Section 9.4). The algorithm of [10] performs this task of pulling out such non series parallel subgraphs in linear time on the number of edges and nodes in the graph. We compute the port characteristics of these 1– ports initially, before we use the procedures described in this section. Therefore our description is in terms of 1– ports with piecewise linear characteristics rather than in terms of DRS 1– ports.

We begin with an elementary but basic lemma. We remind the reader that ‘piecewise linear’ refers to ‘continuous piecewise linear with positive slope’.

Lemma 17. Let $\mathcal{N}_P^1, \mathcal{N}_P^2$, be 1– ports with piecewise linear $v - i$ characteristics, respectively $i = f_1(v), i = f_2(v)$. Let $\mathcal{N}_P^{parallel}, \mathcal{N}_P^{series}$, be the multiports obtained by aligned parallel connection of the 1– ports at P and aligned series connection of the 1– ports at P respectively. Let the corners of the characteristics of $\mathcal{N}_P^1, \mathcal{N}_P^2$, occur at $(v_1, i_1) \cdots, (v_k, i_k)$, and $(v'_1, i'_1) \cdots, (v'_m, i'_m)$ respectively. Then the $v - i$ characteristics of $\mathcal{N}_P^{parallel}, \mathcal{N}_P^{series}$, are also piecewise linear. The corners of $\mathcal{N}_P^{parallel}$ belong to the set of points $(v_1, f_1(v_1) + f_2(v_1)), \cdots, (v_k, f_1(v_k) + f_2(v_k)), (v'_1, f_1(v'_1) + f_2(v'_1)), \cdots, (v'_m, f_1(v'_m) + f_2(v'_m))$ and the corners of \mathcal{N}_P^{series} belong to the set of points $(f_1^{-1}(i_1) + f_2^{-1}(i_1), i_1), \cdots, (f_1^{-1}(i_k) + f_2^{-1}(i_k), i_k), (f_1^{-1}(i'_1) + f_2^{-1}(i'_1), i'_1), \cdots, (f_1^{-1}(i'_m) + f_2^{-1}(i'_m), i'_m)$.

Proof. The $v - i$ characteristic of $\mathcal{N}_P^{parallel}$ is obtained by adding the currents i_P^1, i_P^2 , into $\mathcal{N}_P^1, \mathcal{N}_P^2$, respectively for a given voltage v_P . It follows that the points $(v_1, f_1(v_1) + f_2(v_1)), \cdots, (v_k, f_1(v_k) + f_2(v_k)), (v'_1, f_1(v'_1) + f_2(v'_1)), \cdots, (v'_m, f_1(v'_m) + f_2(v'_m))$, lie in the $v - i$ characteristic of $\mathcal{N}_P^{parallel}$. Suppose $v - i$ characteristics of both $\mathcal{N}_P^1, \mathcal{N}_P^2$, are straight lines between v'_P, v''_P . Then it is clear that the $v - i$ characteristic of $\mathcal{N}_P^{parallel}$ would also be a straight line (whose slope would be the sum of the slopes of the characteristics of the individual multiports). If one orders $(v_1, i_1) \cdots, (v_k, i_k), (v'_1, i'_1) \cdots, (v'_m, i'_m)$ according to increasing values of voltage say $(\hat{v}_1, \hat{i}_1), \cdots, (\hat{v}_{k+m}, \hat{i}_{k+m})$, it follows that between $\hat{v}_j, \hat{v}_{j+1}, j = 1, \cdots, k+m-1$, the characteristic of $\mathcal{N}_P^{parallel}$ would be a straight line with positive slope. Therefore any corners that exist must belong to the set $(\hat{v}_1, \hat{i}_1), \cdots, (\hat{v}_{k+m}, \hat{i}_{k+m})$.

We note that when the slope is positive, $i = f(v)$ is an invertible function and the slope of $f^{-1}(\cdot)$ is positive. The proof of the series case is similar with the addition taking place along the $i -$ axis. \square

We have the following consequence of Lemma 17.

Lemma 18. *Let \mathcal{N}_P be a DRS 1– port built by series or parallel combination of DRS multiports $\mathcal{N}_P^1, \mathcal{N}_P^2$, where the $v - i$ characteristic of $\mathcal{N}_P^1, \mathcal{N}_P^2$, have k_1, k_2 corners respectively. Then \mathcal{N}_P has atmost $k_1 + k_2$ corners.*

The following result is a consequence of Lemma 18.

Theorem 19. *Let \mathcal{N}_P be a DRS 1– port that is obtained by series-parallel combination of DRS 1– ports $\mathcal{N}_{P_j}, j = 1, \dots, k$. We then have the following.*

1. *If the DRS 1– ports $\mathcal{N}_{P_j}, j = 1, \dots, k$, are primitive, then the $v - i$ characteristic of \mathcal{N}_P has atmost k corners.*
2. *Let each of the corners of the 1– ports $\mathcal{N}_{P_j}, j = 1, \dots, k$, lie within the the open box $-kx < v < kx, -kx < i < kx$. Then all the corners of the $v - i$ characteristic of \mathcal{N}_P lie within the box $-kx \leq v \leq kx, -kx \leq i \leq kx$.*

Proof. 1. This is immediate from Lemma 18.

2. This is clearly true for $k = 1$. Let it be true for $k < m$. Let \mathcal{N}_P be a series or parallel combination of $\mathcal{N}_{P_1}^1, \mathcal{N}_{P_2}^2$, with all the corners in their $v - i$ characteristics contained respectively within the open boxes $-px < v < px, -px < i < px$ and $-qx < v < qx, -qx < i < qx$. Without loss of generality, we may assume that the multiports are aligned. When $\mathcal{N}_{P_1}^1, \mathcal{N}_{P_2}^2$, are put in parallel to result in \mathcal{N}_P , the final $v - i$ characteristic is obtained by adding currents for a given voltage. It is clear that the corners of the $v - i$ characteristic of \mathcal{N}_P lie within $-k'x \leq v \leq k'x, -mx \leq i \leq mx$, where $k' = \max\{p, q\}$. Therefore the corners of the $v - i$ characteristic of \mathcal{N}_P lie within $-mx \leq v \leq mx, -mx \leq i \leq mx$. When $\mathcal{N}_{P_1}^1, \mathcal{N}_{P_2}^2$, are put in series to result in \mathcal{N}_P , the final $v - i$ characteristic is obtained by adding voltages for a given current. It is clear that the corners of the $v - i$ characteristic of \mathcal{N}_P lie within $-mx \leq v \leq mx, -k'x \leq i \leq k'x$, where $k' = \max\{p, q\}$. Therefore the corners of the $v - i$ characteristic of \mathcal{N}_P lie within $-mx \leq v \leq mx, -mx \leq i \leq mx$. \square

The following result generalizes the essential idea of Theorem 19.

Theorem 20. *Let $\mathcal{N}_P^1, \mathcal{N}_P^2$, be 1– ports with characteristics $i_P^1 = f^1(v_P^1), i_P^2 = f^2(v_P^2)$, where $f^1(\cdot), f^2(\cdot)$, are piecewise linear functions. Further, let $\mathcal{N}_P^1, \mathcal{N}_P^2$, have unique solutions for every port voltage (current). Then the series and parallel combinations of $\mathcal{N}_P^1, \mathcal{N}_P^2$, also inherit these properties.*

Proof. Since $f^1(\cdot), f^2(\cdot)$, are strictly monotonically increasing, they are invertible functions so that we have $v_P^1 = (f^1)^{-1}(i_P^1), v_P^2 = (f^2)^{-1}(i_P^2)$. We will only prove the result for the parallel case. The series case proof is by interchanging the roles of current and voltage. Let \mathcal{N}_P^3 be the parallel combination of $\mathcal{N}_P^1, \mathcal{N}_P^2$. Then its port characteristic is $i_P^3 = f^1(v_P^3) + f^2(v_P^3)$. For a given voltage v_P^3 the port voltages of $\mathcal{N}_P^1, \mathcal{N}_P^2$, are unique being equal to it and therefore voltages and currents for the non port edges of $\mathcal{N}_P^1, \mathcal{N}_P^2$, are uniquely fixed. The function $f^1(\cdot) + f^2(\cdot)$ is also strictly monotonically increasing and therefore invertible. For a given current i_P^3 , the voltage v_P^3 and therefore the port voltages of $\mathcal{N}_P^1, \mathcal{N}_P^2$, are uniquely fixed. As before, this fixes uniquely the voltages and currents for the non port edges of $\mathcal{N}_P^1, \mathcal{N}_P^2$. \square

Theorem 19 suggests a linear time algorithm for the computation of the $v - i$ characteristic of a DRS 1– port that is a series parallel connection of primitive DRS 1– ports whose $v - i$ characteristics are known. We need a couple of preliminary definitions for the convenient description of the connection of the primitive 1– ports.

Definition 21. *Let \mathcal{N}_P be a DRS 1– port with all its corners $(v^j, i^j), j = 1, \dots, k$, in the open box $-x < v < x, -x < i < x$, and let $(-x, f(-x)), (x, f(x))$ be points in the $v - i$ characteristic of \mathcal{N}_P . We will call $(-x, f(-x)), (x, f(x))$, the **extreme points** and, we will call the corners and the extreme points together, the **essential points** of \mathcal{N}_P .*

The $v - i$ characteristic of a DRS 1– port is determined by its essential points. We simply have to join the left extreme point (along the $v -$ axis) to the left most corner and extend it to $-\infty$, join each corner to the one to its right and the right most corner to the right extreme point and extend it to ∞ . If the

connection tree of a DRS 1– port \mathcal{N}_P and essential points of the primitive DRS 1– ports that are the leaf nodes of the connection tree are given, it is easy to compute the essential points of \mathcal{N}_P in linear time on the number of leaf nodes.

Algorithm I

Input: 1. The connection tree $t(\mathcal{G}_P)$ of the port connection graph \mathcal{G}_P of \mathcal{N}_P .

2. The essential points of the $v-i$ characteristic of the leaf nodes of the device characteristic.

Output: The essential points of the $v-i$ characteristic of \mathcal{N}_P at the port P .

Step 1. Compute the essential points of the $v-i$ characteristic of a node n at level $m+1$ as follows.

Let edges e_1, e_2 be between n_1, n and n_2, n , where n_1 is at level m and n_2 at level m or lower. Let the essential points of n_1 lie in the box $-x_1 \leq i_1 \leq +x_1, -x_1 \leq v_1 \leq +x_1$ and that of n_2 lie in the box $-x_2 \leq i_2 \leq +x_2, -x_2 \leq v_2 \leq +x_2$, with $x_1 \geq x_2$. Extend the $v-i$ characteristic of n_2 to $-x_1 \leq i_2 \leq +x_1$ by extending the leftmost and rightmost line segments.

Step 2(a). If e_1, e_2 are green, for each essential point (v', i') of n_1 ((v', i') of n_2), compute the point (v'', i'') of n_2 ((v'', i'') of n_1) and thence the essential point $(v', i' + i'')$ of n .

Step 2(b). If e_1, e_2 are red, for each essential point (v', i') of n_1 ((v', i') of n_2), compute the point (v'', i'') of n_2 ((v'', i'') of n_1) and thence the essential point $(v' + v'', i')$ of n .

STOP if n is the root node.

7. Computation of port characteristics by approximation of piecewise linear devices

Piecewise linear devices lend themselves to approximations by devices whose $v-i$ characteristics have fewer corners. Let $(v_l, i_l), (v_r, i_r)$, be the left most and right most corners respectively of piecewise linear device L^{orig} . We construct the $v-i$ characteristic of the device L^{approx} , as follows. We take as its left most and right most corners, points $(v'_l, i'_l), (v'_r, i'_r)$, respectively, which lie in L^{orig} and further are to the left and right of $(v_l, i_l), (v_r, i_r)$, respectively. We make the two curves agree with each other in the intervals $(-\infty, v'_l]$ and $[v'_r, +\infty)$ but modify the characteristic of L^{orig} within $[v'_l, v'_r]$ appropriately.

Definition 22. Let $\epsilon_v, \epsilon_i > 0$. We say a $v-i$ characteristic L^{approx} is an (ϵ_v, ϵ_i) approximation to a characteristic L^{orig} iff for each point (v', i') in L^{orig} , there exist points $(v'', i''), (v', i^3)$ in L^{approx} such that $|v'' - v'| \leq \epsilon_v$ and $|i^3 - i'| \leq \epsilon_i$.

Example 23. The following are examples of (ϵ_v, ϵ_i) approximations.

Take points $(v'_l, i'_l), (v'_r, i'_r)$ of L^{orig} which are to the left and right of the left most and right most corners respectively of L^{orig} , to be points in L^{approx} and let the latter agree with L^{orig} outside $[v'_l, v'_r]$.

1. Divide the interval (v'_l, v'_r) into subintervals of length ϵ_v and the interval (i'_l, i'_r) into subintervals of length ϵ_i . Sample L^{orig} at the endpoints of these subintervals along the v and i axes and take these to be the corners of L^{approx} . This is a suitable method where L^{approx} has to be computed when L^{orig} is not available explicitly (see Section 8.1).
2. Retain some of the corners of L^{orig} , including the left most and right most, as corners in L^{approx} and join successive retained corners by straight line segments. Let these successive corners never differ in width by more than ϵ_v and in height by more than ϵ_i . Outside the left most and right most corners, let L^{orig}, L^{approx} agree. This is a suitable method where L^{orig} is available explicitly.

We now examine how much the port characteristics change if every piecewise linear device were replaced by its approximation when the underlying graph is series parallel.

Theorem 24. Let $\mathcal{N}_P^{orig}, \mathcal{N}_P^{approx}$, be the 1– ports with the same series parallel graph \mathcal{G}_P but with the original piecewise linear devices $L_1^{orig}, \dots, L_n^{orig}$ and with their (ϵ_v, ϵ_i) approximations $L_1^{approx}, \dots, L_n^{approx}$, respectively. Let their $v - i$ characteristics at port P be L_P^{orig} and L_P^{approx} , respectively. Let $k + 1$ be the number of edges of \mathcal{G}_P (k be the leaf nodes of the connection tree of \mathcal{G}_P). Then L_P^{approx} is a $(k\epsilon_v, k\epsilon_i)$ – approximation of L_P^{orig} .

Proof. Let $\mathcal{N}_P^{1orig}, \mathcal{N}_P^{2orig}, \mathcal{N}_P^{1approx}, \mathcal{N}_P^{2approx}$ be 1– ports with port characteristics $L_P^{1orig}, L_P^{2orig}, L_P^{1approx}, L_P^{2approx}$ respectively. Further, let $L_P^{japprox}$ be an $(\epsilon_v^j, \epsilon_i^j)$ – approximation of L_P^{jorig} , for $j = 1, 2$. Let the two original 1– ports be combined in parallel (series) to result in \mathcal{N}_P^{3orig} , with port characteristic L_P^{3orig} , and the two approximation 1– ports be combined in parallel (series) to result in $\mathcal{N}_P^{3approx}$ with port characteristics $L_P^{3approx}$.

Using the fact that during parallel (series) combination, currents (voltages) get added, it can be shown that $L_P^{3approx}$ is a $((\epsilon_v^1 + \epsilon_v^2), (\epsilon_i^1 + \epsilon_i^2))$ – approximation of L_P^{3orig} . We will show this for the parallel case and for the case where points $(v^{1orig}, i^{1orig}) \in L_P^{1orig}, (v^{2orig}, i^{2orig}) \in L_P^{2orig}$, and points $(v^{1orig} - \epsilon_v^1, i^{1orig}), (v^{1orig}, i^{1orig} + \epsilon_i^1) \in L_P^{1approx}, (v^{2orig} - \epsilon_v^2, i^{2orig}), (v^{2orig}, i^{2orig} + \epsilon_i^2) \in L_P^{2approx}$. The other cases are similar. The point $(v^{1orig}, i^{1orig} + i^{2orig}) \in L_P^{3orig}$. The segments of $L_P^{1approx}, L_P^{2approx}$ between points $(v^{1orig} - \epsilon_v^1, i^{1orig}), (v^{1orig}, i^{1orig} + \epsilon_i^1)$, and points $(v^{2orig} - \epsilon_v^2, i^{2orig}), (v^{2orig}, i^{2orig} + \epsilon_i^2)$, respectively are continuous increasing curves (both in the v – and in the i – direction). When these segments are added along the i – direction, the resulting segment of $L_P^{3approx}$ contains points $(v^{1orig}, i^{1orig} + i^{2orig} + \epsilon_i^1 + \epsilon_i^2), (v^{1orig} + \epsilon_v^1 + \epsilon_v^2, i^{1orig} + i^{2orig})$. In general, it can be seen that $L_P^{3approx}$ contains points $(v^{1orig}, i^{1orig} + i^{2orig} \pm \epsilon)$, $(v^{1orig} \pm \epsilon', i^{1orig} + i^{2orig})$, where $0 \leq \epsilon' \leq \epsilon_v^1 + \epsilon_v^2$ and $0 \leq \epsilon \leq \epsilon_i^1 + \epsilon_i^2$.

If L_P^{1orig}, L_P^{2orig} are leaf nodes in the connection tree, then L_P^{3orig} is the parent node and by the above argument, $L_P^{3approx}$ is a $(2\epsilon_v, 2\epsilon_i)$ – approximation of L_P^{3orig} . The number of leaf nodes of L_P^{3orig} is 2 and the result is true in this case. If L_P^{1orig}, L_P^{2orig} are higher level nodes with k_1, k_2 leaf nodes respectively, let us assume that $L_P^{1approx}, L_P^{2approx}$ are their $(k_1\epsilon_v, k_1\epsilon_i)$ –, $(k_2\epsilon_v, k_2\epsilon_i)$ – approximations respectively. The parent node is L_P^{3orig} and it follows that $L_P^{3approx}$ is a $((k_1 + k_2)\epsilon_v, (k_1 + k_2)\epsilon_i)$ – approximation of L_P^{3orig} . Since the sets of leaf nodes of L_P^{1orig}, L_P^{2orig} do not intersect, $(k_1 + k_2)$ is the number of leaf nodes of L_P^{3orig} and the result is true in this case. By induction, the result is true when L_P^{3orig} is the root node. \square

8. Maximum power transfer for 1– ports with piecewise linear characteristics

The computation of maximum power transfer when the port characteristic is piecewise linear is easy if the number of corners is not very large. When the 1– port is a series parallel combination of primitive DRS 1– ports, we have seen that the characteristic can be computed in linear time on the number of primitive 1– ports (i.e., the number of diodes in the overall 1– port) and further the number corners does not exceed the number of diodes in the 1– port. The computation of maximum power transfer in this case is particularly easy and is outlined below.

Lemma 25. The line segment between the points $(v_1, i_1), (v_2, i_2)$, is equivalent to $v = E + ir$, $i_1 \leq i \leq i_2$, where $r = (v_2 - v_1)/(i_2 - i_1)$, and $E = [(i_2/(i_2 - i_1))v_1 - (i_1/(i_2 - i_1))]v_2$. The minimum of the product $v \times i$, at points in the line segment, occurs at $i = -E/2r$, if $i_1 \leq -E/2r \leq i_2$, otherwise it occurs at $i = i_1$ or $i = i_2$.

To compute the minimum power absorbed (negative of maximum power transfer) points we first compute the $v \times i$ product at all the corners between $(v_0, 0)$ and $(0, i_{k+1})$. Additionally if the minimum power, absorbed in a line segment between successive corners, occurs between its endpoints, compute that product and take the overall minimum of all these products. The corner points as well as the intermediate points at which this value is the $v \times i$ product, are the maximum power transfer points.

8.1. Approximate maximum power transfer for DRS 1– ports

The power absorbed $v_P \times i_P$ by a DRS 1– port will be negative (power delivered positive) only in the second and fourth quadrants of the $v_P - i_P$ plane. We have seen that the $v - i$ characteristic of a DRS 1– port is piecewise linear with all the straight line segments having positive slope (Corollary 13). It follows that for computing the maximum power transfer, we need only examine the portion of the characteristic lying between $(0, i^{sc})$ and $(v^{oc}, 0)$. Without loss of generality, we will take $v^{oc} \geq 0, i^{sc} \leq 0$. As mentioned before, solving a DRS 1– port for a given voltage source or current source termination is a quadratic programming problem which can be solved efficiently. A natural way of approximating the $v - i$ characteristic is to divide a box $\tilde{i}_1 \leq i \leq \tilde{i}_2, \tilde{v}_1 \leq v \leq \tilde{v}_2$, by a grid with $k_1 + 1$ vertical lines corresponding to voltages and $k_2 + 1$ horizontal lines corresponding to currents. We then compute the port current, port voltage corresponding to the vertical, horizontal lines respectively. Successive computed points along the characteristic will not be farther than $(\tilde{v}_2 - \tilde{v}_1)/k_1$ in the v coordinate and $(\tilde{i}_2 - \tilde{i}_1)/k_2$ in the i coordinate. This fact can be used to estimate the error between the actual maximum power transfer and the computed one, as in the next theorem.

Lemma 26. *Let \mathcal{N}_P be a DRS 1– port with $v^{oc} \geq 0, i^{sc} \leq 0$. Let $(\tilde{v}_1, \tilde{i}_1), (\tilde{v}_2, \tilde{i}_2)$ be points in the $v - i$ characteristic of \mathcal{N}_P at the port P such that $0 \leq \tilde{v}_1 < \tilde{v}_2 \leq v^{oc}, i^{sc} \leq \tilde{i}_1 < \tilde{i}_2 \leq 0$, $\tilde{v}^m := \tilde{v}_1 + (\tilde{v}_2 - \tilde{v}_1) \times (m/k_1), m = 0, \dots, k_1, \tilde{i}^n := \tilde{i}_1 + (\tilde{i}_2 - \tilde{i}_1) \times (n/k_2), n = 0, \dots, k_2$. Let \tilde{i}^m, \tilde{v}^n , be the port current and voltage when \tilde{v}^m, \tilde{i}^n , are the port voltage and current respectively. Let the points $(\tilde{v}^m, \tilde{i}^m), (\tilde{v}^n, \tilde{i}^n), m = 0, \dots, k_1, n = 0, \dots, k_2$, be reordered as $(v^j, i^j), j = 0, \dots, k_1 + k_2 - 1$ such that $(v^j, i^j), (v^{j+1}, i^{j+1}), j = 0, \dots, k_1 + k_2 - 2$ are successive points along the $v - i$ characteristic.*

1. *Let (v', i') be the point in the $v - i$ characteristic of \mathcal{N}_P between the points $(v^j, i^j), (v^{j+1}, i^{j+1})$. Then $\max\{|v' \times i' - v^j \times i^j|, |v' \times i' - v^{j+1} \times i^{j+1}|\} \leq |(v^{j+1} - v^j) \times i^j| + |(i^{j+1} - i^j) \times v^j| < |(\tilde{v}_2 - \tilde{v}_1) \times \tilde{i}_1/k_1 + |(\tilde{i}_2 - \tilde{i}_1) \times \tilde{v}_2/k_2|$.*
2. *Let the minimum value of $v_P \times i_P$ along the characteristic between the points $(\tilde{v}_1, \tilde{i}_1), (\tilde{v}_2, \tilde{i}_2)$ be reached at (v'', i'') with $\tilde{v}_1 \leq v'' \leq \tilde{v}_2, \tilde{i}_1 \leq i'' \leq \tilde{i}_2$. Then $|v'' \times i'' - \min_{0 \leq j \leq k_1 + k_2 - 1} \{v^j \times i^j\}| < |(\tilde{v}_2 - \tilde{v}_1) \times \tilde{i}_1/k_1 + |(\tilde{i}_2 - \tilde{i}_1) \times \tilde{v}_2/k_2|$.*

Proof. 1. Because the slope of the $v - i$ curve is always positive, we must have $|i^j| > |i^{j+1}|$ and therefore the rectangle corresponding to $v_P \times i_P$ at points in the characteristic between $(v^j, i^j), (v^{j+1}, i^{j+1})$ is contained in the rectangle corresponding to $v^{j+1} \times i^j$ and contains the rectangle corresponding to $v^j \times i^{j+1}$. It follows that the power absorbed at points in the characteristic between $(v^j, i^j), (v^{j+1}, i^{j+1})$ lies between $v^j \times i^{j+1}$ and $v^{j+1} \times i^j$. Therefore, $\max\{|v' \times i' - v^j \times i^j|, |v' \times i' - v^{j+1} \times i^{j+1}|\} \leq |v^j \times i^{j+1} - v^{j+1} \times i^j| = |v^j \times i^{j+1} - v^j \times i^j + v^j \times i^j - v^{j+1} \times i^j| = |(i^{j+1} - i^j) \times v^j + (v^j - v^{j+1}) \times i^j| = |(v^j - v^{j+1}) \times i^j| + |(i^{j+1} - i^j) \times v^j|$ (since $(i^{j+1} - i^j) \times v^j$ and $(v^j - v^{j+1}) \times i^j$ have the same sign) $< |(\tilde{v}_2 - \tilde{v}_1) \times \tilde{i}_1/k_1 + |(\tilde{i}_2 - \tilde{i}_1) \times \tilde{v}_2/k_2|$.

2. Let (v'', i'') lie in the characteristic between the points $(v^j, i^j), (v^{j+1}, i^{j+1}), 0 \leq j \leq k_1 + k_2 - 2$. Then $|v'' \times i'' - \min_{0 \leq m \leq k_1 + k_2 - 1} \{v^m \times i^m\}| \leq \min\{|v'' \times i'' - v^j \times i^j|, |v'' \times i'' - v^{j+1} \times i^{j+1}|\}$. By part 1 above, $\max\{|v' \times i' - v^j \times i^j|, |v' \times i' - v^{j+1} \times i^{j+1}|\} < |(\tilde{v}_2 - \tilde{v}_1) \times \tilde{i}_1/k_1 + |(\tilde{i}_2 - \tilde{i}_1) \times \tilde{v}_2/k_2|$. Thus $|v'' \times i'' - \min_{0 \leq m \leq k_1 + k_2 - 1} \{v^m \times i^m\}| < |(\tilde{v}_2 - \tilde{v}_1) \times \tilde{i}_1/k_1 + |(\tilde{i}_2 - \tilde{i}_1) \times \tilde{v}_2/k_2|$. \square

9. Validity region and maximum power transfer for a given diode state

9.1. General DRS multiport case

The maximum power transfer problem for \mathcal{N}_P at ports P for a valid diode state (D_1, D_2) is as follows:

$$\text{minimize } v_P^T i_P \text{ for } \mathcal{N}_P, \text{ where } v_{D_1} = 0, i_{D_1} \geq 0, i_{D_2} = 0, v_{D_2} \leq 0. \quad (3)$$

Consider the hybrid port representation for \mathcal{N}_{DP} in Equation 1. Under the valid state (D_1, D_2) , this equation reduces to

$$\begin{pmatrix} g_{D_1 D_1} & h_{D_1 D_2} & h_{D_1 P} \\ h_{D_2 D_1} & r_{D_2 D_2} & r_{D_2 P} \\ h_{P D_1} & r_{P D_2} & r_{PP} \end{pmatrix} \begin{pmatrix} 0_{D_1} \\ 0_{D_2} \\ i_P \end{pmatrix} + \begin{pmatrix} J_{D_1} \\ E_{D_2} \\ E_P \end{pmatrix} = \begin{pmatrix} i_{D_1} \geq 0 \\ v_{D_2} \leq 0 \\ v_P \end{pmatrix}, \quad (4)$$

which is equivalent to

$$h_{D_1 P} i_P + J_{D_1} \geq 0 \quad (5)$$

$$r_{D_2 P} i_P + E_{D_2} \leq 0 \quad (6)$$

$$r_{PP} i_P + E_P = v_P, \quad (7)$$

Therefore, the maximum power transfer problem reduces to

$$\text{minimize } E_P^T i_P + i_P^T r_{PP} i_P \text{ under} \quad (8)$$

$$h_{D_1 P} i_P + J_{D_1} \geq 0 \quad (9)$$

$$-r_{D_2 P} i_P - E_{D_2} \geq 0. \quad (10)$$

Since the matrix r_{PP} is a symmetric positive definite matrix, this is a convex quadratic programming problem which has a unique optimum value. There are polynomial time algorithms available now for solving convex programming problems [18],[15] (see Appendix A).

If we choose to use port voltages as inputs, we have to work with a hybrid matrix in place of the one in Equation 4, where in place of the variable v_P on the right, we have i_P and in place of i_P, E_P on the left, we have v_P, J_P respectively.

9.2. DRS 1– port case

The important special case where \mathcal{N}_P is a 1– port has a much simpler solution. Here, the inequalities of Equation 8 are in terms of a single scalar variable i_P of the form $a_j i_P \geq b_j$, or $a_q i_P \leq b_q$, taking a_j, a_q to be non negative. The inequalities where the coefficient is zero are feasibility conditions of the form $0 \geq b_j$ or $0 \leq b_q$. If (D_1, D_2) is a valid diode state, these feasibility conditions would be satisfied.

The remaining inequalities are of the form of the form $a_j i_P \geq b_j$, or $a_q i_P \leq b_q$, taking a_j, a_q to be positive. For the former inequalities, we must have $i_P \geq \max_j \{\frac{b_j}{a_j}\}$. Let $i_P^1 \equiv \max_j \{\frac{b_j}{a_j}\}$. For the latter inequalities, we must have $i_P \leq \min_q \{\frac{b_q}{a_q}\}$. Let $i_P^2 \equiv \min_q \{\frac{b_q}{a_q}\}$. If (D_1, D_2) is a valid diode state, these would not be inconsistent and it would follow that $i_P^1 \leq i_P^2$ and the interval over which (D_1, D_2) is valid would be $[i_P^1, i_P^2]$.

For computation of maximum power transfer for the given diode state, we need to consider two situations.

Case 1. All the inequalities are satisfied strictly, i.e., $i_P > \max_j \{\frac{b_j}{a_j}\}, i_P < \min_q \{\frac{b_q}{a_q}\}$, but $E_P i_P + i_P r_{PP} i_P$ reaches a minimum.

This corresponds to the usual maximum power transfer for the linear case, viz. $v_P = -r_{PP} i_P$ so that $E_P = -2(r_{PP})i_P$.

Case 2. Atleast one of the inequalities is satisfied as an equality, i.e., $i_P = \max_j \{\frac{b_j}{a_j}\}$ or $i_P = \min_q \{\frac{b_q}{a_q}\}$.

Since \mathcal{N}_P is a DRS multiport, it has a unique solution corresponding to the value of i_P for either of the above cases. The following algorithm summarizes the above discussion.

Algorithm II

Input: A DRS 1– port \mathcal{N}_P and a state (D_1, D_2) for \mathcal{N}_P .

Output: a) The interval of i_P within which (D_1, D_2) is valid.

b) The port current i_P for which the power output $-v_P i_P$ is maximum for \mathcal{N}_P .

Step 1. Construct the inequalities of Equation 8.

These are of the form $a_j i_P \geq b_j$, or $a_q i_P \leq b_q$, taking a_j, a_q to be non negative.

The inequalities where the coefficient is zero are feasibility conditions of the form $0 \geq b_j$ or $0 \leq b_q$.

If these are incorrect declare (D_1, D_2) to be invalid.

The inequalities where the coefficient of i_P is not zero are equivalent to $i_P \geq \max_j \{\frac{b_j}{a_j}\}, i_P \leq \min_q \{\frac{b_q}{a_q}\}$, a_j, a_q , positive. Let $i_P^1 = \max_j \{\frac{b_j}{a_j}\}$, $i_P^2 = \min_q \{\frac{b_q}{a_q}\}$.

If $i_P^1 > i_P^2$, declare (D_1, D_2) to be invalid.

Otherwise declare (D_1, D_2) to be valid in the interval $i_P^1 \leq i_P \leq i_P^2$.

Step 2. Compute $i_P^3 = \frac{-E_P}{2r_{PP}}$. If $i_P^1 \leq i_P^3 \leq i_P^2$, output i_P^3 .

If not output i_P^1 or i_P^2 for which $-v_P i_P$ is maximum.

STOP.

9.3. Methods for computing port characteristic

We have seen that the number of straight line segments in the port characteristic of a DRS 1– port is the number of valid diode states (Corollary 13). It is possible to construct circuits for which the number of valid states is exponential in the number of diodes. Therefore, explicitly computing the port characteristic of a DRS 1– port in some specified interval $v_1 \leq v_2$ ($i_1 \leq i_2$) is in general of exponential complexity in the number of diodes. There are situations where the number of valid diode states of the DRS 1– port is a polynomial in k . (The extreme situation of this kind was described in Subsection 6 where the number of diode states did not exceed the number of diodes. However, we saw that a much faster algorithm was available for computing the port characteristic, in that case.) Suppose the diode state at (v_1, i_1) is known or has been computed solving a quadratic programming problem. We could increase the port voltage (current) until one of the inequalities becomes an equality, as in Step 1 of Algorithm II (i.e., setting $i_P = \min_q \{\frac{b_q}{a_q}\}$).

We could then change the diode state correspondingly (i.e., if the equality holds at $\frac{b_r}{a_r}$, the diode at that position changes state) and recompute the diode voltage and current inequalities in Equation 8. This needs the evaluation of r_{PP} and E_P in the Equation $r_{PP} i_P + E_P = v_P$ (see below Equation 5), which can be obtained by computing two solutions of the resistive network obtained by shorting or opening the appropriate diode ports - one setting all internal sources to zero and setting $v_P = 1$, and second, keeping internal sources active but $v_P = 0$. The process is repeated until (v_2, i_2) is reached.

Similarly, starting at (v_2, i_2) we could have reached (v_1, i_1) by decreasing the port voltage (current).

Suppose \hat{k} is the number of states between $(v_1, i_1), (v_2, i_2), v_1 \leq v_2$. To exactly compute the piecewise linear $v - i$ characteristic of \mathcal{N}_P , between $(v_1, i_1), (v_2, i_2)$, we need to solve purely resistive networks, with the same number of resistors as in \mathcal{N}_P , $2\hat{k}$ times, in addition to solving the DRS 1– port \mathcal{N}_P with port voltage (current) equal to v_1 (i_1).

An alternative method is suitable for non series parallel networks which are small (say edge set of size about 10 or less). We could pick diode states at random and compute their interval of validity in terms of say i_P using Algorithm II, until we encounter a valid diode state. The corresponding values of v_P can be calculated through the equality in the third row of Equation 4. We can take this as our initial state, increase and decrease i_P and use the same algorithm to compute the interval of validity of every valid diode state (D_1, D_2) , and the corresponding values of v_P . This would automatically compute the $v_P - i_P$ port characteristic for $-\infty < v_P < \infty, -\infty < i_P < \infty$. In this case, if \hat{k} is the number of valid states, we need to use Algorithm II, for say m randomly picked states and then, for the \hat{k} valid states. Each such calculation involves solution of two purely resistive networks, with the same number of resistors as in \mathcal{N}_P . The expected value of m can be seen to be $2\hat{k}/\hat{k}$. An advantage here is that we do not need to solve \mathcal{N}_P with some fixed input, which, as mentioned before, is a quadratic programming problem.

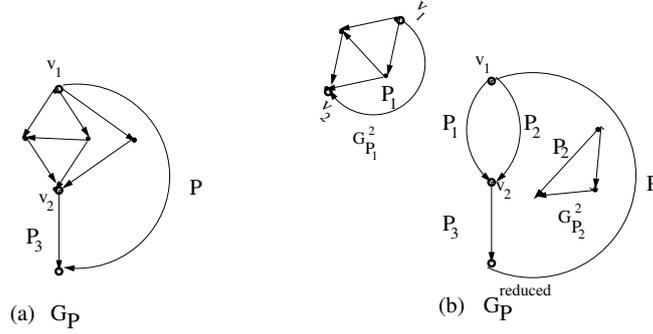


Figure 5: Simplification of \mathcal{G}_P to $\mathcal{G}_P^{\text{reduced}}$

9.4. Simplification of the DRS 1– port

In order to make best use of the methods outlined above, we present a preprocessing scheme in the following informal algorithm. This reduces the port connection graph \mathcal{G}_P of a DRS 1– port \mathcal{N}_P to that of a piecewise linear 1– port \mathcal{N}_P^L , that has the same port characteristic at P as \mathcal{N}_P . Computation of the port characteristic of \mathcal{N}_P^L when it is series parallel is discussed in Section 6. For the general case, approximate computation of port characteristic for estimating the maximum power transfer is discussed in Section 8.1.

Definition 27. A graph with more than 3 nodes is said to be 3– connected if it does not get disconnected by removal of any two nodes. A 3– connected subcomponent is a subgraph which has two nodes in common with the subgraph on the remaining edges, and which becomes 3– connected with the addition of an edge between the common nodes. A series subcomponent is a subgraph which has two nodes in common with the subgraph on the remaining edges and which is a series combination of edges. A parallel subcomponent is a subgraph which has two nodes in common with the subgraph on the remaining edges and which is a parallel combination of edges. **Algorithm (3–connected)** outputs 3– connected, series and parallel subcomponents of a graph [10]. It is linear time on the number of edges and nodes in the graph.

Algorithm III

Input: A port connection graph \mathcal{G}_P of a DRS 1– port \mathcal{N}_P in terms of primitive multiports with $v-i$ characteristic of each edge given.

Output: (a) A graph $\mathcal{G}_P^{\text{reduced}}$ that is either 3– connected or series parallel, with $v-i$ characteristic for each edge other than P .

(b) The port characteristic of \mathcal{N}_P .

Step 1. Check if \mathcal{G}_P is series parallel, using Algorithm (series-parallel) [17].

If it is, output the port characteristic of \mathcal{N}_P , using Algorithm I, output \mathcal{G}_P as $\mathcal{G}_P^{\text{reduced}}$ and STOP.

Step 2. If \mathcal{G}_P is not series parallel, decompose it into 3– connected subcomponents and series parallel subcomponents using Algorithm (3–connected). If \mathcal{G}_P is 3– connected, output \mathcal{G}_P as $\mathcal{G}_P^{\text{reduced}}$, compute the port characteristic of \mathcal{N}_P , directly (no simplification possible here) and STOP.

Step 3. Let G_1 be one of the 3– connected subcomponents. Let v_1, v_2 denote its terminals. Split this component from \mathcal{G}_P at the terminals v_1, v_2 . Add a directed edge P_1 from v_1 to v_2 in the two split subgraphs. Denote the subgraph containing the edge P by G_P^1 and the other by $G_{P_1}^2$. Compute the port characteristic of $G_{P_1}^2$ at P_1 and treat this as the $v-i$ characteristic of the piecewise linear device P_1 in G_P^1 . Computation of port characteristic $G_{P_1}^2$ at P_1 proceeds replacing P by P_1 and \mathcal{G}_P by $G_{P_1}^2$ and going back to

Step 1 (see Figure 5).
STOP.

Remark 4. *The method suggested in Algorithm III is effective only if explicit computation of port characteristic is performed for series parallel subgraphs or for 3– connected subgraphs with a small number of diodes (say ≤ 10). If the final reduced multiport $\mathcal{N}_P^{\text{reduced}}$ with piecewise linear devices is a series parallel graph, even an approximate computation of the characteristics of the devices in it, can be used to compute an approximation of the port characteristic of \mathcal{N}_P (Section 7). If $\mathcal{N}_P^{\text{reduced}}$ has a 3– connected graph, to compute the maximum power transfer, only the approximate method of Section 8.1, can be used since the number of states would be too large. (For instance if the graph has 10 edges and each piecewise linear device has 4 states, the number of states could be of the order of 2^{20} .) We saw, in Theorem 8, a method of reducing solution of multiports with piecewise linear devices to that of repeated solution of multiports with the same number of diodes. In the next section we present an alternative method using gradient descent.*

10. Analysis of circuits with piecewise linear devices through optimization methods

Optimization methods provide a useful option for the analysis of electrical circuits. Unlike the technique described in Section 4, these methods do not depend upon the number of corners in the $v - i$ characteristics of the devices. The following gradient descent algorithm is essentially the one available in [16], page 142. In the next subsection we will adapt this algorithm to the solution of networks with piecewise linear devices.

Algorithm IV

Let the search region Q be closed and convex with diameter R . Let $\phi(\cdot)$ be the convex function to be minimized over Q . Let $\phi(\cdot)$ satisfy the Lipschitz condition $|\phi(x) - \phi(y)|_2 \leq M|x - y|_2$.

To compute \hat{x} such that $\phi(\hat{x}) - \min_{x \in Q} \phi(x) \leq \epsilon > 0$, proceed as follows.

Choose $x_0 \in Q, N = \frac{M^2 R^2}{\epsilon^2}, h = \frac{\epsilon}{M}$.

(k^{th} iteration) Compute $\phi(x_k), \nabla \phi(x_k)$ and set $x_{k+1} = \text{projection of } (x_k - h \frac{\nabla \phi(x_k)}{|\nabla \phi(x_k)|_2}) \text{ onto } Q$.
 $\hat{x} = x_N$.

10.1. Circuit analysis through minimization of functions

Consider the problem

$$\text{Minimize } \phi(i) \tag{11}$$

$$Ai = J, \tag{12}$$

Where $\phi(\cdot)$ is continuously differentiable, and A is the reduced incidence matrix of a graph. Let $x^T := (x_1, \dots, x_n), \nabla \phi(i)^T := (\partial \phi(i) / \partial i_1, \dots, \partial \phi(i) / \partial i_n)$. The condition for local optimum is

$$\nabla \phi(i)^T = \lambda^T A.$$

We refer to the constraints

$$Ai - J = 0, \quad v = A^T \lambda, \quad v = \nabla \phi(i), \tag{13}$$

as the Lagrangian form of Equation 11. It is clear that these are the constraints of an electrical network \mathcal{N} on a graph \mathcal{G} whose reduced incidence matrix is $(A| - I)$ with cutset free current sources J and a single

‘multiport’ device with characteristic $v = \nabla\phi(i)$. Thus \hat{i} is a local optimum for Equation 11, iff \hat{i} is the current vector part of a solution of \mathcal{N} . For every static network defined as

$$Ai - J = 0, \quad v = A^T\lambda, \quad v = f(i), \quad (14)$$

we can create an optimization problem as in Equation 11 taking $f(i) \equiv \nabla\phi(i)$. If in addition the function $\phi(i)$ is convex, it can be shown that the local optimum is also a global optimum.

In the case of piecewise linear devices, $f(i)^T \equiv (f_1(i_1), \dots, f_n(i_n))$, where $f_j(i_j)$ is described by a (continuous positive slope) piecewise linear characteristic. The function $\phi(i)$ can be taken to be $\Sigma \int f_j(i_j) di_j$, where the integration is performed over some convenient interval for i_j which includes the current point i' of interest. In our procedure, it is not necessary to compute this integral explicitly, since only $\nabla\phi(i)$ plays a role. This function would be convex because the $v - i$ characteristic of the piecewise linear devices have positive slope, i.e., each of the functions $f_j(i_j)$ in $(f_1(i'_1), \dots, f_n(i'_n)) = \nabla\phi(i'_1, \dots, i'_n)$, is an increasing function. Since the network \mathcal{N} has no current source cutsets and the other devices are piecewise linear, by Theorem 4, it has a unique solution. Thus in this case there is a unique value of i at which the local optimum occurs.

A first order gradient descent algorithm that is an adaptation of Algorithm IV for the solution of Equation 11 is given below. We will suppose that for any given i_j of the piecewise linear device L_j , the voltage v_j is available through an oracle. This means $\nabla\phi(i'_1, \dots, i'_n) = (v'_1, \dots, v'_n)$ is available given any (i'_1, \dots, i'_n) . Let R denote the diameter of the search region, i.e., $|i - i^0|_2 \equiv \sqrt{\Sigma_j (i_j - i_j^0)^2} \leq R, Ai = Ai^0 = J$. Let $M \equiv \max\{|(v_1, \dots, v_n)|_2\}$, when (i_1, \dots, i_n) is in the search region. (This is the Lipschitz constant for $\phi(i)$, i.e., $|\phi(i') - \phi(i)|_2 \leq M|i' - i|_2$.)

Algorithm V

Gradient Descent of $\phi(i)$ under constraint $Ai = J$

Input: Initial current i^0 such that $Ai^0 = J$, diameter R , Lipschitz constant M for $\phi(i)$, Oracle for $\nabla\phi(i)$, A, J , error ϵ , number of steps $N = \frac{M^2 R^2}{\epsilon^2}$, step size $\eta \equiv \frac{\epsilon}{M}$.

Output: \hat{i} such that $A(\hat{i}) = J, \phi(\hat{i}) - \min_{Ai=J}\{\phi(i)\} \leq \epsilon$.

Repeat for $k = 0$ to $N - 1$
 Let $\theta(i^k)$ be the projection of $\nabla\phi(i^k)$ onto the space $Ai = 0$.

$$i^{k+1} = i^k - \eta \frac{\theta(i^k)}{|\theta(i^k)|_2}.$$

 end repeat

$$\hat{i} \equiv i^N.$$

Apart from the call to the oracle, the main computation in each step is that of evaluating $\theta(i^k)$ from $\nabla\phi(i^k)$. To project a vector \mathcal{E} , where $\mathcal{E}^T \equiv (\mathcal{E}_1, \dots, \mathcal{E}_n)$ on to the space $Ai = 0$, we need to solve the problem

$$\text{Find } i^T = (i_1, \dots, i_n) \text{ such that} \quad (15)$$

$$i^T - v^T = (\mathcal{E}_1, \dots, \mathcal{E}_n), Ai = 0, v = A^T\lambda. \quad (16)$$

This is the same as solving the resistive network problem with constraints $Ai = 0, v = A^T\lambda, i = I(v + \mathcal{E})$. This yields $\lambda = -(AA^T)^{-1}A\mathcal{E}$ and $i = A^T\lambda + \mathcal{E}$. Throughout the iterations, the matrix AA^T which has to be LU factored does not change so that only one such triangular factorization is required.

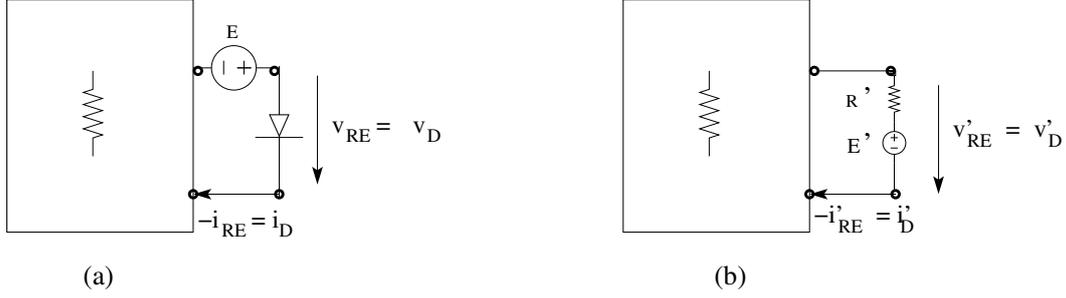


Figure 6: (a) $\mathcal{N}^{reduced}$ (b) Incremental network

11. Quadratic programming formulation for DRS networks

We sketch below the equivalence of the solution of a DRS network to that of an appropriately constructed quadratic programming problem. In the main we follow the treatment in [5]. We later adapt the interior point algorithm as described in [15] for the solution of DRS networks.

Let \mathcal{N} be a DRS network on graph \mathcal{G} with edge set $E_{\mathcal{D}} \cup E_{\mathcal{R}} \cup E_{\mathcal{E}} \cup E_{\mathcal{J}}$ corresponding to ideal diodes, positive resistors, voltage sources and current sources. Let \mathcal{N}_P be the multiport that is the diode elimination multiport of \mathcal{N} , i.e., the diodes are pulled out and across the resulting terminals we have ports. Since the diodes do not contain loops or cutsets of \mathcal{G} , the multiport \mathcal{N}_P has every possible hybrid representation and, in particular, the Thevenin equivalent $v_P = Ri_P + \mathcal{E}$. The solution of \mathcal{N} is equivalent, as far as the diode currents and voltages are concerned, to that of a reduced network $\mathcal{N}^{reduced}$ on $\mathcal{G}^{reduced}$ with edge set $P \cup E_{\mathcal{D}} \cup E_{\hat{\mathcal{E}}}$, with the series combination of a voltage and diode across each each port, as in Figure 6 (a).

The equations of $\mathcal{N}^{reduced}$ have the form

$$(I|I) \begin{pmatrix} i_{\hat{\mathcal{R}}\hat{\mathcal{E}}} \\ i_{\mathcal{D}} \end{pmatrix} = 0; v_{\hat{\mathcal{R}}\hat{\mathcal{E}}} = v_{\mathcal{D}}; v_{\hat{\mathcal{R}}\hat{\mathcal{E}}} = \hat{R}i_{\hat{\mathcal{R}}\hat{\mathcal{E}}} + \hat{\mathcal{E}} \quad (17)$$

$$-v_{\mathcal{D}} \geq 0, i_{\mathcal{D}} \geq 0, v_{\mathcal{D}}^T i_{\mathcal{D}} = 0, \quad (18)$$

where \hat{R} is symmetric positive definite. Equation 17 is the Lagrangian form of the Quadratic programming problem

$$\text{Minimize } \frac{1}{2} i_{\hat{\mathcal{R}}\hat{\mathcal{E}}}^T \hat{R} i_{\hat{\mathcal{R}}\hat{\mathcal{E}}} + \hat{\mathcal{E}}^T i_{\hat{\mathcal{R}}\hat{\mathcal{E}}} \quad (19)$$

$$i_{\hat{\mathcal{R}}\hat{\mathcal{E}}} \leq 0. \quad (20)$$

This is a convex programming problem (see Appendix A), where one has to minimize a strictly convex function over a convex region. When the objective function is bounded from below (as shown later), such a problem has a global optimum solution, which can be computed through polynomial time algorithms which are available since the early 90s ([18], [15]). The self concordant barrier method of [15] can be easily adapted for analysis of DRS networks as we show below.

Next consider the problem

$$\text{Maximize } -\frac{1}{2} (v_{\hat{\mathcal{R}}\hat{\mathcal{E}}}^T - \hat{\mathcal{E}}^T) (\hat{R})^{-1} (v_{\hat{\mathcal{R}}\hat{\mathcal{E}}} - \hat{\mathcal{E}}) \quad (21)$$

$$v_{\hat{\mathcal{R}}\hat{\mathcal{E}}} = -(\lambda) \quad (22)$$

$$\lambda \geq 0. \quad (23)$$

equivalently

$$\text{Maximize } -\frac{1}{2}(\lambda^T + \hat{\mathcal{E}}^T)(\hat{R})^{-1}(\lambda + \hat{\mathcal{E}}) \quad (24)$$

$$\lambda \geq 0. \quad (25)$$

It can be verified that this has the Lagrangian form

$$(I|I) \begin{pmatrix} (\hat{R})^{-1}(-\lambda - \hat{\mathcal{E}}) \\ \mu \end{pmatrix} = 0, \quad (26)$$

$$\lambda \geq 0, \mu \geq 0, \lambda^T \mu = 0, \quad (27)$$

If we set $v_{\hat{R}\hat{\mathcal{E}}} := -\lambda, i_{\hat{R}\hat{\mathcal{E}}} := (\hat{R})^{-1}(v_{\hat{R}\hat{\mathcal{E}}} - \hat{\mathcal{E}})$, we get the following equivalent form

$$(I|I) \begin{pmatrix} i_{\hat{R}\hat{\mathcal{E}}} \\ \mu \end{pmatrix} = 0; v_{\hat{R}\hat{\mathcal{E}}} = -\lambda; i_{\hat{R}\hat{\mathcal{E}}} = (\hat{R})^{-1}(v_{\hat{R}\hat{\mathcal{E}}} - \hat{\mathcal{E}}) \quad (28)$$

$$\lambda \geq 0, \mu \geq 0, \lambda^T \mu = 0, \quad (29)$$

Note that this is identical to Equation 17, if we set $\mu := i_D, \lambda := -v_D$.

We will next show that when both Equations 19 and 24 have feasible solutions, the value of the objective function of the former is always greater than or equal to that of the latter.

We have,

$$\frac{1}{2}(\hat{i}_{\hat{R}\hat{\mathcal{E}}}^T)(\hat{R})(i_{\hat{R}\hat{\mathcal{E}}}) + \hat{\mathcal{E}}^T i_{\hat{R}\hat{\mathcal{E}}} - (-\frac{1}{2}(v_{\hat{R}\hat{\mathcal{E}}}^T - \hat{\mathcal{E}})^T(\hat{R})^{-1}(v_{\hat{R}\hat{\mathcal{E}}} - \hat{\mathcal{E}})) \quad (30)$$

$$= \frac{1}{2}(i_{\hat{R}\hat{\mathcal{E}}}^T \hat{R} - v_{\hat{R}\hat{\mathcal{E}}}^T + \hat{\mathcal{E}}^T)(\hat{R})^{-1}(\hat{R}i_{\hat{R}\hat{\mathcal{E}}} - v_{\hat{R}\hat{\mathcal{E}}} + \hat{\mathcal{E}}) - i_{\hat{R}\hat{\mathcal{E}}}^T \lambda \geq 0, \quad (31)$$

where we have used the facts that \hat{R} is symmetric positive definite, $i_{\hat{R}\hat{\mathcal{E}}} \leq 0$ and $v_{\hat{R}\hat{\mathcal{E}}} = -\lambda, \lambda \geq 0$.

Examining the Lagrangian form, we see that $v_{\hat{R}\hat{\mathcal{E}}}^T i_{\hat{R}\hat{\mathcal{E}}} + v_D^T i_D = 0, v_D^T i_D = 0, v_{\hat{R}\hat{\mathcal{E}}} = \hat{R}i_{\hat{R}\hat{\mathcal{E}}} + \hat{\mathcal{E}}$, for optimality of either of Equations 19 or 21. It follows that under optimum conditions, the term on the LHS in Equation 30 goes to zero and therefore the optimum values of the Equations 19 or 21 have to be equal.

Electrically, this means that $\frac{1}{2}i_{\hat{R}\hat{\mathcal{E}}}^T \hat{R}i_{\hat{R}\hat{\mathcal{E}}} + \hat{\mathcal{E}}^T i_{\hat{R}\hat{\mathcal{E}}} = -\frac{1}{2}(v_{\hat{R}\hat{\mathcal{E}}}^T - \hat{\mathcal{E}}^T)(\hat{R})^{-1}(v_{\hat{R}\hat{\mathcal{E}}} - \hat{\mathcal{E}})$, i.e., that $\hat{\mathcal{E}}^T i_{\hat{R}\hat{\mathcal{E}}} + i_{\hat{R}\hat{\mathcal{E}}}^T \hat{R}i_{\hat{R}\hat{\mathcal{E}}} = 0$. i.e., that the net power absorbed by the resistors and the voltage sources is zero.

12. Interior point methods for DRS networks

We adapt the log-barrier method as described in [15], to the solution of DRS networks. The quadratic programming problem of Equation 19 is solved by instead solving, repeatedly changing the parameter μ , the barrier subproblem

$$\text{minimize } \frac{1}{2}i_{\hat{R}\hat{\mathcal{E}}}^T \hat{R}i_{\hat{R}\hat{\mathcal{E}}} + \hat{\mathcal{E}}^T i_{\hat{R}\hat{\mathcal{E}}} - \mu \sum \ln \rho_j, \mu > 0, \quad (32)$$

$$i_{\hat{R}\hat{\mathcal{E}}} + \rho = 0, \quad (33)$$

and maintaining the condition $\rho > 0$. The Lagrangian form for this problem is

$$i_{\hat{R}\hat{\mathcal{E}}} + \rho = 0, \rho > 0, y = \hat{R}i_{\hat{R}\hat{\mathcal{E}}}, y + \hat{\mathcal{E}} + \lambda = 0, \rho_j \lambda_j = \mu \forall j, \mu > 0. \quad (34)$$

If we set $v_{\hat{R}\hat{\mathcal{E}}} := y + \hat{\mathcal{E}}, v_D = -\lambda$, this expression reduces to the equations of the network which is obtained by replacing the diode of Figure 6 (a), by a device with characteristic $v_D i_D = -\mu$. Interior point methods start with some solution which satisfies the above equations and move to another which satisfies it with a lower value $\sigma\mu, 0 < \sigma < 1$, in place of μ . In practice ([4]), we can take $\rho_j \lambda_j = \mu_j \forall j, \mu_j > 0$, and the μ_j can all be different. Also each μ_j can be replaced at the next step with $\sigma_j \mu_j, 0 < \sigma_j < 1$, and the σ_j also can all be different. Equation 34 yields the following constraints on the incremental variables.

$$\Delta i_{\hat{R}\hat{\mathcal{E}}} + \Delta \rho = 0, \rho + \Delta \rho > 0, \Delta y = \hat{R} \Delta i_{\hat{R}\hat{\mathcal{E}}}, \Delta y + \Delta \lambda = 0, \Delta \rho_j \lambda_j + \rho_j \Delta \lambda_j = \Delta \mu_j \forall j, \mu_j + \Delta \mu_j = \sigma_j \mu_j > 0, \quad (35)$$

where we have ignored the $\Delta \rho_j \Delta \lambda_j$ term. If we treat $\Delta i_{\hat{R}\hat{\mathcal{E}}}, \Delta i_D := \Delta \rho$ as current variables, $\Delta y, \Delta v_D := -\Delta \lambda$ as voltage variables and keep the increments small enough so that $\rho + \Delta \rho > 0$ and $\sigma_j \mu_j > 0$, these are the equations for the ‘incremental’ network in Figure 6 (b) where an incremental current or voltage variable Δz is denoted z' . Note that $\Delta \rho_j \lambda_j + \rho_j \Delta \lambda_j = \Delta \rho_j \lambda_j - \rho_j \Delta y_j = \Delta \mu_j = (\sigma_j - 1) \mu_j$ has the form $v'_D = R' i'_D + E'_j$, where $v'_D := \Delta y_j = -\Delta \lambda_j, i'_D := \Delta \rho_j, R' := (\rho_j)^{-1} \lambda_j, E'_j := (\rho_j)^{-1} (1 - \sigma_j) \mu_j$.

Each iteration requires one solution of the incremental network. From iteration to iteration the change in the incremental network is only in the parameters R' and E' . The resistive multiport (on the left of Figure 6 (b)), remains invariant. Preconditioned conjugate gradient methods (see for instance [9]) are very suited for such situations, the preconditioner being the factored version of the incremental network at the first step. The authors of [4] report that the number of iterations remains more or less constant (less than 30) when the size of the quadratic programming problem is of the order of 10^5 variables and constraints, with less than ten variables involved in each constraint. These methods appear very promising for computing approximate maximum power transfer as in Section 8.1.

12.1. Preconditioned Conjugate Gradient Method (PCG)

We sketch how PCG may be adapted to DRS network analysis while using the interior point method. We begin by describing resistive network analysis. For notational convenience we will assume that we have only resistors and current sources in the network. Since DRS networks permit transformation from the Thevenin to Norton form this is a feasible assumption. For retaining sparsity, it is better to work directly with nodal analysis equations rather than Equation 35, where the dense matrix \hat{R} is computed explicitly.

Let A be the reduced incidence matrix of the graph of the network obtained by omitting one row of the incidence matrix per component of the graph. We partition the columns of A in terms of resistors and current sources as $A = (A_R | A_J)$. The nodal analysis equations are

$$(A_R G A_R^T) v = -A_J \mathbf{J},$$

where \mathbf{J} is the vector of current source values, the matrix G is a diagonal matrix with positive entries along the diagonal representing the conductances. Since the current sources contain no cutsets, A_R has linearly independent rows, so that $(A_R G A_R^T)$ is symmetric positive definite. Even if the network is large, each row of A_R contains very few (say less than 5) nonzero entries. Since each column of A_R has at most 2 entries and G is diagonal, it can be seen that the total number of non zero entries of $(A_R G A_R^T)$ cannot exceed twice the number of resistors in the network. So the matrix is sparse, the ratio of nonzero entries to the total number of entries being bounded by $2|E_R|/n^2 = 10n/n^2 = 10/n$, where $|E_R|$ is the number of resistors and n , the number of nodes in the graph.

Computing the product $(A_R G A_R^T) x$ requires no more than $2|E_R|$ multiplications. There are very efficient techniques for factorizing such sparse matrices into triangular matrices in the form $(A_R G A_R^T) = LL^T$, retaining sparsity for the factors also. Solving (‘back substituting’) the equation $LL^T x = b$ is known to be inexpensive in comparison with the effort required for factoring. With this background let us adapt PCG described below, to DRS network analysis.

To solve $\hat{A}x = b$, with preconditioner $M = LL^T$.

$$\mathbf{r}_0 := \mathbf{b} - \hat{\mathbf{A}}\mathbf{x}_0, \quad \mathbf{z}_0 := \mathbf{M}^{-1}\mathbf{r}_0, \quad \mathbf{p}_0 := \mathbf{z}_0, \quad k := 0.$$

repeat

$$\alpha_k := \frac{\mathbf{r}_k^\top \mathbf{z}_k}{\mathbf{p}_k^\top \hat{\mathbf{A}} \mathbf{p}_k}, \quad \mathbf{x}_{k+1} := \mathbf{x}_k + \alpha_k \mathbf{p}_k, \quad \mathbf{r}_{k+1} := \mathbf{r}_k - \alpha_k \hat{\mathbf{A}} \mathbf{p}_k$$

if r_{k+1} is sufficiently small then exit loop.

$$\mathbf{z}_{k+1} := \mathbf{M}^{-1} \mathbf{r}_{k+1}, \quad \beta_k := \frac{\mathbf{r}_{k+1}^\top \mathbf{z}_{k+1}}{\mathbf{r}_k^\top \mathbf{z}_k}, \quad \mathbf{p}_{k+1} := \mathbf{z}_{k+1} + \beta_k \mathbf{p}_k, \quad k := k + 1,$$

end repeat

The main computational effort in each iteration, ignoring the dot products, is in the product $\hat{\mathbf{A}} \mathbf{p}_k$ and in the solution of $\mathbf{M} \mathbf{z}_{k+1} := \mathbf{r}_{k+1}$. When $\hat{A} = (A_R G A_R^T)$, We have seen that $\hat{\mathbf{A}} \mathbf{p}_k$ requires not more than $2|E_R|$ multiplications and $\mathbf{M} := (A_R G_{initial} A_R^T)$ corresponds to the resistor values at the beginning of the iteration and is available in the factored form. So solution of $\mathbf{M} \mathbf{z}_{k+1} := \mathbf{r}_{k+1}$ is inexpensive.

13. Conclusion

We have presented new and efficient methods of computing, explicitly or approximately, port characteristics and maximum power transfer conditions for diode resistor source (DRS) 1– ports. We have adapted gradient descent methods to the solution of networks with piecewise linear devices and polynomial time interior point methods to the solution of DRS networks.

Appendix A. Convex Programming

A convex programming problem is defined to be the following.

$$\text{Minimize } \phi(x) \text{ equivalently Maximize } -\phi(x) \tag{A.1}$$

$$g(x) \geq 0, \tag{A.2}$$

where $\phi(x)$ is a convex function and $g(x) \geq 0$ defines a convex region. For convenience, we rewrite Equation A.1 as

$$\text{Minimize } \phi(x) \text{ equivalently Maximize } -\phi(x) \tag{A.3}$$

$$g(x) - \rho = 0, \rho \geq 0. \tag{A.4}$$

Let $x^T := (x_1, \dots, x_n), g(x)^T := (g_1(x), \dots, g_m(x)), \partial\phi(x)^T := (\partial\phi(x)/\partial(x_1), \dots, \partial\phi(x)/\partial(x_n)), dg(x)^T := (\partial(g_1(x)), \dots, \partial(g_m(x)))$. Suppose the optimum occurs at x^0 and Δx is the perturbation about x^0 satisfying $g(x_0 + \Delta x) \geq 0$. We must have $\phi(x^0 + \Delta x) \geq \phi(x^0)$, i.e., $\partial\phi(x)^T|_{x^0} \Delta x \geq 0$, whenever $g(x^0 + \Delta x) \geq 0$, i.e., whenever $dg_i|_{x^0} \Delta x > 0$, where $g_i(x^0) = 0$. Using Farkas Lemma (see for instance Section 5.8.3 of [2]), this means $\partial\phi(x)^T|_{x^0} = \sum_i \lambda_i \partial g_i^T|_{x^0}, \lambda_i \geq 0$, where $g_i(x^0) = 0$. Using the notation of Equation A.3, this becomes $\partial\phi(x)^T|_{x^0} = (\lambda_1^T | \lambda_2^T) dg|_{x^0} = \lambda^T dg|_{x^0}, \lambda^T \geq 0, \rho \geq 0, \lambda^T \rho = 0$. The vector λ can have positive components only in the positions where ρ has zero components (complementary slackness). Note that we have assumed that it is possible to perturb the optimal solution satisfying the feasibility condition $g(x) \geq 0$. (This can be shown to be true when the feasibility region has more than one point and is convex.)

These conditions can be shown to be also sufficient when $\phi(\cdot)$ is convex ($-\phi(\cdot)$ is concave) and the feasibility region defined by $g(x) \geq 0$ is convex. (If we have two points of local optimality, the line between them must lie in the convex region. Convex functions satisfy $\phi(\lambda x_1 + (1-\lambda)x_2) \leq \lambda\phi(x_1) + (1-\lambda)\phi(x_2), 0 \leq \lambda \leq 1$. Using this one can see that if $\phi(x_1) > \phi(x_2)$, then local optimality would be violated at x_1, x_2 .)

We are particularly interested in the case where $g(x) := Ax - b$. For this case, we refer to the constraints

$$Ax - \rho = b, \rho \geq 0, \quad (\text{A.5})$$

$$\partial\phi(x)^T|_{x_0} - \lambda^T A = 0, \lambda^T \geq 0, \quad (\text{A.6})$$

$$\lambda^T \rho = 0, \quad (\text{A.7})$$

as the Lagrangian form of the programming problem.

Interior point method ([16]) for Equation A.1, with $g(x) := Ax - b$, would begin with the formulation including a log barrier function in the term to be optimized,

$$\text{Minimize } \phi(x) - \mu \Sigma \ln \rho_j, \mu > 0, \quad (\text{A.8})$$

$$Ax - \rho = b, \rho > 0. \quad (\text{A.9})$$

The Lagrangian form for this problem is

$$Ax - \rho = b, \quad (\text{A.10})$$

$$\partial\phi(x)^T|_{x_0} - \lambda^T A = 0, \quad (\text{A.11})$$

$$\rho_j \lambda_j = \mu \quad \forall j, \mu > 0, \quad (\text{A.12})$$

keeping $\rho > 0$ always.

The incremental version of the Lagrangian form is

$$A\Delta x - \Delta\rho = 0, \quad (\text{A.13})$$

$$\partial\phi(x)^T|_{x_0+\Delta x} - \partial\phi(x)^T|_{x_0} - \Delta\lambda^T A = 0, \quad (\text{A.14})$$

$$\Delta\rho_j \lambda_j + \rho_j \Delta\lambda_j = \Delta\mu = (\sigma - 1)\mu \quad \forall j, \mu > 0, 0 < \sigma < 1. \quad (\text{A.15})$$

Remark 5. *Dennis's treatment [5] of convex programming (as opposed to quadratic programming) does not appear substantially more general. It also does not appear to have an electrical interpretation. It is not clear how to bring in complementary orthogonality. However Equation A.5 is simpler if we also work with a function $\phi(x) := \frac{1}{2}(x^T Px) + \mathcal{E}^T x$. If $\phi(x)$ is strictly convex, then Px is a strictly increasing function, i.e., $(z - x)^T Px < (z - x)^T Pz, z \neq x$. In the derivation of Equation A.5, let us take $x := i, y := Px, v := y + \mathcal{E}$. It follows that $v := -A^T \lambda$. Since $Ai \leq 0$ and $\lambda \geq 0$, we can see that $i^T v = -i^T A^T \lambda \geq 0$. Therefore $\mathcal{E}^T x = \mathcal{E}^T i \geq -i^T (v - \mathcal{E}) = -x^T y$. In the network of Figure 6 (a), if we take $v = \partial\phi(x), y = v - \mathcal{E}$, equivalently, $x = -\partial\theta(y)$, i.e., $i = -\partial\theta(v - \mathcal{E})$, the topological and device characteristic constraints together are equivalent to the Lagrangian form of the primal convex programming problem*

$$\text{Minimize } \phi(x) := \frac{1}{2}(x^T Px) + \mathcal{E}^T x \quad (\text{A.16})$$

$$Ax \leq 0 \quad (\text{A.17})$$

or its dual

$$\text{Maximize } \theta(y) := -\frac{1}{2}(y^T P^{-1}(y)) \quad (\text{A.18})$$

$$y = -\mathcal{E} - A^T \lambda, \lambda \geq 0. \quad (\text{A.19})$$

Now $\theta(y)$ is the Legendre dual of $f(x) := \frac{1}{2}(x^T Px)$. We have the general inequality $f(x) - \theta(y) - x^T y \geq 0$. It then follows that $f(x) + \mathcal{E}^T x - \theta(y) \geq 0$ in general and $f(x) + \mathcal{E}^T x - \theta(y) = 0$ for optimality.

This is only slightly more general than the one with a resistive multiport in Figure 6 (a). Instead of P being symmetric positive definite, Px is taken as strictly increasing without insisting on symmetry.

Appendix B. Proofs of results in Section 2.1

We need the following preliminary result for the proofs.

Lemma 28. *Let \mathcal{N}_P be a multiport with devices which are either diodes or those whose $v - i$ characteristics are continuous piecewise linear with positive slope. Let the set of diodes and ports contain no loops or cutsets. Let some of the ports be terminated by voltage sources and others by current sources. Then the resulting network \mathcal{N} has atmost one solution.*

Proof. Let the sources at the ports P be $\mathcal{E}_1, \dots, \mathcal{E}_{k_1}, \mathcal{J}_1, \dots, \mathcal{J}_{k_2}$. Suppose $(v'_1, \dots, v'_n, i'_1, \dots, i'_n)$, $(v''_1, \dots, v''_n, i''_1, \dots, i''_n)$ are two distinct solutions of \mathcal{N} for the same source values. Then by Tellegen's Theorem, we must have $\sum (v'_j - v''_j) \times (i'_j - i''_j) = 0$. We consider the following partition of the devices.

- Sources;
- subset of diodes in which the state is the same in both the solutions;
- subset of diodes in which the state is different in the two solutions;
- devices with continuous piecewise linear positive slope $v - i$ characteristics;

The terms corresponding to the first two kinds of branches will have either $(v'_j - v''_j)$ or $(i'_j - i''_j)$ equal to zero. It follows that the remaining terms must add up to zero. Now, in the latter two kinds of devices, if (v', i') , (v'', i'') are two distinct points in the characteristic, we must have $(v' - v'') \times (i' - i'') > 0$. We therefore have a contradiction unless there are no diodes in which the state is different in the two solutions and in the last kind of device we have $(v'_j, i'_j) = (v''_j, i''_j)$. The set of diodes and ports contains no loops or cutsets and therefore the remaining devices contain both a tree and a cotree. Therefore their voltages and currents (which are the same in both the solutions) uniquely determine the voltages and currents of the diodes and ports. Thus the two solutions are identical. We conclude that \mathcal{N} can have atmost one solution. \square

Proof. (Theorem 3) By Theorem 2, \mathcal{N} has atleast one solution. By Lemma 28, \mathcal{N} has atmost one solution. The result follows. \square

Proof. (Theorem 4) By Lemma 28, \mathcal{N} has atmost one solution. If every piecewise linear device were replaced by its realization with diodes, positive resistors and sources as in Lemma 5, we get a network \mathcal{N}' which has a solution. It follows that \mathcal{N} has a unique solution. \square

Appendix B.1. Realization of piecewise linear devices

Example 29. *Figure B.7 indicates a general scheme for realizing (continuous positive slope) piecewise linear devices using diodes, positive resistors and sources. The procedure is in terms of series parallel combination of basic module 1- ports which have a unique solution for any port voltage or current. By Theorem 20, it follows that the resulting multiport also has a unique solution for any port voltage or current. Figure (a) shows the $v - i$ characteristic of a piecewise linear device with 3 states. The corresponding line segments have slopes G_0, G_1 and G_2 . Figures (b) and (c) show primitive piecewise linear devices which agree with the original device. The resistors R_0, R_1, R_2 have values in ohms which are reciprocals of G_0, G_1, G_2 respectively. The corners occur at (v_1, i_1) and (v_2, i_2) . The resistance value of R_{10} is $1/(G_1 - G_0)$, R_{12} is $1/(G_1 - G_2)$, and of R_{21} is $(1/G_2) - (1/G_1)$. The values of the newly introduced sources are as follows: $E_0 = v_1 - R_0 i_1, E_2 = v_2 - R_2 i_2$.*

Informally, the circuits are built as follows. Start from the left. Build the circuit which has the given straight line characteristic. We have used a Thevenin equivalent. At the first corner, the characteristic has to change. If, as in the present example, the conductance increases, add a parallel branch with a diode in series with a resistor and voltage source. This limb of the circuit becomes active for voltage greater or equal to v_1 . (Below this level it behaves like an open circuit.) The conductance in this branch is the excess over the previous conductance level. Suppose at the next corner the the conductance decreases (i.e., the resistance increases). Add a series branch with a diode in parallel with a current source and resistor. This limb of

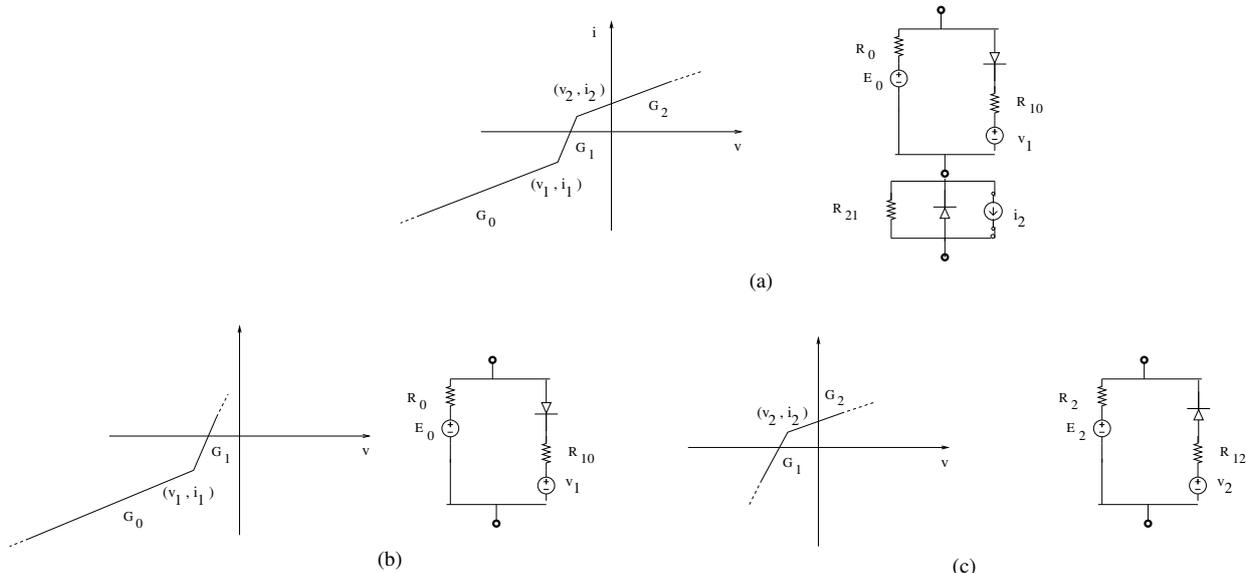


Figure B.7: Realization of piecewise linear devices using diodes

the circuit becomes active for current greater or equal to i_2 . (Below this level it behaves like a short circuit.) The resistance in this branch is the excess over the previous resistance level.

A similar construction is possible starting from the right and reducing the voltage. As before, when the conductance reduces (moving left in this case), a parallel module, and when it falls, a series module have to be introduced.

The primitive DRS realization in (b) is by moving from left to right and in (c), is by moving from right to left. In (b) the limb containing the diode becomes active above voltage v_1 and in (c) the limb containing the diode becomes active below voltage v_2 .

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