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# UHF RFID Tag Robustness

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## Abstract

RFID systems (radio frequency identification) purpose is to transmit information between a reader and a passive receiver distant of few meters. The receiver or tag is powered by the conversion of the incident wave in a dc voltage. The amplitude of the wave decreases rapidly with distance and makes it necessary to use a RF / DC converter. The converter generates a continuous voltage higher than the incoming voltage amplitude. This study presents the impacts of some of the most fluent parameters on the effectiveness of multipliers RF / DC and on the antenna mismatch.

## 1. Introduction

The circuit is composed of three distinct parts, each representing about one-third of the total surface of the chip (for the chips that meet the EPC Gen2 standard with a memory of 400 to 500 bits)

- The analog part, it includes the converter RF / DC, the voltage regulator with a reference oscillator and the receiver, and a block to the start and stop of the circuit depending on the strength of field (POR: Power On Reset).
  - Digital, it handles the protocol and commands all the functions of the tag. It represents 15000 logic gates.
  - The plan memory, its size is not limited by the EPC standard; however UHF products currently contained with a small map memory. It incorporates a portion analog high voltage needed to writing in the EEPROM cells
- The architecture of the tag is shown in figure I.

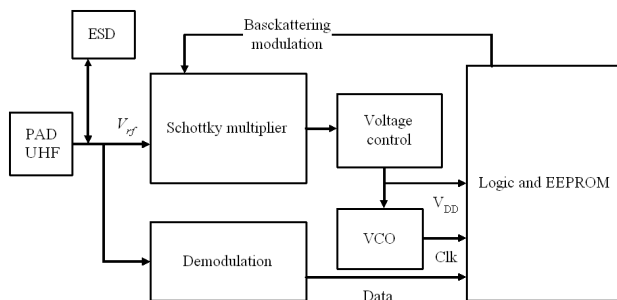


Fig. 1 UHF RFID system

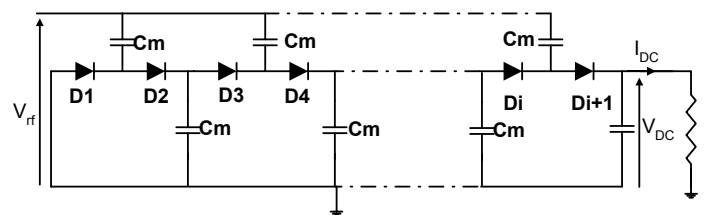


Fig.2 RFID multiplier

The configuration is close to the HF circuit. However, some important differences are worth noting. First, there's no matching circuit in IC. The antenna is designed to ensure impedance close to the conjugate impedance of the chip, so, matching networks are unnecessary. Second, in UHF RFID, the IC recovers power thanks to a voltage multiplier circuit. Indeed, received waves are too low to permit the rectifier to power the circuit. That's why a multiplier is used to increase the voltage. So it's crucial to warranty the system functionality. Its effectiveness directly affects the scope of the system: lower is the power for which it is able to deliver the voltage needed, longer is the range of the system. In this kind of circuit, an architecture based diodes or MOS transistor predominates, it is represented on figure 2.

The design of these circuits is subject to significant constraints. Paradoxically, the design parameters which affect the performance are often poorly defined. In this context the use of an analytical model allows to quickly determine the best design solution [1, 2]. However, as the conception of voltage multipliers is very sensitive, corners simulations have to be done in order to evaluate the robustness of the best solution. These corners simulations can consume huge time and prove that the chosen solution is not stable enough. In this study, the impact of variation in the fabrication process is discussed, the aims is to find the best and most robust solution in face of process variation for the chip or the antenna.

## 2. Multiplier's key parameters

The IC input impedance depends mainly of multiplier's design parameters such as Schottky size or number of stages. In fact, three elements are connected to the antenna pad and influence chip input impedance: the input pad, the ESD circuits and the multiplier.

### 2.1. Multiplier model

The input impedance of an integrated multiplier circuit is capacitive. An antenna with inductive impedance is generally used to achieve a power matching [3]. The equivalent circuit including the antenna and the tag input at the fundamental frequency of the incident RF wave is given in figure 3. The input impedance ( $Z_{chip}$ ) of the chip is composed of  $R_{IC}$  and  $C_{IC}$ , which are non-linear functions of the magnitude of the input voltage  $V_{rf}$ .

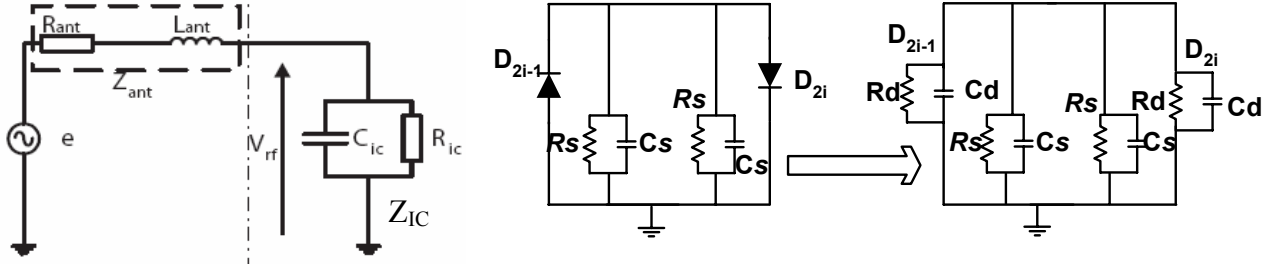


Fig. 4 One multiplier stage equivalent circuit

For the multiplier shown in fig.2, it has been established in previous study [4], that the current can be expressed in term of modified Bessel functions series:

$$I_D \approx I_s \left[ \exp\left(\frac{Vd}{n_i \cdot vt}\right) \left( B_0 \left( \frac{|V_{rf}|}{n_i \cdot vt} \right) + 2 \sum B_n \left( \frac{|V_{rf}|}{n_i \cdot vt} \right) \cdot \cos(n\omega t) \right) \right] \quad (1)$$

$$= I_{DC} + \sum Id_n \cos(n\omega t)$$

$B_n$  are Bessel functions. The voltage applied on each diode called  $Vd$  can be expressed in function of multiplier output voltage and number of multiplier stages (N):

$$V_d = \frac{-V_{DC}}{2 \cdot N} \quad (2)$$

So for a fixed IDC and VDC, this equation can be solved numerically to get the value of incident voltage  $|V_{rf}|$  with. The expression of the first harmonic can then be calculated. And then the non-linear resistive part of each diodes impedance at first harmonic can be computed for a given  $V_{rf}$  input voltage magnitude:

$$Rd = \left| V_{rf} \right| / \left| Id_1 \right| \quad (3)$$

Considering the multiplier topology for each stages, and if the impedance of the capacitors  $C_m$  is large enough to be negligible around 900 MHz, each impedance stage can be calculated with the equivalent circuit given on Fig. 4. On this circuit, substrate losses are taken into account by the network  $R_s, C_s$ .

Substrate losses are in parallel with the diode equivalent circuit  $R_d C_d$ . The complete chip input impedance including the input pads and the ESD protection circuit is given in Eq 4. ESD and pads effects are negligible on the resistive part of the IC impedance. However, they must be taken into account on the imaginary part of the input impedance.

$$R_{IC} = \frac{1}{2N} \frac{Rd \cdot Rs}{Rd + Rs} \quad C_{IC} = 2N \cdot (Cd + Cs) + C_{pad} + C_{ESD} \quad (4)$$

The maximum power transfer between antenna and chip is obtained under matching condition. It is possible to determine antenna impedance corresponding to the computed chip impedance thanks to Eq 5:

$$Z_{ANT} = Z_{IC}^* \quad (5)$$

Thanks to this model, we can determine the first harmonic impedance, the input power to reach a fixed operating point ( $V_{DC}, I_{DC}$ ) and the efficiency of the multiplier.

$$P_{IN} = \left| V_{rf} \right|^2 / 2R_{IC} \quad \eta = P_{OUT} / P_{IN} \quad (6)$$

The model allows determining main multiplier characteristic: input impedance and efficiency versus design and process parameters. Then, with this tool once the best design solutions was selected, its robustness can be evaluated thanks to a variation of process input parameters.

## 2.2. Results and robustness on the chip

Thanks to the model, main design parameters can be computed for a selected technology: Fig. 5 shows the diodes surfaces have to be chosen as small as possible and the number of stages reduce to the minimum.

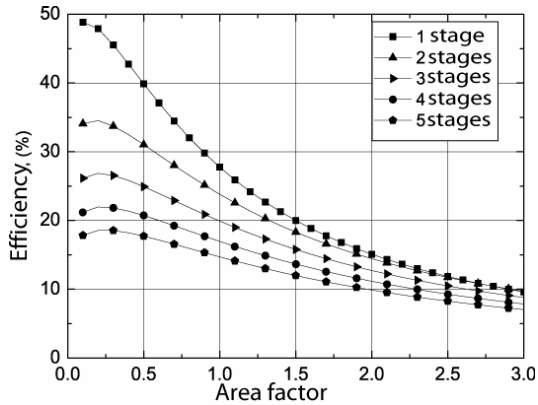


Fig. 5 Efficiency vs Area factor and number of stages

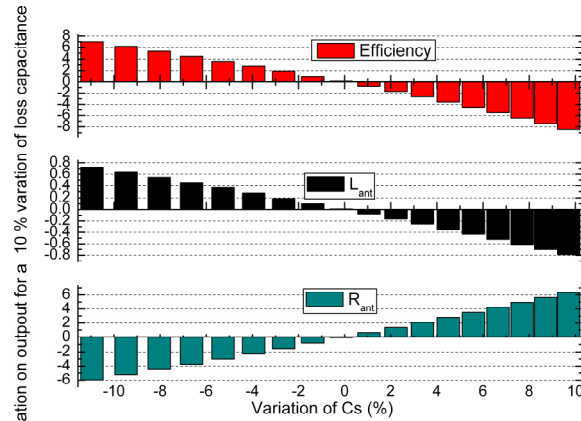


Fig. 6 Impact of capacitor losses variation

However, if this choice of diodes sizes and number of stages seems to be optimal, this result mainly depends on process parameters such as  $I_s$ ,  $R_s$ , and  $C_s$ . In order to estimate the impact of process deviation, a variation of 10% is applied on technologies parameters.

First studied parameter is the loss capacitance, called  $C_s$  in the model; result on 10% variation for a one stage multiplier is presented in figure 6. This variations leads to an important imprecision on the efficiency ( $\pm 8\%$ ), moreover a part of received power will be wasted due to the mismatch. Indeed antennas have fixed impedance and if it is matched to standard chip impedance process variation will be ignored and antenna and chip would be mismatched.

On Table 1, results on process variation for different parameters are presented. From these results many guidelines for robust design appear:

- increasing the number of multiplier stages decreases the efficiency variations
- The imaginary part of the matched antenna is robust versus process variation
- The saturation current of diodes has less impact on performance than subtract losses ( $R_s$  and  $I_s$ )

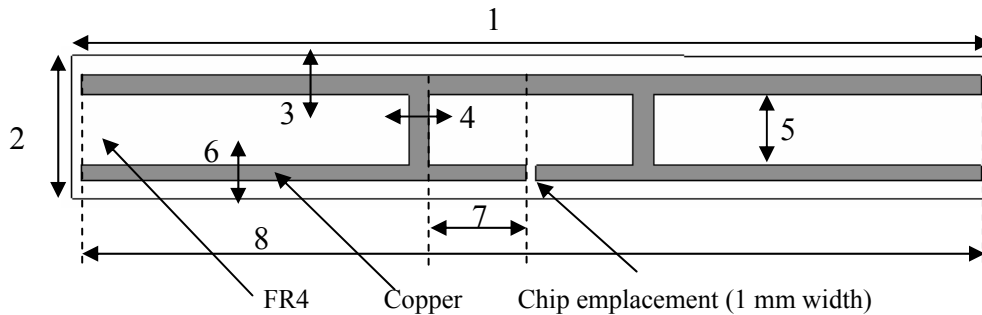
Table 1: Impact on multiplier of  $\pm 10\%$  variation on process parameters for different number of stages

Number of stages	Variation	$R_{ant}$	$L_{ant}$	Efficiency
N=1	$R_{sub} \pm 10\%$	$\pm 4\%$	$< 1\%$	$\pm 10\%$
N=1	$C_{sub} \pm 10\%$	$\pm 6.33\%$	$< 1\%$	$\pm 8\%$
N=1	$I_s \pm 10\%$	$< 1\%$	$< 1\%$	$< 1\%$
N=3	$R_{sub} \pm 10\%$	$\pm 2.5\%$	$< 1\%$	$\pm 6\%$
N=3	$C_{sub} \pm 10\%$	$\pm 1.4\%$	$\pm 2\%$	$\pm 5\%$
N=3	$I_s \pm 10\%$	$< 1\%$	$< 1\%$	$\pm 0.6\%$
N=5	$R_{sub} \pm 10\%$	$\pm 2\%$	$< 1\%$	
N=5	$C_{sub} \pm 10\%$	$\pm 1.2\%$	$\pm 2.5\%$	$\pm 3.8\%$
N=5	$I_s \pm 10\%$	$< 1\%$	$< 1\%$	$\pm 0.7\%$

These results lead to a modification in the design methodology of a RFID chip, the key design parameter can be selected not only for their performances but also for their sensitivity on process variation.

### 3. Complete System robustness

Once a chip solution has been selected with minimum shift on the input impedance, a matched antenna has to be designed. Due to the chip impedance, the antenna need to be very inductive with a very low resistance as presented in [5]. An antenna topology has been chosen to be adapted on the circuit impedance (Fig 7). Once the design finished a sensibility study is done on some of the antenna's parameters (table2) in order to estimate the robustness of the matching between chip and antenna.



N°	Name	Value(mm)
1	LFR4	90
2	WFR4	14
3	W1	2
4	W2	2
5	L1	6.9
6	W4	1.5
7	L2	10
8	L3	88.2

Fig. 7 antenna layout

Table 2: Impact on antenna impedance of  $\pm 5\%$  variation on antenna's parameter

	$R_{ant}$ maximum variation	$L_{ant}$ maximum variation
$\epsilon_r \pm 5\%$	6.33%	1.8%
T(metal tickness) $\pm 5\%$	3.8%	1.3%
W (line width) $\pm 5\%$	15%	3%

As for the chip, the imaginary part seems to be the most robust parameters on the antenna. Owing to the very low resistance of the RFID chip, variations about few ohms on the antenna's impedance involve great mismatch on complete system. So, the real part of the antenna's impedance is very sensitive to variation especially on line width.

### 4. Conclusion

This study showed the sensitivity of a tag to the fabrication process and guidelines are presented to increase the total system robustness. The most critic parameter to control is the real part of the chip and antenna. This parameter is very sensitive on chip and antenna variations, with a difference respectively about 4 to 15% on antenna and up to 6.3% on chip. A simple way to increase chip stability is to increase the number of stages, with considering that the efficiency do not become to small. Increasing the tag robustness is very important in RFID applications in which chip must be very low cost and operating of an important number of tag, should be preferred to the performance of a few.

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