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# Design of a 35 kW Power Equipment for energy harvesting in the aeronautic context

Hassan Cheaito  
Univ Lyon, INSA Lyon, Univ Claude  
Bernard, Ecole Centrale Lyon, CNRS,  
F-69621  
Villeurbanne, France  
hassan.cheaito@insa-lyon.fr

Joris Pallier, Paul Albouy  
Power Department Centum Adeneo  
Ecully, France  
jpallier@centumadeneo.com

Pascal Pommier-Petit  
Power Department Centum Adeneo .  
Ecully, France  
ppommier-petit@centumadeneo.com

Bruno Allard  
Univ Lyon, INSA Lyon, Univ Claude  
Bernard, Ecole Centrale Lyon, CNRS,  
F-69621  
Villeurbanne, France  
bruno.allard@insa-lyon.fr

Guy Clerc  
Univ Lyon, Univ Claude Bernard, INSA  
Lyon, Ecole Centrale Lyon, CNRS,  
F-69621  
Villeurbanne, France  
guy.clerc@univ-lyon1.fr

XXX  
Univ Lyon, Univ Claude Bernard, INSA  
Lyon, Ecole Centrale Lyon, CNRS,  
F-69621  
Villeurbanne, France  
xxxx@univ-lyon1.fr

**Abstract**— Electrical power systems is steadily gaining in importance as more subsystems are electrified to improve overall aircraft efficiency and reduce CO2 emissions. This paper deals with the design of a 35 kW – 2500 Wh equipment (SUNSET) intended to recover energy from aircraft electrical brake. First, the the main technical and electrical characteristics of SUNSET prototype are described. The design of the pack battery is detailed, highlighting the battery management. A power module has been designed and validated using Insulated Metal Substrate board. Losses and electrical performance are tested. From the system viewpoint, it is shown that the power density target is reached within the converter but still not satisfying at the storage system level.

**Keywords**—Energy Storage System, Battery Management System (BMS), Bidirectional converter (BDC), SiC MOSFET

## I. INTRODUCTION

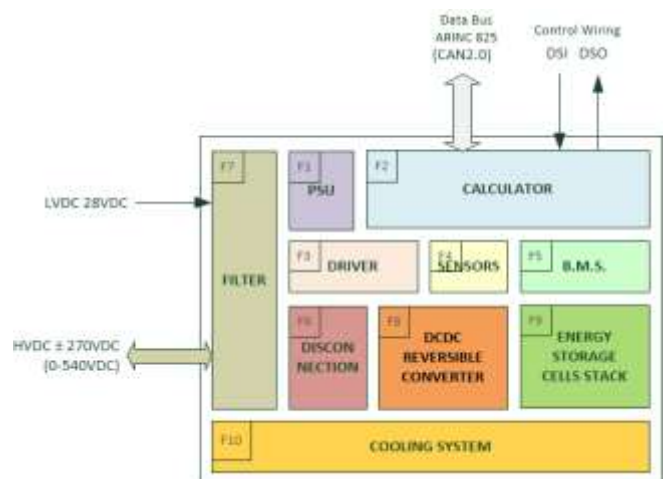
Electric Taxiing (ET) for landing systems will allow the aircraft to push-back and taxi under on-board generated electrical power without the main engines running [1]. The ET is estimated to save up to 4% of the total fuel used on a flight, especially for short range flights. In addition, this system allows aircrafts to push back without support from an external tug. Thus, ET equipped aircrafts will be able to operate more quickly, thereby reducing both gate and tarmac congestion and CO2 emission.

As part of the development of the more electrical aircraft, a new project of Storage energy UNit for Smart and Efficient operation on Tarmac (SUNSET) is being developed. The main objective of this project is to recover energy at braking during the aircraft taxiing phase (after landing). The final goal is to develop a demonstrator integrating both energy storage system and bidirectional converter.

This paper describes the hardware design of the SUNSET equipment. It is important to note that this paper is a follow-up of the trade-off study presented in [2]. As mentioned in [2], the design of this equipment is very challenging because, in addition to the high power and energy densities (30 Wh/kg – 2 kW/kg – 60 Wh/dm<sup>3</sup>), it should meet all the aeronautic specifications, in DO160 reference book, such as safety, vibration stress, electromagnetic compatibility (EMC), etc....

This paper is organized as follows. The functional architecture is reviewed in Section II. Section III covers the

balancing strategy and the Energy Storage System (ESS). The DC-DC power converter is described in Section IV. Finally a few concluding remarks and further steps are drawn in Section V.



Synopsis of the architecture of the SUNSET prototype.

## II. SYSTEM ARCHITECTURE

This section discusses the main sub-functions of the system in order to understand how the overall system will operate. As depicted in Fig. 1, the architecture is based on the following main sub-equipments:

- A control board,
- A power converter including drivers and IMS power board and inductors,
- An energy storage system including battery cells, battery management system (BMS) and protection circuit,
- Two interconnecting boards for LV and HV.

The control board consists in three main functions: the primary manager, digital control and ultimate fault monitoring. Besides, all functional states and communication are managed by the control board.

The bidirectional DC-DC converter is based on a buck architecture. The buck is used to lower the input HVDC voltage to the battery voltage level. On the other side, it is necessary to step-up the battery voltage to the input HVDC voltage level using a boost converter operation. The boost

converter is obtained by replacing the diode of the buck converter by a second MOSFET.

The Energy Storage System (ESS) includes three independent packs of 100 cells. The cells are connected in series. In addition, the ESS contains one BMS per pack that monitors and balances the cell states of charge (SoC). Furthermore, a hardware isolation between the battery pack and the converter is a mandatory requirement. For this reason, a solid-state protection circuit (SSPC) board solution has been chosen for its compactness (compared to a circuit breaker). The SSPC limits the battery inrush current due to the charge of various capacitors. The SSPC is controlled by the BMS. The latter system disconnects the pack (by opening the SSPC) in case of a hard fault.

The **J1** board manages the digital input and output signals between the SUNSET control unit and the aircraft one. The **J2** board is the HVDC input of the SUNSET prototype which contains mainly the EMC filter.

### A. Voltage Control

One of the intrinsic objectives of the SUNSET prototype is to maintain the aircraft HVDC network around a stable 560 V DC. In this Section, the different conditions to operate as a buck or boost converter are discussed. As mentioned before, the SUNSET prototype features two main operations:

- i. Charge or buck mode: it recovers the electrical energy supplied by the inverter during the electric brake phase.
- ii. Discharge or boost mode: restore the electrical energy from the battery to the aircraft network through the inverter during electric traction phase.

Notice that there is a standby mode when there is no energy transferred between the battery and the aircraft network. Whatever the SoC of the battery pack, this mode is active when  $B < HVDC < C$  (see Fig. 2). However, to enter into buck or boost mode, there are two hysteretic conditions between the HVDC and battery pack voltages.

**Buck:** If  $HVDC > D$  the SUNSET prototype can recover energy from the aircraft network if and only if the SoC of the battery pack is lower than level F. The pack may be charged until level E. The standby mode will be reactivated when the HVDC voltage reaches level C.

**Boost:** If  $HVDC < A$  the SUNSET prototype can restore energy from the battery pack to the aircraft network if and only if the SoC of the battery pack is higher than level G. The battery pack may be discharged until level H. The standby mode will be reactivated when the HVDC voltage reaches level B.

For security issues, the point of level E might be limited to 90% of maximum charge level. On the other hand, to extend the battery lifetime, the point of level H might be limited to 20% of maximum charge level.

### B. Balancing Strategy

Balancing in battery pack is the concern of literature focus about the hardware implementation [3]. The most common topologies are divided into two categories:

- Passive: fixed shunt resistors or switched shunt resistors.

- Active: multiple switched capacitors, switched transformers and/or shared transformers.

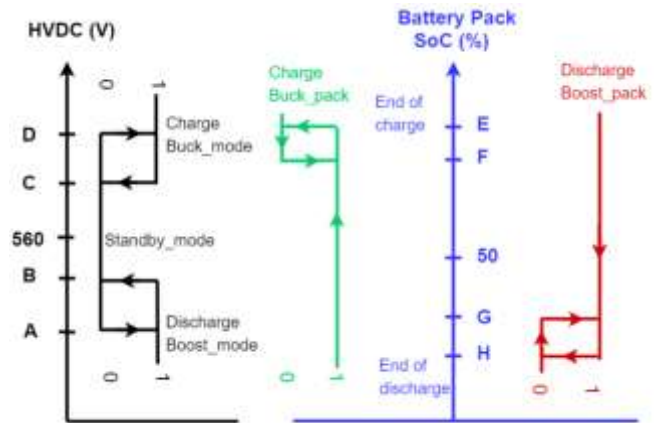


Fig. 1. The threshold voltage on the HVDC and SoC on the battery pack to activate the buck or boost mode

Balancing strategy is less highlighted in literature in the aeronautic context. This Section aims to discuss this issue. Indeed, the best strategy consists in optimizing the power capability: minimizing power losses and preventing cell overcharge. This is achieved by finding the optimal time and duration of cell power dissipation. With 100 cells in series the balancing is a fastidious task. In order to simplify the hardware implementation, the balancing method used in this study is based on the passive method: one resistor is connected across each cell of the pack to drain excess charge via a MOSFET [4]. As a result, 100 resistors and 100 MOSFETs are integrated on the BMS board. Each group of cells is monitored by a slave BMS which belongs all to one master BMS.

The battery is made of LFP technology. The voltage as a function of the battery SoC is very flat [5]. That's why the open-circuit-voltage (OCV) of a cell is not so representative of the actual SoC. Thus, the strategy should be expressed directly in terms of SoC. In this paper, we consider that SoC is well-given from BMS. And will not be discussed for the sake of place. In order to summarize, two main algorithms exist to choose the appropriate cell states to balance. *Top balancing*: balance the cells at the fully charged state (and let them diverge at the bottom). Inversely, *bottom balancing*, balance the cells at the discharged state and let them diverge at the top. In fact, bottom balancing has no merit in systems that utilize dissipative balancing because energy is released from the highest capacity cell to align with the lowest capacity one without improving the run time. With top balancing, the majority of cells could have high SoC whereas only several cells have low ones. In that case, the majority will be discharged to reach the minimum charge level.

For these reasons, another strategy is proposed for continuous operation for all SoC level. It takes into account both the SoC average value among all cells and the unitary ones. This strategy is shown in the flowchart in Fig. 3. First, the average SoC among the 100 cells (defined as  $\mu$ ) is evaluated in real time. Then, the SoC of each cell ( $\mu_i$ ) is compared to the average. This strategy allows a variability ( $\Delta\mu_i = \mu_i - \mu$ ) between the cells' SoC. In the case of a low average SoC, there is no real need to balance very accurately the battery pack. For instance, at average SoC  $< 30\%$ , 20% SoC variability is authorized. However, the higher the average SoC, the more critical the variability value. Actually,

at high average SoC, cells aging effect accelerates dramatically what compromises safety and security. This is why the SoC variability should not exceed 2% at the end of the battery pack charge.

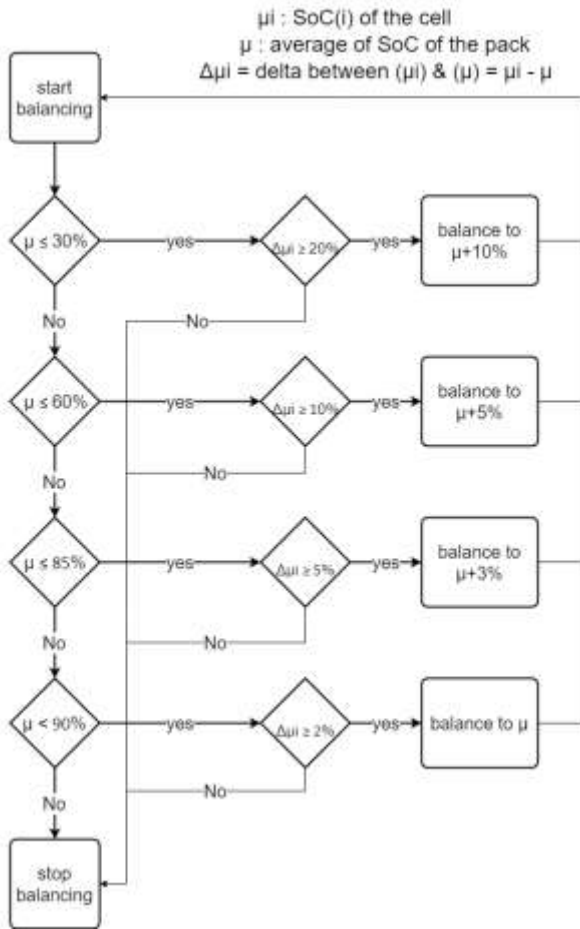


Fig. 2. Flowchart of the balancing strategy dependent on the average SoC of the battery pack

If not, cells could be overcharged leading to risk of thermal runaway. This algorithm will be implemented and validated in a further step.

### III. BATTERY PACK

This Section describes how to choose the power and energy densities of cells in order to meet initial challenges.

#### A. A123system cell

To build the energy storage system (ESS), the mechanical design will be based on the smallest unit which is the cell. According to the trade-off in [2], the A123system cell (2.5 Ah) has shown a very competitive energy density (240 Wh/L and 108 Wh/kg).

#### B. Packaging

The mechanical design of the SUNSET equipment is optimized in terms of weight and volume. The design of the equipment is mainly based on printed circuit boards that include several functions, in order to reduce the wiring and increase compactness. 20 battery cells are packaged in series into one module (see Fig. 4). 5 modules in series constitute one pack. For each pack (100 cells in series), there is one BMS board and one SSPC board. The ESS of the SUNSET equipment comprises three packs. At each packaging level,

the energy densities are evaluated. Fig. 5 shows how densities highly decrease from the cell level to the pack level.

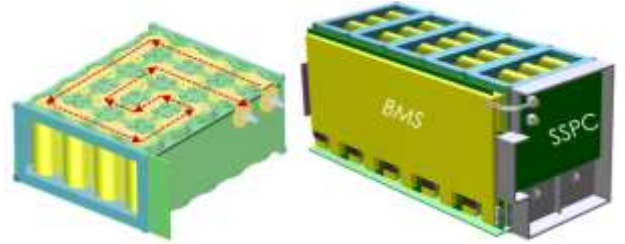


Fig. 3. The 3D schematic of one module (20 cells in series) and one pack (5 modules in series)

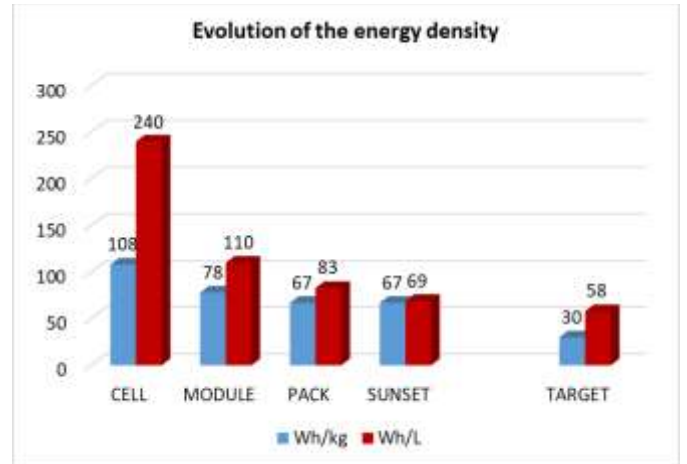


Fig. 4. Evolution of the energy density with packaging

From these latter results, we should consider the degradation in energy densities. The volume density drops down to 70% of the theoretical value (240 to 69) whereas the mass density decreases to 37% (108 to 67). However, the energy still meets the target fixed at the beginning of the project.

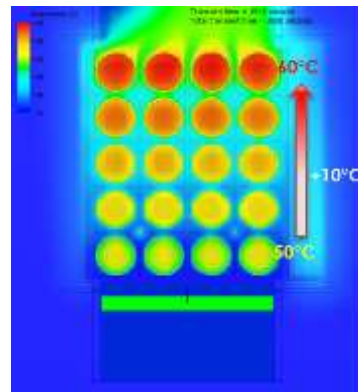


Fig. 5. Thermal simulation of the module in typical operation condition.

#### C. Cooling design

The cooling system is designed based on calculations and simulations from typical operation profiles and electrical losses in the devices at a specified ambient temperature (SiC MOSFET, battery cells and inductors). The mechanical design of sub-parts such as the battery module must reduce the local hot points in order to reduce the sizing of the cooling system. The cooling system is based on forced air ventilation (no water cooling authorized). The first results shown in Fig. 6 give an air

flow requirement equal to  $400\text{m}^3/\text{hr}$  in order to limit the absolute temperature to  $60^\circ\text{C}$ .

#### IV. POWER CONVERTER

This Section discusses the power converter architecture compatible with a nominal inrush power level of 35 kW.

##### A. Architecture

The designed DC-DC power converter is a two-voltage-level converter [6]. A leg comprises two Insulated Metal Substrate (IMS) board and each switch is a two-parallel-chip MOSFET (Fig. 7). The first objective of this topology is to reduce voltage constraints on semiconductor devices what allows to lower the switching losses. Another objective is to minimize voltage constraints on magnetic devices as inductors and capacitors, for easier integration on PCB due to low form factors. As can be seen in Fig. 7, three battery branches are connected to a three-interleaved-phase converter. A  $120^\circ$  phase delay is managed between the three phases thus reducing conducted emissions. Indeed the first harmonic seen by the HVDC network is related to the number of phases. The switching frequency is chosen to set the first harmonic below EMC limits. The high side and low side transistors of both levels are triggered simultaneously by  $\alpha$  and  $(1-\alpha)$  respectively.

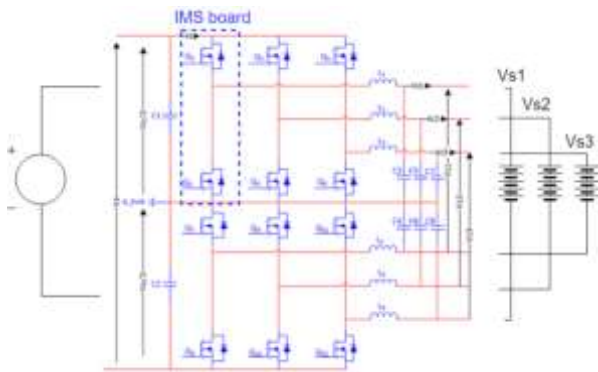


Fig. 6. Architecture of the converter

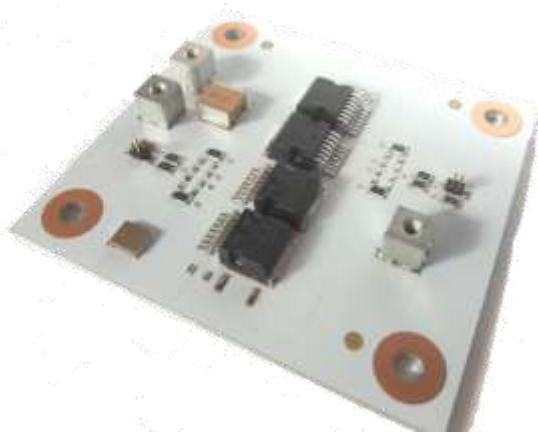


Fig. 7. Picture of the IMS PCB of one leg of one level of the designed architecture

##### B. Design of a PCB

IMS board is increasingly used in power electronics for its excellent heat transfer properties. The IMS board also privileges SMD components for more compact designs. However, the IMS board has a strong influence on the EMC, namely at the routing level. Indeed, in one hand, the proximity of tracks with a large conductive surface will allow minimizing their inductive effects. On the other hand, the common-mode capacitance will be larger. Routing becomes a key point for getting a circuit with good performances. The floating node area must be as small as possible to limit the common-mode capacitance. The symmetry of the circuit is extremely important to avoid common-mode to differential-mode conversion [7] (Fig. 8).

The SiC MOSFET technology seems to offer the best solution for high power density. The current design of the power converter based on this technology gives a final power density of  $3\text{kW}/\text{kg}$  (including inductors and heatsink). Besides, to reduce EMI issues, kelvin connections are highly recommended. Leadless or low-lead components are preferred as well to reduce parasitic inductance. In fact, SMD MOSFETs provide an easier soldering and wiring from the industrial point of view. For these reasons, D<sup>2</sup>-PAK with 4 pins (SCTH90N65G2V) has been chosen for the application.

A preliminary switching unit (dashed square in Fig. 7) using IMS and SMD SiC technology has been designed and manufactured as shown in Fig. 8.

##### C. Validation test of the elementary power board

This Section discusses the electrical performances of the designed board (switching, losses, and nominal power).

###### 1) Theoretical study

A theoretical analysis was able to predict the total losses in the high-side MOSFET of the board. It also allows evaluating losses distribution between switching (on and off) and conduction mode. For the sake of place, only the final results are shown, according to the measurement procedure detailed in [8]. The conditions in Table 1 have been considered for the buck mode. Fig. 7 shows the distribution of losses in the high-side MOSFET (11.9 W).

Switching Frequency	50 kHz	V input	325 V
Duty cycle	0.6	I output	30.1 A
Power	5.72 kW	Load	6.3

Table 1 Operating conditions of the elementary board

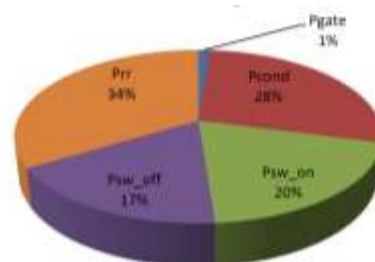


Fig. 8. Losses breakdown in the high-side MOSFET on the elementary power board

## 2) Electrical study

Tests in boost- and buck- modes have been performed at the maximum power of 5.8 kW. The switching frequency is settled at 50 kHz and the duty cycle is 60%. The dead time is set to 500 ns. Only the results for the high-side MOSFET in buck mode are presented. The curves in Fig. 10 show  $V_{GS}$  (yellow),  $V_{DS}$  (green) and  $I_D$  (red).

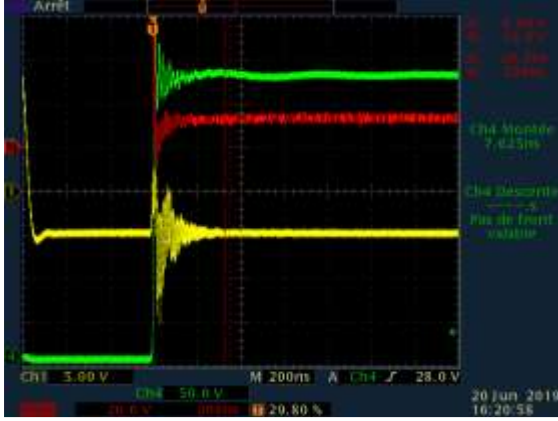


Fig. 9. Main waveforms on the high-side MOSFET on the elementary board:  $V_{GS}$  (yellow),  $V_{DS}$  (green) and  $I_{DS}$  (red)

This measurements validate the design of the IMS PCB. The gate voltage ( $V_{GS}$ ) does not exceed the minimum threshold of 1.7 V: no false turn-on will happen. Furthermore, the total losses have been evaluated using (1) from [9]:

$$P_{total} = P_{cond} + P_{com} + P_{rr} + P_{gate} \quad (1)$$

Where:

$P_{cond}$  : conduction losses

$P_{com}$  : commutation losses

$P_{rr}$  : reverse recovery losses

The total losses have been found to be around 11.5 W per MOSFET.

## 3) Thermal study

In order to validate the latter results, it was necessary to carry out thermal tests. First, the thermal resistance ( $R_{th,IMS}$ ) is calculated for the IMS PCB and then with the heatsinks to determine the global  $R_{th}$ . A series of tests have been done using the MOSFETs in the saturation region operation ( $V_{GS} < 10V$ ) to control the injected thermal power. The  $R_{th}$  can be deduced readily from the ratio of temperature elevation over the dissipated power. The  $R_{th}$  effective value is round 1.65°C/W for the overall board including the heatsink. Fig. 11 shows the elevation of temperature at IMS surface. Notice that the highest temperature point is 83°C when the ambient temperature is 28.3°C.

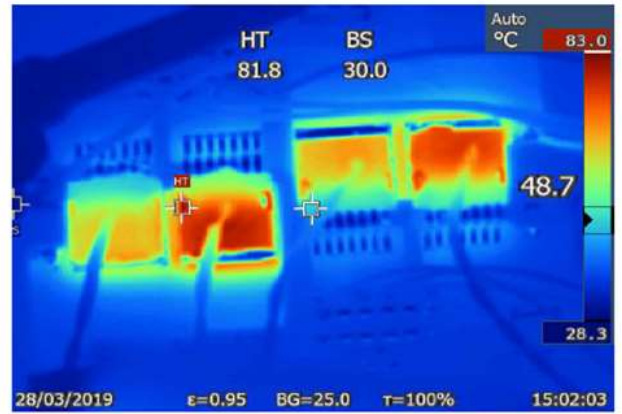


Fig. 10. Infrared camera picture of the elementary power board at 5.8kW and 28°C ambient temperature.

Once  $R_{th}$  is given, the same switching conditions as in section IV.C.2 have been applied. Temperature elevation ( $\Delta T$ ) has been measured to be 20°C. This means that the power losses using thermal measurements are equal to 12.1 W ( $\Delta T/R_{th}$ ).

Table 2 compares the previous results using the three methods. A good agreement has been found between theoretical and experimental evaluations.

Theoretical	Electrical	Thermal
11.9 W	11.5 W	12.1 W

Table 2 Losses from the high side MOSFET on the elementary power board at 5.8kW

The MOSFETs on the elementary power board enables to transfer power with an effective efficiency of 99.6%. Main losses are then awaited from passive components.

## V. CONCLUSION

This paper has presented the main technical and electrical characteristics of the SUNSET equipment. A new balancing strategy has been proposed. It decreases gradually the variability regarding the cells' SoC in the battery pack.

This work has shown that the power density of the cell alone is not significant. Study should take into account the packaging, BMS and protections. These added features reduce the densities to around 37% for the mass energy density and to 70% of the initial volume energy density.

IMS power switching unit has shown a good experimental agreement with the expected results. Six IMS boards are connected afterwards to create the entire power converter. The SUNSET demonstrator is under manufacturing. Next steps consist in validating of the performances of the whole equipment.

## ACKNOWLEDGMENT

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\*This output reflects only the author's view and that the JU is not responsible for any use that may be made of the information it contains.

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