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PAPER

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Abstract

In the present work, we investigate the effect of low phosphorus doped polysilicon thin films. These later are deposited on glass substrates by low pressure chemical vapor Deposition (LPCVD) technique and are *in situ* doped with phosphine adjunction to silane. Doping levels are reported by the phosphine to silane ratio Γ varying from 0 (undoped layer) to heavily doped layer almost 1.2×10^{-3} . Films are characterized by different techniques as Photothermal Deflection Spectroscopy (PDS), photoluminescence measurements and x-ray diffraction of polycrystalline layers. The last one reveals that doping concentration giving modification in crystallite size and presence of microstrain, so a clear reduction in the E_g value was observed for the slightest doped layer ($\Gamma = 3.7 \times 10^{-7}$) by comparison with the undoped one ($\Gamma = 0$). Results give evidence of an optimum doping level to obtain higher polysilicon films quality. Polysilicon film quality has been correlated to phosphorus doping levels. Thin film transistors (TFTs) are fabricated on glass substrate using a top gate four mask process at low temperature (< 600 °C). Electrical characterizations highlight significant improvements in the TFTs performances using slightly doped film instead of undoped one as active layer. Based on Levinson's model, density of states within the grain boundaries is also found to be the lowest. Stability under stress is enhanced too. For slightly doped films, electrical characterizations indicate that both threshold voltage V_{th} and density of states N_T within the grain boundaries have their lowest values. Although, the field effect mobility μ records its highest values. Additionally, low doping levels enhances the TFT stability under stress. As a result, the *in situ* low doping strategy opens the way to manufacture polysilicon electronic devices exhibiting high electrical performances and a rather high stability under stress effects.

1. Introduction

Polycrystalline silicon thin films are used in the low cost fabrication of large area electronic devices as active matrix flat panel displays [1, 2]. Devices performances are strongly correlated with polysilicon films quality because electrical properties are strongly affected by the presence of defects in polysilicon layers [3]. High quality polysilicon films can be obtained using different methods as laser annealing [4], metal induced lateral crystallization [5] or using disilane as gas source [6] in order to increase grain size.

So many study [7] shows that the properties of the annealed phosphorus n-doped silicon films are dependent on the crystallization method used SPC crystallization technique [8, 9], increasing the phosphorus content favors the crystallization process in terms of an enhancement of the crystal growth rate for SPC. Crystallization step was performed at 600 °C for several hours by a rapid thermal annealing [10] or by laser excimer annealing [11]. Wherein a laser can be used to minimize the heating of the glass substrate [12]. Poly-Si TFTs have a higher carrier mobility and higher driving current, this characteristic allow the increase of the response speed of the

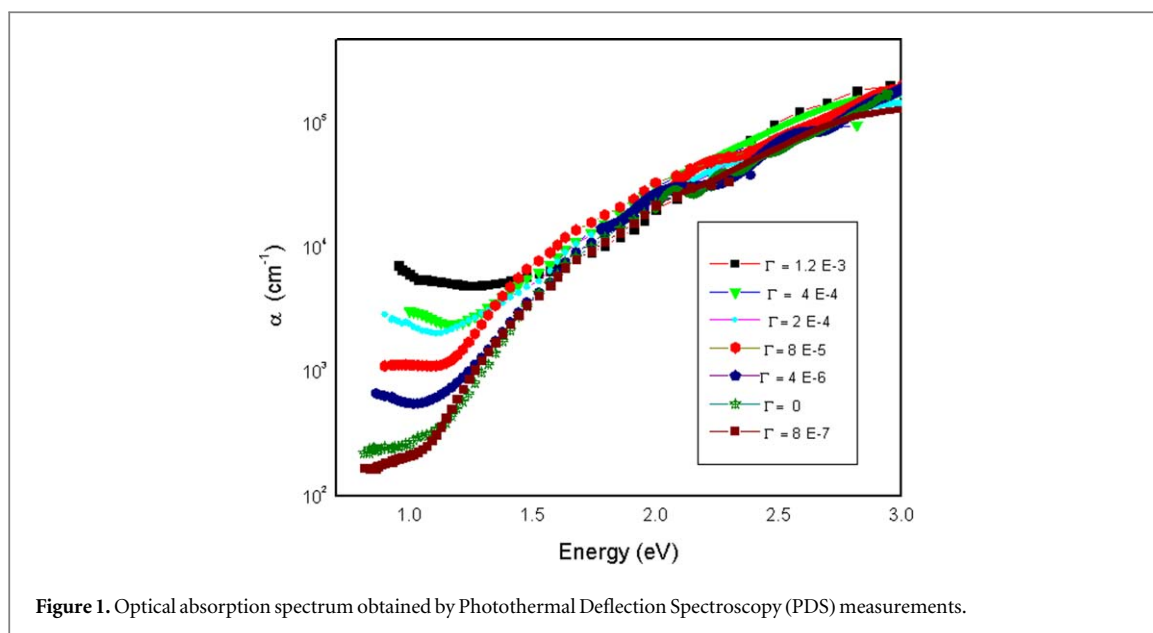


Figure 1. Optical absorption spectrum obtained by Photothermal Deflection Spectroscopy (PDS) measurements.

pixels [13, 14]. The TFTs processing give the possibility to integrate display circuit directly on the glass substrate [8, 15].

Mariem *et al* [16] presented that optical and electrical characterizations show lower defect density in slightly doped samples compared to the undoped material. Phosphorus passivation of the defects can be involved to explain this decrease of the defect density by doping. Then the increase of the electrical conductivity in slightly doped polysilicon is not due to doping effect but to the passivation of defects.

An attractive and low cost method proposed in this paper can consist in *in situ* doping polysilicon films with very low phosphorous atoms content. We present here a new technique for improving quality of polysilicon active layer of TFTs and the TFTs performance by slight phosphorus doping.

2. Material characterization

2.1. Optical characterization

Silicon films are deposited by Low Pressure Chemical Vapor Deposition (LPCVD) on glass substrate capped with a 250 nm thick SiO₂ buffer layer. Films are deposited in an amorphous state at 550 °C and 90 Pa and are *in situ* doped using silane (SiH₄) and phosphine (PH₃) gases. Doping level is controlled by adjusting the phosphine on silane ratio Γ varying from 0 (undoped film) to 1.2×10^{-3} (highly doped film). Layers are then crystallized by solid phase crystallization performed at 600 °C under vacuum. Films are characterized using Photothermal Deflection Spectroscopy (PDS) technique to measure optical absorption in the range $\alpha \leq 10^5 \text{ cm}^{-1}$. Photoluminescence measurements are also performed at 7 K using a liquid nitrogen cooled Ge detector. A krypton laser line (647 nm) with a power of 100 mW cm^{-2} is used as the excitation source. Optical absorption spectrum obtained by Photothermal Deflection Spectroscopy (PDS) measurements is reported on figure 1. In the low energy region, results highlight a minimum value of the absorption coefficient for the slightest doped layer ($\Gamma = 3.7 \times 10^{-7}$) compared to undoped ($\Gamma = 0$) and Heavily doped films ($\Gamma \geq 8 \times 10^{-6}$). Considering that defects in polysilicon are mainly located within grain boundaries, a decrease of their density can be correlated with a lower sub gap absorption coefficient. So, the trend observed can be interpreted as a decrease of the density of defects located deeply in the gap for a low phosphorus doping level. This result is the first evidence of a phosphorus passivation of defects.

The graphs between $(\alpha h\nu)^{1/2}$ and photon energy were plotted for all the samples as shown in figure 2

And results were confirmed by the calculation of the energy gap E_g for the polysilicon layers given above at different concentration of phosphine. Optical band gaps of prepared polysilicon layers doped with phosphine have been estimated by using Tauc's relation given by the following equation:

$$(\alpha h\nu)^n = B(\alpha h\nu - E_g)$$

Where h is the Planck's constant, ν is the frequency (s⁻¹) E_g is the optical energy band gap B is arbitrary constant, n is an index. For indirect band gap, the index is $n = 2$ [17].

The figure 3 shows the relation between $(\alpha h\nu)^{1/2}$ for doped and slightly doped polysilicon layers with the photonic energy ($h\nu$).

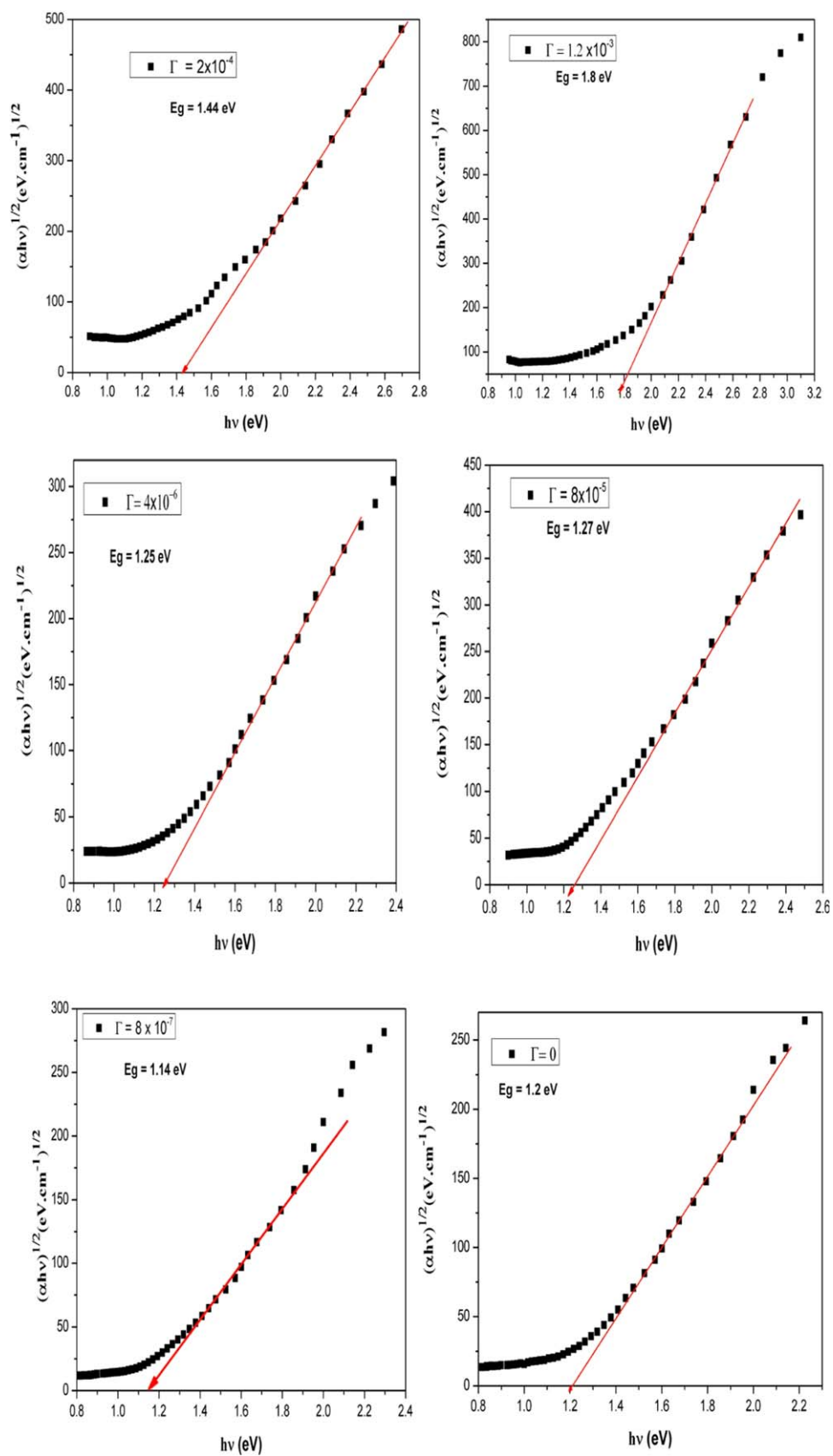


Figure 2. Tauc's plots for polycrystalline layers doped with phosphine at different concentration (from undoped to highly doped layer).

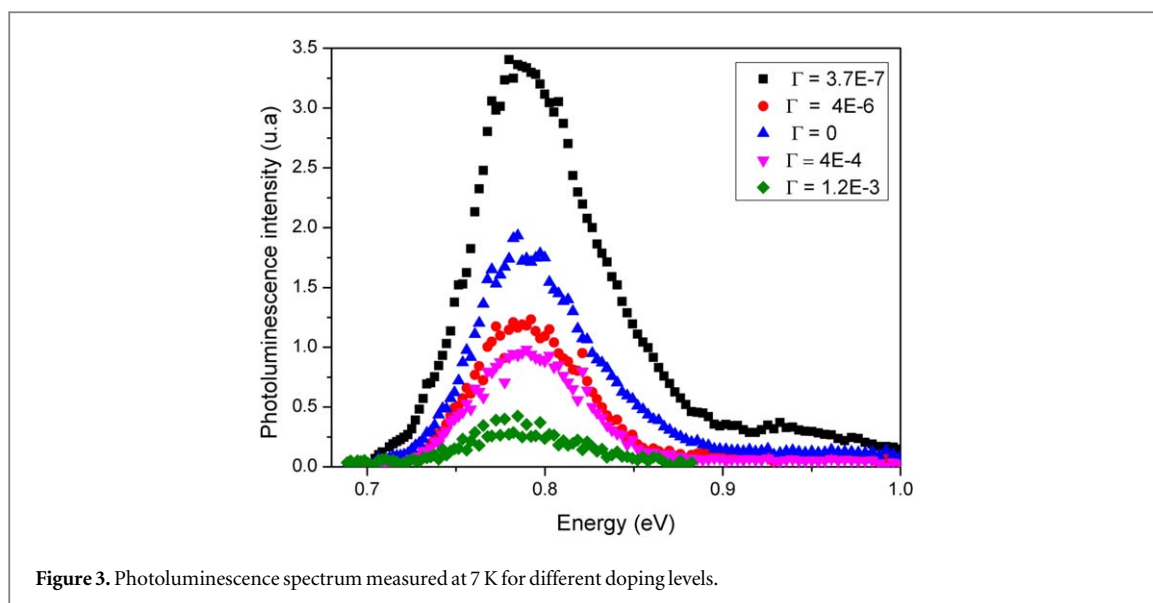


Figure 3. Photoluminescence spectrum measured at 7 K for different doping levels.

Table 1. Numerical values of the optical gaps obtained from the Tauc's plot.

$\Gamma = \varphi(\text{PH}_3)/\varphi(\text{SiH}_4)$	Band gap (eV)
1.2×10^{-3}	1.80
2×10^{-4}	1.44
8×10^{-5}	1.27
4×10^{-6}	1.25
8×10^{-7}	1.14
0	1.20

The extrapolation of the curve to the value $(\alpha hv)^{1/2} = 0$ can be used to determine the indirect band gap for the doped polysilicon samples.

The obtained results given in table 1 show a clear reduction in the E_g value for the slightest doped layer ($\Gamma = 3.7 \times 10^{-7}$) by comparison with the undoped one ($\Gamma = 0$). The value increases with heavily doped films ($\Gamma \geq 4 \times 10^{-6}$) by increasing phosphorus dopant concentration. Ganesh Lal *et al* [18] showed a decrease of band gap energy with decreasing Zn concentration and Li doping in nanoferrites. On the contrary, K Kumari *et al* [19] and Kamal *et al* [20] observed that band gap decreases as the dopant concentration atom increases, where E_g increases from 1.20 for undoped to 1.80 eV for highly doped film (1.2×10^{-3}).

Photoluminescence spectrum for samples with different phosphorus doping levels is shown on figure 3. It gives evidence of an increase of the intensity peak at 0.78 eV from undoped layer to a maximum value obtained for a slightly doped layer, and then a decrease for high level doped layers. The deconvolution of this peak on several bands led to assume it as the D band, known in single crystalline silicon and attributed to the presence of dislocations within the material [21, 22]. Dislocations within grains in solid phase crystallized polysilicon are usually observed [23]. Based on Sauer's work [24], an increase of the intensity peak at 0.78 eV can be correlated to the relaxation of dislocations within grains. So, the maximum intensity of the peak reached for the slightly doped film indicates a better quality film. This trend correlates PDS measurements highlighting the passivation effect of a low doping level in polysilicon layers and the presence of an optimum doping level value. These results constitute an array of pieces of evidence for higher quality of slightly doped polysilicon films. Characterizations performed highlighted the beneficial effect of low phosphorus doping for the passivation of defects. As a result, TFTs are fabricated with different doping levels of the active layer to confirm these previous results.

2.2. Structural analysis

The x-ray diffraction traces of the layers are given in figure 3. Three peaks were observed at 2θ values of 28.3° , 47.42° and 56.3° . These can be indexed respectively to the [111], [220] and [311].

The broadening in the XRD peak is directly related with crystallite size through Debye-Scherrer equation [25, 26].

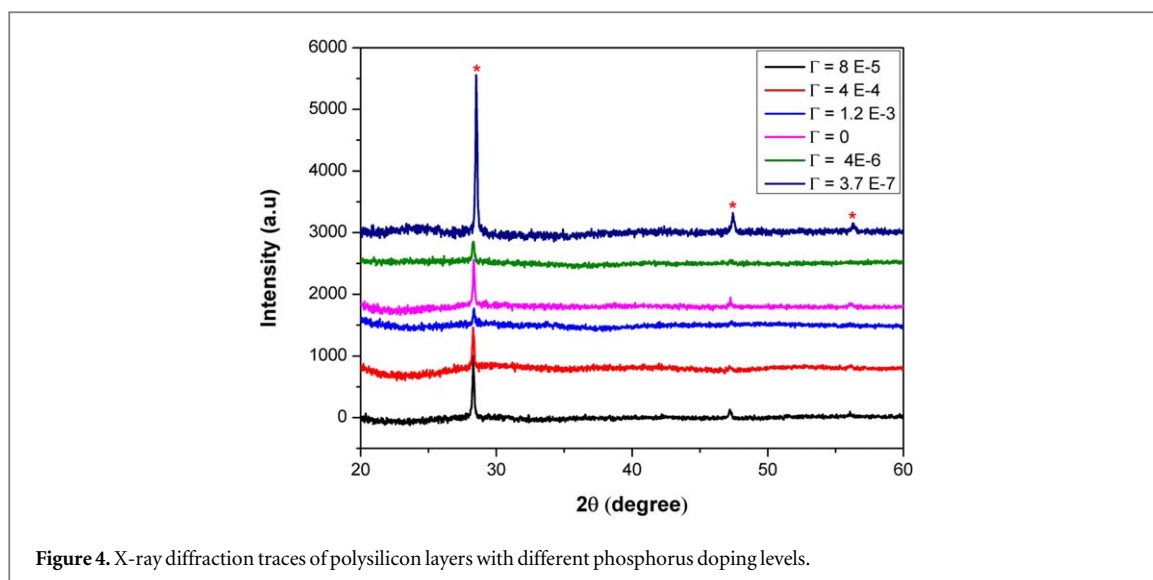


Figure 4. X-ray diffraction traces of polysilicon layers with different phosphorus doping levels.

Table 2. Details of crystallite polysilicon layers size and produced micro-strain for samples .

$\Gamma = \varphi (PH_3) / \varphi (SiH_4)$	Crystallite size (D) (nm)	Micro-strain (ϵ) ($\times 10^{-3}$)
4 E-4	45.7	3.20
8 E-5	43.2	3.10
4E-6	36.0	3.08
0	35.8	3
3.7E-7	33.4	2.8

$$D = \frac{k\lambda}{\beta \cos \theta} \quad (1)$$

Where k is a Scherrer constant, λ is the wavelength of radiation used in according of XRD, β is the Full-Width at HalfMaxima (FWHM) of particular XRD peak and θ is the angular position of the particular XRD peak.

The contributions of crystallite size and strain are the properties of materials, which can be determined using OriginLab and excel sheet to find the following parameters from XRD data. The average crystallite sizes of these samples were estimated from the line width of the most intense and well resolved diffraction peaks using Scherrer formula. The calculated value of crystallite size and micro-strain for samples was given in table 2. The slightly doped sample 3.7E-7 showed the lowest value of the crystallite size and the micro-strain by comparison with the undoped and highly doped samples. It is noted that the micro-strain value of samples remains almost constant and no remarkable change was noticed.

3. Devices

TFTs are fabricated through a four mask process at low temperature ($<600^\circ\text{C}$). First, a 250 nm thick SiO_2 buffer layer is deposited on glass substrate. Then, a 450 nm thick LPCVD amorphous silicon layer is deposited at 550°C and 90 Pa with two different stacked regions: the lower region (300 nm thick) is slightly doped (or undoped) and the upper one (150 nm thick) is heavily phosphorus doped. Solid phase crystallization is then performed at 600°C during 8 h. The heavily *in situ* doped layer is plasma etched to define the channel, source and drain regions. Then, a 70 nm thick silicon dioxide film is deposited by APCVD technique to be used as a gate dielectric layer. Source and drain contacts are opened by wet etching through gate insulator. Finally, 500 nm aluminium thick layer is thermally evaporated to form source, drain and gate contacts. Final structure is reported on figure 3.

The transfer characteristics of N-type transistors with different phosphorus doping levels of the active layer are presented on figure 4. These characteristics are measured at room temperature using a HP 4155 B programmable parameter analyzer.

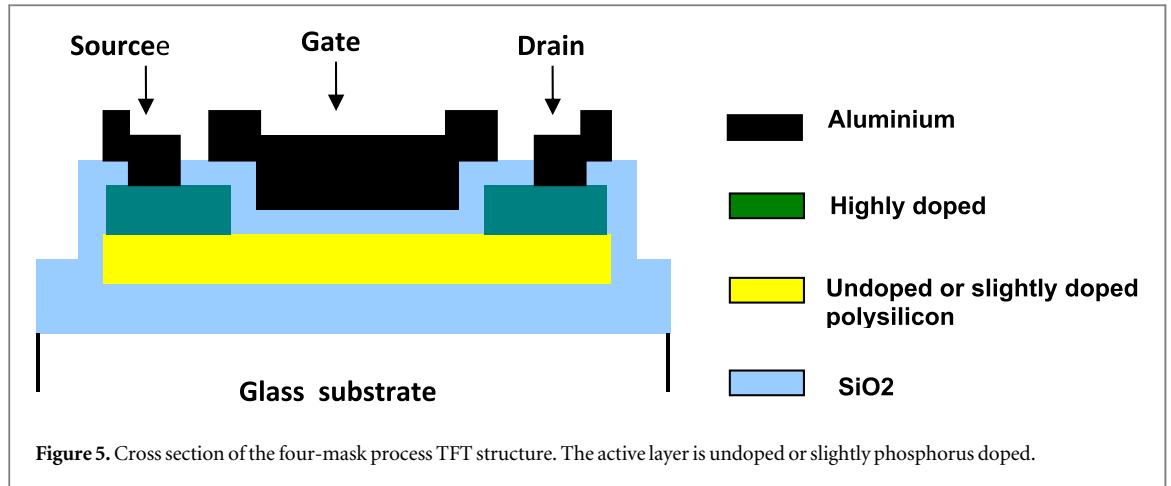


Table 3. Main electric parameters of the TFTs $\frac{I_{on}}{I_{off}}$ ratio, field effect mobility μ , threshold voltage V_{th} and subthreshold slope S for N-type TFTs fabricated with different doping levels Γ .

$\Gamma = \varphi(PH_3)/\varphi(SiH_4)$	0	3.7×10^{-7}	8×10^{-7}	2.6×10^{-6}
I_{on}/I_{off}	7.5×10^5	6.8×10^5	1.7×10^5	2×10^4
μ (cm ² /V.s)	128	162	122	120
V_{th} (V)	1.5	1.2	2	1.3
S (V/dec)	0.99	0.98	1.23	2.2

Table 4. Density of trap states within grain boundaries according to the Levinson's model.

$\Gamma = \varphi(PH_3)/\varphi(SiH_4)$	0	3.7×10^{-7}	8×10^{-7}	2.6×10^{-6}
N_T (cm ⁻² .eV ⁻¹)	$2-4 \times 10^{18}$	$1-2 \times 10^{18}$	5×10^{18}	7×10^{18}

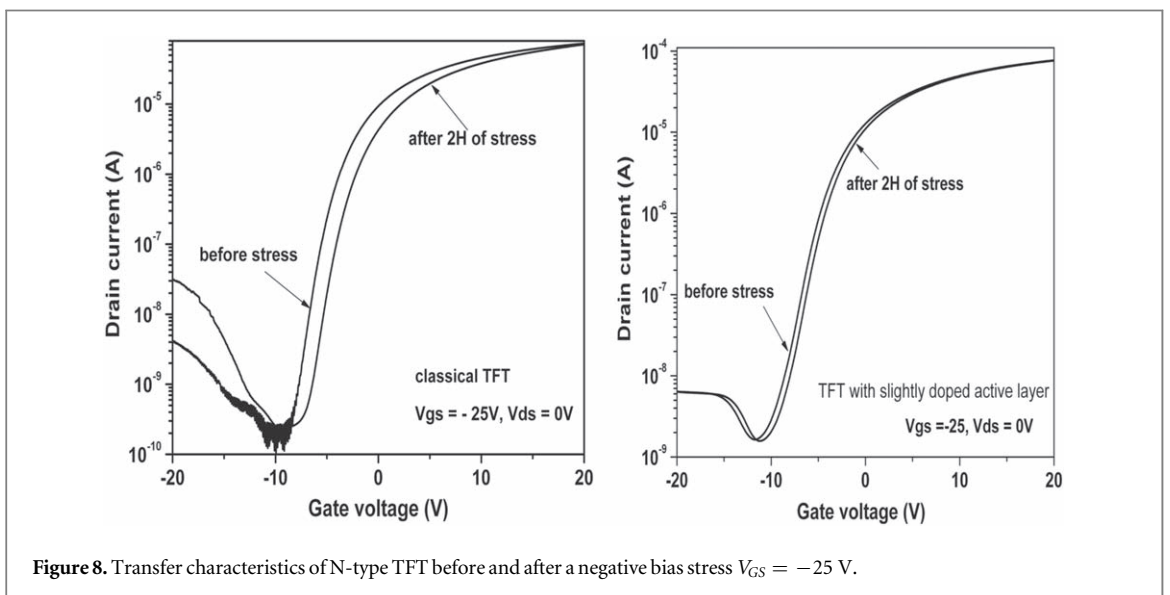
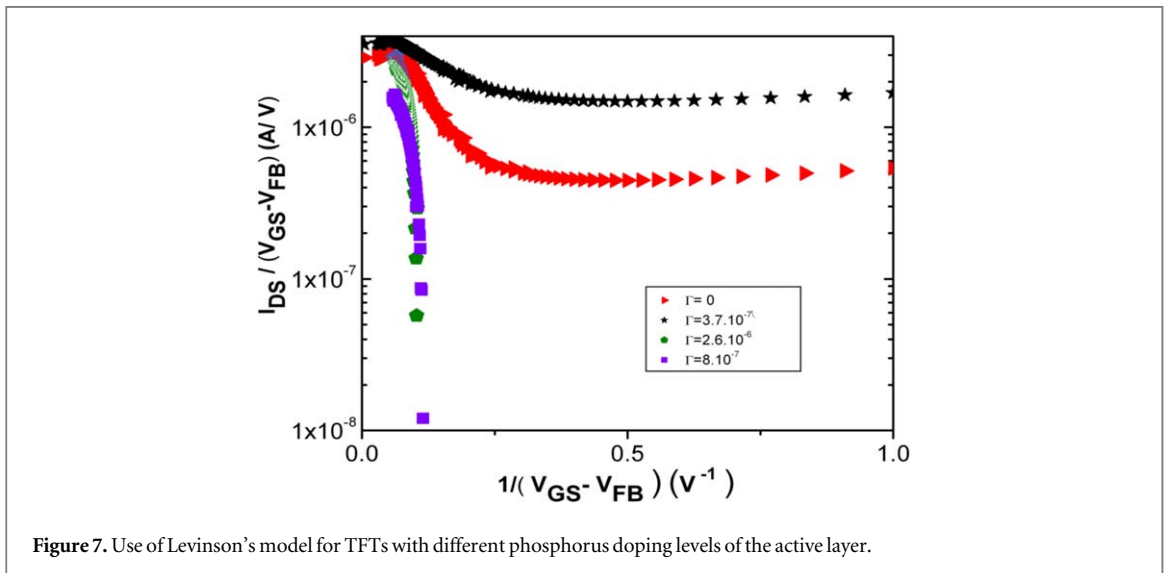
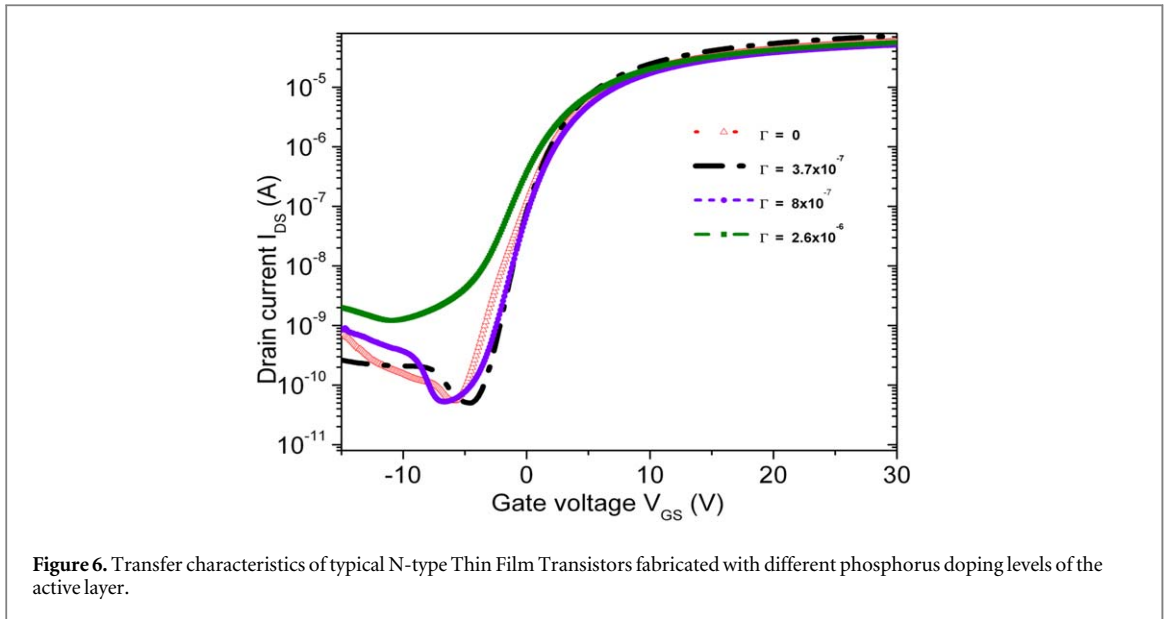
The main parameters extracted from these curves are reported in table 3. As we can see from table 3, the use of a slightly doped polysilicon film as active layer induces very significant improvements in the TFTs performances compared to classical TFTs made with an undoped active layer. Indeed, field effect mobility μ exhibits a gain about 30% and a lower threshold voltage value is also obtained. From undoped to slightest doped layer, I_{on}/I_{off} ratio is quasi constant. With doping level increasing, polysilicon film conductivity increases inducing an efficient doping role for phosphorous atoms. As a consequence, the I_{on}/I_{off} ratio decreases. Using this simple and low cost method consisting in slightly doping polysilicon active layer, a very high mobility value can be obtained; reaching then the usual value obtained with LTPS (more expensive laser crystallization) TFTs.

The high level mobility values obtained are due to the present process where both the active layer and the doped layer that constitutes the source and drain regions are deposited in the same run, removing the interface between active layer and source and drain regions [27]. Using Levinson's model [14], the drain current of the TFT can be expressed by the following equation (1):

$$I_{DS} = \frac{W}{L} \mu_0 V_{DS} C_{ox} (V_{GS} - V_{th}) \exp\left(-\frac{q^3 N_T^2 t}{8 \varepsilon K_B T C_{ox} (V_{GS} - V_{th})}\right) \quad (2)$$

Where W and L are width and length of the channel respectively, C_{ox} the surface oxide capacitance, e the channel thickness. This relation is valid when the electron concentration in the channel is greater than a critical concentration $N^* = N_T L_G$ where N_T is the density of traps within grain boundaries and L_G the length of the grains. So, using a semi-logarithmic plot of the $I_{DS}/(V_{GS} - V_{th})$ versus $1/(V_{GS} - V_{th})$ we can obtain a linear function which slope is proportional to N_T . Results are shown on figure 5.

V_{th} is defined at the minimum of the transfer characteristics. For each TFT, we can observe a linear behavior corresponding to the Levinson's model validity. As shown on figure 7, the linear region is more extended for TFTs with the slightest doped active layer and the slope is the lowest indicating a better material quality. Calculated values of the density of traps within grain boundaries are reported on table 4. Stress effect on the two types of TFTs (with an undoped active layer or the slightest phosphorus doped layer) was investigated.



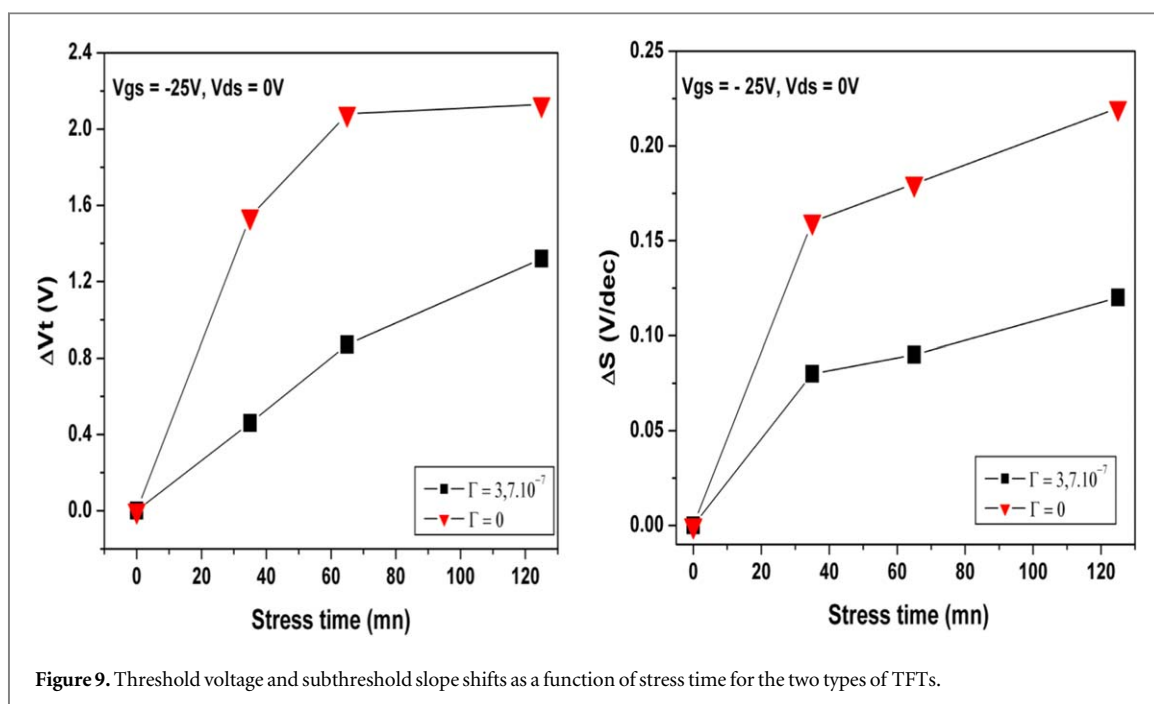


Figure 9. Threshold voltage and subthreshold slope shifts as a function of stress time for the two types of TFTs.

Figure 6 shows the transfer characteristics measured for a constant drain voltage $V_{DS} = 1\text{ V}$ before and after applying a negative stress bias $V_{GS} = -25\text{ V}$ during 2 h. The source and drain regions are short circuited during the gate bias stress in order to avoid any hot carrier effect. This stress induces a shift of the transfer characteristics for both types of TFTs. The gate bias stress may result in the state creation in the band gap of the channel material and at the $Si - SiO_2$ interface, which is a disordered region [28]. As shown on figure 8, gate bias effect is strongly reduced when the active layer is slightly phosphorus doped.

This trend may be explained by the higher polysilicon film quality obtained with slight phosphorous content. Better stability under stress is confirmed by the lower shift of the threshold voltage and the subthreshold slope for doped active layer TFT as shown on figure 9. This stress effect is another piece of evidence of the beneficial effect of a weak phosphorus doping function of stress time for the two types of TFTs.

4. Conclusion

Effects of weak phosphorus doping in polysilicon layers were investigated. PDS and photoluminescence measurements highlighted the phosphorus passivation of defects giving evidence of an optimum doping level to obtain high quality polycrystalline silicon films. It is observed a clear reduction in the E_g value for the slightest doped layer ($\Gamma = 3.7 \times 10^{-7}$) by comparison with the undoped one ($\Gamma = 0$). Two types of polysilicon TFTs were fabricated, with an undoped active layer and with a slightly phosphorus doped one. Electrical characterizations highlighted the beneficial effect of *in situ* doping the active layer. Optimal doping level induced high mobility ($\geq 160\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$) and a low threshold value. Stability under stress effect was also enhanced due to the higher quality of the *in situ* doped material. These enhancements gave evidence that control of weak phosphorus doping in polysilicon films is a new simple way to improve polysilicon based devices.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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