

Random telegraph signals in nanoscale vertical junctionless transistor with gate-all-around

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The role of a single defect on the electrical performance of transistors is unclear for transistors at nanometric dimensions. This role must be understood in order to improve the design and fabrication process of nanoscale transistors. Herein, we detected a single defect by a noise analysis approach on 18-nm-long gate junctionless (JL) vertical gate-all-around nanowire (VGAANW) transistors. Random telegraph signals (RTS) are reported to have a relative amplitude as high as 60%. We studied these RTS to assess the capacitive network in such nanoscale devices, providing routes to avoid large noise in the further downscaling of VGAANW and to exploit the high charge sensitivity for sensing applications. Defect density comparisons between JL and classic accumulation-mode transistors offered the opportunity to discuss a noise model developed when transistors were of several micrometers in size, questioning the significance of a defect density of less than one defect per device at the nanoscale.

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As we are reaching scales where one-dimensional transport and ballistic behaviors can be observed¹⁻⁷, the transport mechanisms at the nanoscale need to be better understood for their applications in single-electron sensors⁸⁻¹¹, quantum computing^{12,13}, and the next generations of transistors^{14,15}. At the nanoscale, the continuous concepts of dopant concentrations and trap densities are challenged by their discrete occurrence, increasing variability from device to device, and uncertain transport mechanism at this scale. Whereas the study of noise in nanoscale devices gives access to a lot more information than just direct current (DC) measurements, there are several candidate models for noise in nanodevices. One model was developed at a time when device dimensions were on the order of micrometers and considers a correlated number and mobility fluctuation (known as unified number fluctuation), corresponding to the trapping/detrapping of charges from the channel in interface defects, affecting the overall mobility of charge¹⁶⁻¹⁸. Another model has been recently proposed^{19,20} from the analysis of Coulomb repulsion between neighboring traps in nanoscale devices, an effect that does not involve mobility. This model is based on the same number fluctuation postulate but with an effective charge (q^*) of the involved traps that depends on the carrier's density in the channel. Very interestingly, both models adapted here for the gate-all-around architecture are very similar mathematically (Equations (1) and (2), respectively).

$$\frac{S_I}{g_m^2} = \frac{q^2 N_{ot}}{C_g^2 2RL_g} \left(1 - \frac{\alpha_{sc}\mu}{q} C_g (V_g - V_{th}) \right)^2 \frac{1}{f} \quad (1)$$

$$\frac{S_I}{g_m^2} = \frac{q^2 N_{ot}}{C_g^2 2RL_g} \left(\frac{2\epsilon_{SiO_2}}{\epsilon_{SiO_2} + \epsilon_{Si}} \right)^2 \left(1 - \frac{qt_{acc}}{2k_B T \epsilon_0 (\epsilon_{SiO_2} + \epsilon_{Si})} C_g (V_g - V_{th}) \right)^2 \frac{1}{f} \quad (2)$$

where S_I is the current power spectrum density, g_m is the transconductance, q is the elementary charge, N_{ot} is the density of traps, C_g is the gate capacitance, R is the half-width of the transistor (or radius for nanowire architectures), α_{sc} is the scattering parameter, V_g is the gate voltage, V_{th} is the threshold voltage, L_g is the length of the gate, ϵ_{SiO_2} and ϵ_{Si} are the permittivities of SiO_2 and Si, respectively, t_{acc} is the thickness of the accumulation layer, T is the temperature, and k_B is the Boltzmann constant. See Figure S1 for the comparison of both models with standard parameters.

Junctionless (JL) transistors consist of uniformly and highly doped nanowires, which are sufficiently narrow to be entirely depleted by a gate. In practice, it has been demonstrated that these gated resistors have the full functionality of complementary metal-oxide semiconductor transistors^{21,22}. Several reports have been published on the JL configuration that effectively address short channel issues and the difficulty of fabricating highly doped p-n junctions at the nanoscale^{21–27}. This design can be efficiently combined with a gate-all-around nanowire architecture, which has been actively explored with promising perspectives on integration and downscaling, especially for the vertical approach^{14,15,21,22,24,27–30}. Noise studies widely acknowledge their superiority compared to classic accumulation-mode transistors, mostly thanks to their core-conduction mechanism^{21–23,25–27,29}.

In this paper, we use transistors with 18 nm-long gates in an all-around configuration, allowing fine tuning of the aperture of the channel. We show how the observation and analysis of a random telegraph signal (RTS) resulting from trapping/detrapping of a single charge and low frequency noise can bring insights to noise models. In addition, we compare JL vertical gate all-around nanowire transistors (VGAANWs) with equivalent low-doping-level devices (commonly called Schottky barrier accumulation-mode transistors (SB)) made with the same fabrication

process to discuss the models and their implications on the density of the traps and the charge transport mechanism.

The devices were fabricated following the main process steps described in ref¹⁴. However, in this new generation, the fabrication of the symmetrical source and drain silicide contacts have been specifically optimized by introducing a novel lift-off-free approach, leading to an improvement of the access resistance³¹. The schematics of the device shown in Figure 1a. Briefly, the devices consist of a monocrystalline array with ~ 138 -nm-long Si nanowires vertically arranged with top and bottom contact with PtSi, a 60-nm SiO_x layer at the spacers on both sides of a 18–19-nm-long Cr gate, and a 4–5-nm-thick SiO₂ gate dioxide layer around the nanowires. The silicon for the JL devices was heavily p-doped ($N_p = 3 \times 10^{19}$ at/cm³), and the silicon for the SB devices was undoped ($N_p = 1.8 \times 10^{15}$ at/cm³). The number of nanowires in parallel (n_{NWs}) varied from 1 to 36, and their diameter varied from 16 nm to 43 nm.

The measurement setup is described in the supplementary information (Figure S2). The drain current (I_{ds}) and transconductance (g_m) were measured for all devices versus V_g for a drain-source voltage (V_{ds}) of -0.1 V or -1 V. It was also measured versus V_{ds} , with V_g in the subthreshold and saturation regimes. The characteristics of four devices are shown in Figure 1, with a summary of the measured I_{ON}/I_{OFF} values for all measured devices shown in Figure S3 (8 JL, 7 SB). The maximum current ranged from 1 nA to 1 μ A per nanowire for these devices. Wider JL devices showed a larger I_{OFF} current as V_{ds} increased, which was not the case for a smaller radius or SB devices (Figure S4). By default, the JL devices had a fully opened channel that the gate must deplete entirely to turn off the device. This becomes more difficult as the diameter increases³². As for smaller radii, they showed a lower I_{ON} , though more dispersity was observed, which was

expected with scaling down. The mobility was extracted using Equation (3) in the saturation region for JL devices and Equation (4) in the subthreshold regime for SB devices, with $1 < \mu_{JL,sat} < 50$ cm²/V and $1 < \mu_{SB,sub} < 75$ cm²/V, respectively.

$$\mu_{JL,sat} = \frac{IL}{qN_p\pi R^2V_{ds}} \quad (3)$$

$$\mu_{SB,sub} = \frac{g_m L_g}{2Rn_{NWs}C_gV_{ds}} \quad (4)$$

where L is the length of the nanowire and N_p is the dopant concentration.

For 16-nm-diameter JL devices, I_{ds} tended to saturate and g_m decreased sharply after reaching saturation, as expected for extremely scaled transistor devices for which access resistances are not negligible. This behavior is representative of 16-nm-diameter JL devices (4/4 measured devices of this diameter) and was observed for one SB device (43-nm diameter, $n_{NWs} = 1$). Overall, the performances were improved compared to a previous study on similar devices, in which smaller currents per nanowire were measured, attributed to the access to the contacts²⁹.

Two JL devices with diameters of 16 nm ($n_{NWs} = 4$ and 25, respectively) showed a clear RTS, thus providing a good opportunity to assess information on the capacitive network and electron transport in these nanoscale devices. A time trace of the 4-nanowire one and its amplitude evolution versus V_{ds} and V_g are shown in Figure 2. The relative amplitude was as high as 15% of the overall current (I_{ds} vs. V_g in the inset of Figure 3a), i.e., as high as 60% of the current flowing in the nanowire holding the defect. This RTS amplitude was extremely large when compared to

the RTS usually obtained in nanotransistors^{33,34}. The evolution of the time spent in the up state (τ_{up}) or down state (τ_{down}) showed no correlation with V_g (Figure S5) but demonstrated a clear Fermi distribution with varying V_{ds} (Figure 2b). This finding suggests that a defect is loosely coupled to the gate, i.e., located in the spacers. The amplitude of ΔI_{RTS} varied in both cases but could be well explained versus V_g by the relative series resistance of the spacers and opened channel $\eta = R_s/R_{tot}$, as shown in Figure 2c, with $R_{tot} = V_{ds}/I_{ds}$ and $R_s = \max(R_{tot})$ (measured at the saturation) obtained from DC characteristics.

Considering the Fermi distribution behavior observed from the evolution of τ_{up} and τ_{down} versus V_{ds} , we proposed a thermally activated trap occupancy with the Fermi level being mainly tuned by V_{ds} :

$$\Delta I_{RTS} = \eta \frac{q^* g_m}{C_g^*} \frac{1}{1 + \exp\left(q \frac{V_{trap} - \beta V_{ds}}{k_B T}\right)} \quad (5)$$

where q^* is the effective charge of the trap, g_m is the transconductance, C_g^* is the effective capacitance felt by the trap, $q \times V_{trap}$ is the activation energy of the trap, β is a parameter that takes into account the position of the trap relative to the drain contact, k_B is the Boltzmann constant, and T is the temperature. Being in the saturation regime, we considered $\eta \approx 1$ and constant (i.e., I_{ds} vs. V_{ds} is linear). On a first approximation, q^* could be assumed to be equal to the elementary charge, and g_m was estimated using a linear regression of I_{ds} vs. V_g data ($g_m(V_{ds}) \approx -V_{ds} \times 1.42 \mu S$). Of note, the parameter β was found to be very close to 1 for JL devices in which RTSs were observed, which corresponds to traps located close to the drain side of the transistor. It is reasonable to assume that this will often be the case as a sweep of V_{ds} barely impacts the energy level of the trap

if it is located on the source side, whereas a sweep of V_{ds} scans a much larger amplitude of energy levels if the trap is located closer to the drain.

If we considered $C_g^* = C_g$ in Equation (5), as usually assumed for larger devices, it led to a variation of the current from the trap corresponding to more than 40 elementary charges (Figure 2b). On the other hand, taking $C_g^* \approx C_g/15$ fit well with the RTS measurement. This, in addition to $\eta = 1$ and $\beta \approx 1$, suggests that the trap is located in the spacer, with a small coupling to the gate capacitance. This analysis on C_g is consistent with previous estimations of the capacitive network on similar structures¹⁴. This work emphasizes the importance of the capacitive network to explain the large relative RTS observed. The fact that previous studies did not report such large RTSs due to a trap in the oxide layer of JL devices could be due to Schottky resistances that are too high, the use of another implementation than VGAANWs (leading to higher C_g^*), larger nanowire diameters, or the use of large numbers of nanowires in parallel.^{14,23–27,35} Other studies already have demonstrated a very high RTS amplitude in nanowires due to the quantum confinement effect for smaller devices²⁸, random dopant fluctuations, and traps positioned along the corresponding percolation path, but the effects were observed at a low temperature or for a RTS occurring in the subthreshold region^{6,33,35–37}. Considering that the RTS was observed in the saturation region and that the experiments were performed at room temperature, the percolation path explanation seems unlikely here.

The fact that a RTS was observed for JL devices only with small diameters can be explained by the larger relative resistance of the spacers compared to that of devices with larger diameters, as it scales directly with the section of the nanowires (Equation S4). Another way to look at it is to estimate the apparent radius of the trap (r_{trap}). Adapting work by Ohata *et al.*³⁸ to our geometries

gave an apparent radius of $r_{trap} \approx 2$ nm (Figure 2c). This could explain why large RTSs are observed only for JL devices with a small diameter, as the trap occupies a relatively larger portion of the whole conductive section compared to that of larger JL devices. In the following section, we analyze the current power spectra.

Drain current power spectrum densities (S_I) were measured versus V_{ds} acquired at V_g in the subthreshold and the saturation regions as well as versus V_g at $V_{ds} = -0.1$ V and $V_{ds} = -1$ V (examples in Figure S6). An example of S_I measured at different V_g values ($V_{ds} = -0.1$ V) for a JL device ($n_{NWS} = 4, 16$ nm in diameter) is shown in Figure 3a along with the corresponding I_{ds} and g_m measurements. The contribution of RTS to S_I is visible by the emergence of a shoulder at around 20 Hz. The spectra were fit using a $1/f^\alpha$ background contribution superimposed on Machlup's mathematical description of RTS³⁹. The Hooge constants (α_H) were estimated in the saturation regime, where the channel is fully opened and where the whole length of the transistors was considered for JL devices. Values of α_H were obtained ($2 \cdot 10^{-4} < \alpha_H < 0.4$) in the range of expectations using Equation (6)⁴⁰.

$$\alpha_H = \frac{S_I f N_{carriers}}{I^2} \quad (6)$$

where $N_{carriers} = L\pi R^2 C_g n_{NWS} N_p$ for JL and $N_{carriers} = L_g \pi R^2 C_g n_{NWS} (V_g - V_{th})/q$ for SB.

Previous work on vertical nanowires has demonstrated an exponential increase of S_I/I^2 with V_{ds} for Schottky barrier contact noise⁴¹. For all devices measured herein, the current-normalized noise S_I/I^2 measured versus V_{ds} remained constant (see Figure S7), which confirms the technological improvements achieved on the contacts of these devices³¹. This finding suggests that the Schottky

contact is no longer the limiting factor in noise measurements, unlike those previously reported for similar structures and carbon nanowires^{4,42}. The improvement of the fabrication of such nanoscale devices offers an opportunity to assess the intrinsic carrier transport properties in a nanotransistor.

The two types of devices with different doping levels but manufactured with the same technology allowed a fair comparative analysis of the defect densities. To this end, the defect density N_{ot} was measured near V_{th} , where S_I/g_m^2 is nearly constant (Figure 3b), a marker of number fluctuation-induced noise²⁷, and where the effective capacitance can still reasonably be considered equal to C_g . This regime corresponds to a fluctuation of the threshold voltage rather than a fluctuation of the mobility. Note that the possibility of a dielectric polarization noise⁸ (that leads to a thermal $1/f$ noise in the absence of defects) is excluded because the estimated dielectric loss would be orders of magnitude too large. Therefore, a simplified version of Equation (1) was considered, Equation (7)^{16,18}, to estimate the N_{ot} at $f = 10$ Hz. The results are summarized in Figure 3c–d.

$$N_{ot} = \frac{S_i}{g_m^2} \frac{f C_g^2 2\pi R L^* n_{NWS}}{q^2} \quad (7)$$

The N_{ot} values were approximately $2 \times 10^{11} \text{ cm}^{-2}$ for JL devices and $2 \times 10^{10} \text{ cm}^{-2}$ for SB devices. Although a non-negligible device-to-device fluctuation was observed on these values, both types of devices were fabricated using the same equipment and techniques and should thus have very similar defect densities. Considering the number of defects per nanowire, there was less than one defect per nanowire (Figure 3d). However, considering an effective charge q^* (Equation (2)), N_{ot} became more similar for JL and SB devices, and the number of defects per nanowire

became greater than one. Therefore, these results suggest that Equation (2) is more appropriate than Equation (1) for nanotransistors.

In conclusion, we observed an unprecedentedly high RTS on JL VGAANWs, which was allowed thanks to low Schottky access resistances. The study of this RTS revealed the importance of the capacitive network, C_g^* , for defects that are not located under the gate. Indeed, if traps are uniformly distributed along the length of the nanowire, as the gate tends to be much shorter than the total length of the device, traps will statistically have a greater chance to be controlled by C_g^* than by C_g . Importantly, keeping a relatively large C_g^* to decrease ΔI_{RTS} is contradictory with the requirements for the general demands of the higher switching speed and power efficiency obtained by increasing C_g/C_g^* in transistors. If we consider the expression of q^* , the use of high-K materials for the gate could have a favorable impact on the RTS amplitude, even with the expected increase in the number of defects. With the general trend in downscaling and the defect densities currently obtained, the tradeoff still makes the high permittivity route promising to decrease the impact of traps in nanoscale devices. A recent publication using such a configuration has reported low noise and no RTSs for similar devices²⁷. The comparison of defect densities obtained on JL and SB devices suggest that the effective charge (q^*) model may be the most appropriate to describe the defects in nanoscale devices. Several publications have continued to use the unified number fluctuation model for nanoscale devices, but one can wonder about the physical meaning of such a model when the dimensions of devices get so small that they sometimes have less than one defect per device, on average (e.g., $\sim 0.04/\text{device}$ ²⁵, $0.03\text{--}2/\text{device}$ ⁴², or $0.002/\text{device}$ ^{27,43}). We believe that this study of RTS noise on JL VGAANW devices provides critical information toward a better understanding of nanoscale charge transport and opens new perspectives for high-sensitivity

sensors^{20,44,45} as the charge noise and charge sensitivity are correlated like in quantum computing, where $1/f$ noise is an important cause of decoherence^{12,13}.

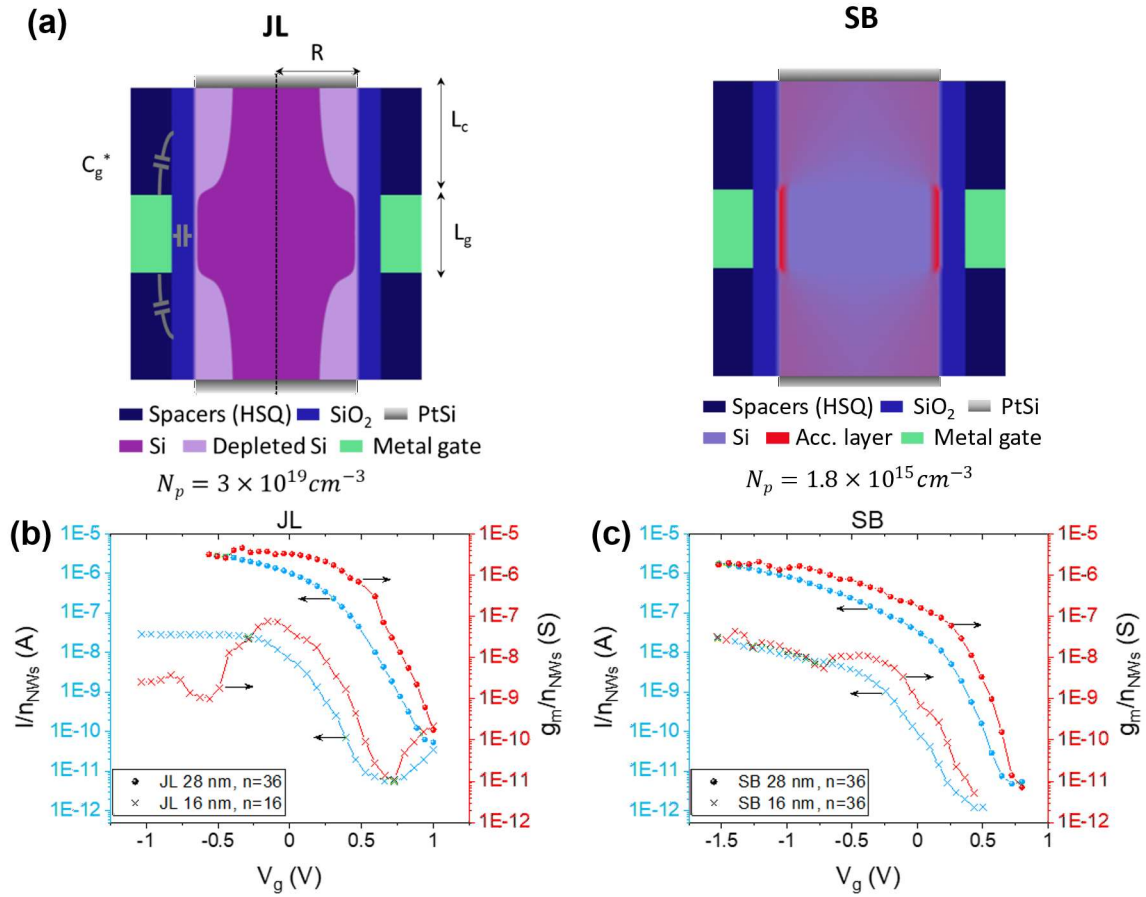


Figure 1. (a) Schematics of the JL and SB structures. (b) I_{ds} vs. V_g and g_m vs. V_g curves of two JL devices and (c) two SB devices. The diameters and numbers of the nanowires are indicated in the figures.

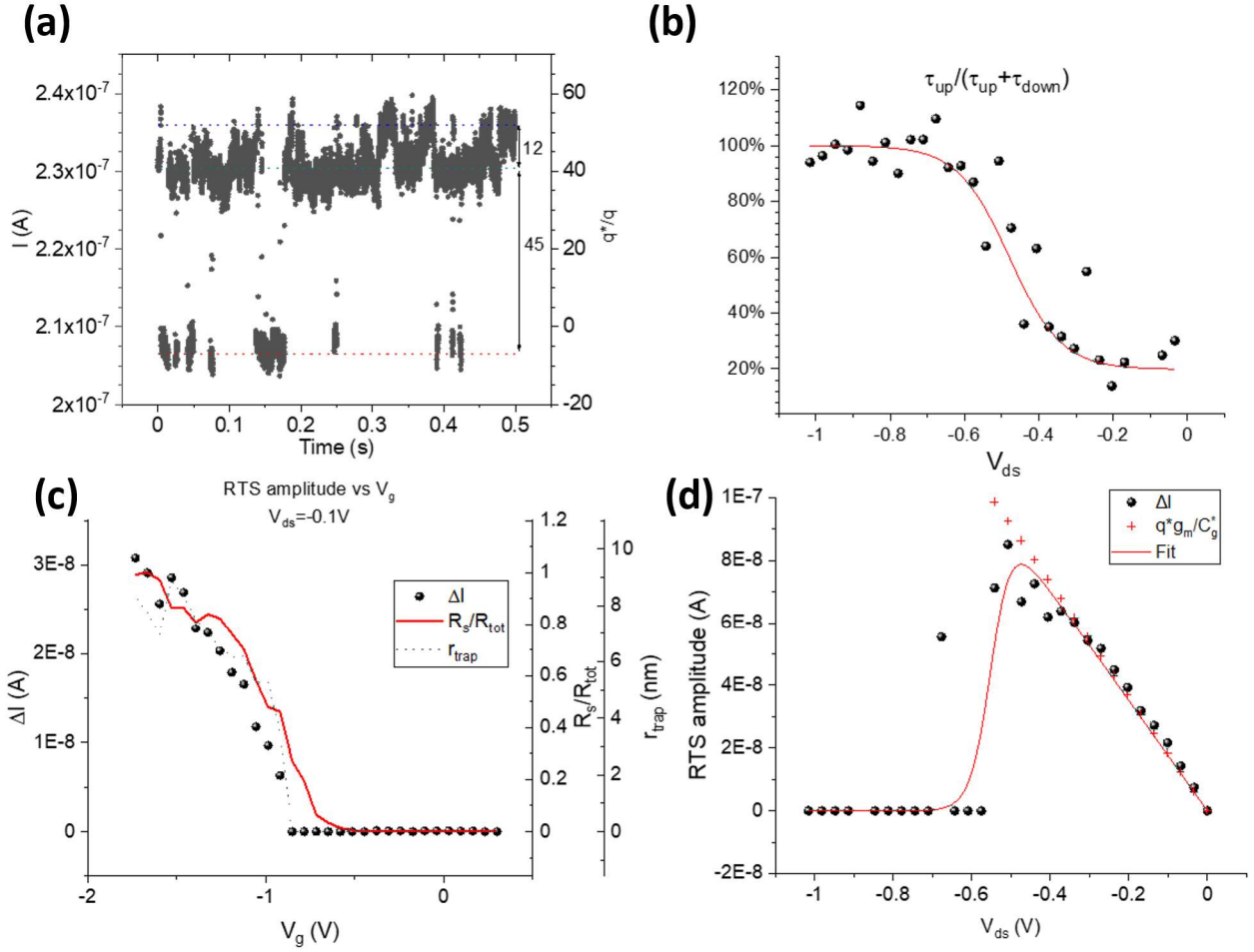


Figure 2 (a) RTS vs. time trace of the corresponding device at $V_g = -1.39$ V and $V_{ds} = -0.1$ V. q^*/q is estimated with C_g and Equation (5). (b) Evolution of $\tau_{up}/(\tau_{up} + \tau_{down})$ vs. V_{ds} at $V_g = -1.2$ V. The solid red line is a Fermi distribution fit. (c) Evolution of ΔI_{RTS} for different V_g values plotted along an equivalent trap radius (r_{trap}) and measured with a relative spacer resistance of R_s/R_{tot} . (d) Evolution of ΔI_{RTS} for different V_{ds} values ($V_g = -1.2$ V). The solid line is fit from Equation (5).

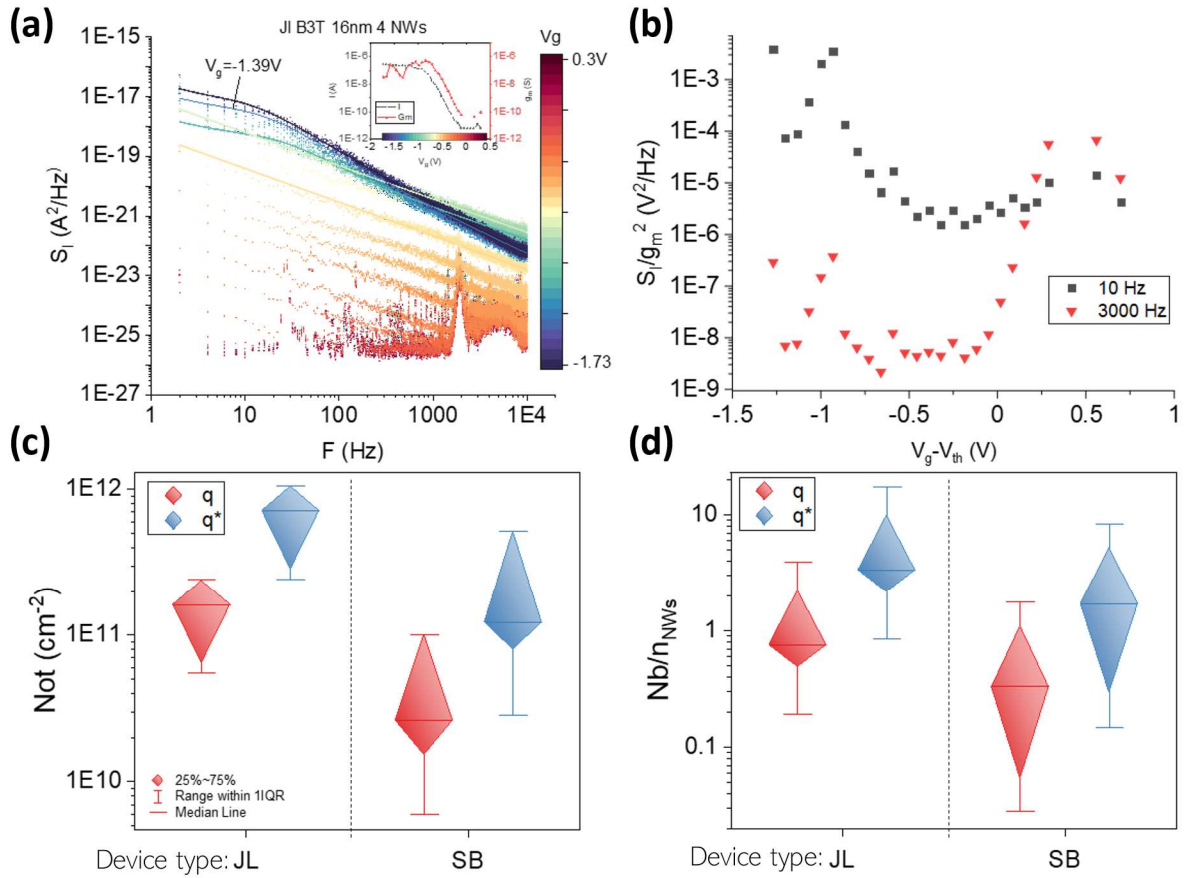


Figure 3. (a) Power spectrum densities of a JL device (16 nm, $n_{NWs}=16$) measured at different V_g values ($V_{ds} = -0.1$ V). I_{ds} vs. V_g and g_m vs. V_g curves of the device are shown in the inset. The solid lines are fits with the $1/f^\alpha$ law + Machlup's description of RTS³⁹. (b) S_I/g_m^2 of the same device measured in (a). N_{ot} measurements were performed at $V_g - V_{th} = -0.2$ V. (c) The density of defects (N_{ot}) and (d) the number of defects per nanowire (Nb/n_{NWs}) measured on JL and SB devices using q (red) or the effective charge of the traps q^* (blue) for the estimation. The diameters and n_{NWs} of the devices included in these results are available in Table S1. For JL devices, q^* is estimated with $t_{acc} = 0$; and for SB devices, q^* is estimated with $t_{acc} = 1$ nm.

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