Circuit partitioning with path delay-based minimization

Julien Rodriguez, François Pellegrini, Galea François, Lilia Zaourar

HAL Id: hal-03604540
https://hal.science/hal-03604540

Submitted on 10 Mar 2022

Circuit partitioning with path delay-based minimization

Julien, Rodriguez
Université Paris-Saclay, CEA, List, F-91120, Palaiseau, France
`julien.rodriguez@cea.fr`

François, Galea
Université Paris-Saclay, CEA, List, F-91120, Palaiseau, France
`francois.galea@cea.fr`

François, Pellegrini
Université de Bordeaux, INRIA
`francois.pellegrini@u-bordeaux.fr`

Lilia, Zaourar
Université Paris-Saclay, CEA, List, F-91120, Palaiseau, France
`lilia.zaourar@cea.fr`

March 2021

1   Abstract

Hypergraph partitioning has been used in several areas including circuit partitioning for VLSI design since the 1970s. The process of evaluating and verifying a System on a Chip (SoC) involves using Field-Programmable-Gate-Arrays (FPGAs). Nowadays, the increasing size of Integer Circuits (IC) requires partitioning them in several sub-circuits. Each one is then mapped onto a multi-FPGA platform while respecting some constraints. This work focuses on the minimization of the maximum path delay.

There are several tools that allow hypergraph partitioning, like hMETIS, PaToH and KaHyPar. These solvers minimize a "min-cut" objective function based on individual penalties for each of the cut hyperedges. The minimization problems for "min-cut" are NP-hard.

Even though this function tries to minimize the number of hyperedges (nets) between parts (vertex set), it does not solve the path delay minimization. There exist some previous works that deal with the timing constraint with good results (40

In this paper, we devise a mathematical model for the problem of IC partitioning with path-delay-based minimization that takes into account various

constraints. We propose a way to derive the classical multilevel approach for graph/hypergraph min-cut methods to adapt it to our specific problem.