A 270 Hz, Fine Frequency Tuning Class-C Oscillator Using Capacitive–Inductive Degeneration Technique in 130nm CMOS

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***Abstract*— This paper presents a high-resolution Class-C type voltage-controlled oscillator (VCO) with a robust start-up. The proposed oscillator achieves a minimum frequency quantification step of 270 Hz without adding any additional dithering approach. The very fine tuning is obtained through a capacitive-inductive degeneration coupling (CIDC) technique which reduces the capacitance value without appreciably affecting the intrinsic oscillator phase noise (PN). This technique also provides a negative transconductance to compensate for losses in the LC tank, resulting in high oscillation amplitude and relatively low power consumption in the oscillator core. The proposed design, implemented in 130 nm CMOS technology, achieves 45% tuning range. It exhibits a phase noise of –107 dBc/Hz @ 1-MHz offset, while it draws 5.75 mA from a supply of 1.2 V, resulting in a FoM of 165 dBc/Hz.**

Keywords—Capacitive-Inductive Degeneration Coupling; Class-C oscillator; LC-VCO; robust start-up; CMOS

I. INTRODUCTION

Nowadays, combining low power consumption, high speed and high spectral purity in voltage-controlled oscillator (VCO) is one of key challenges in CMOS circuit design and process methodologies of radio frequency (RF) VCO. Although the progress in technologies evolves by itself the enhancement of these goals, the target resolution for modern wireless applications is still quite challenging to reach fine frequency steps.

Several techniques such as the capacitive divider [1], the capacitive dithering [2] and the capacitive degeneration [3-5] have been suggested to minimize the unit step capacitance in LC oscillators. For example, a capacitive divider network that can be switched in parallel to the LC-tank is used in [1] to obtain a reduction of the minimum effective capacitance. This method can improve the oscillator frequency resolution but the sensitivity to parasitics and mismatches limits the robustness of the final design. A more reliable idea has been developed by *Staszewski et al.* in [2]. It consists in dithering least significant bits (LSB) of the oscillator control word (like ΣΔ modulator). The technique can achieve fine frequency from 12 kHz to 30 Hz, but as it occurs in any ΣΔ data converter, this solution faces problem of the quantification noise moved to higher frequencies. Another attractive approach is proposed by *Fanori et al.* [3]. It consists in moving a part of the capacitor bank from the LC-tank to the sources of the cross-coupled transistors of the oscillator.

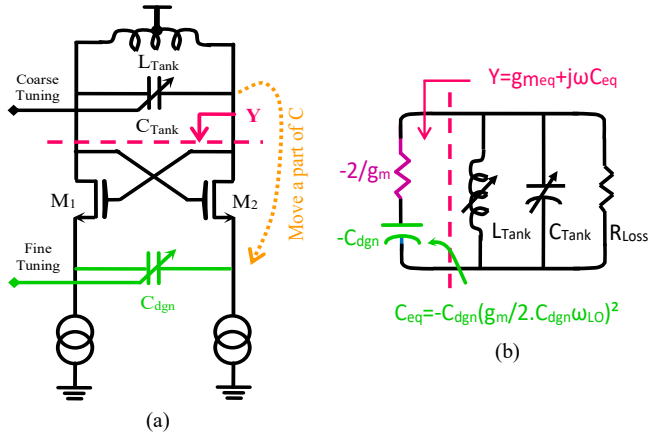

Fig. 1. (a) Simplified bloc diagram of the oscillator, (b) oscillator equivalent scheme [3]

At this level, an intrinsic shrink factor reduces the equivalent capacitive element and lowers considerably the equivalent oscillator frequency resolution (an averaged resolution of 300 Hz in [3], with a reasonable noise performance at the cost of several design constraints). The topology requires both small transconductance and high capacitance value to ensure an adequate shrink factor [3] and, at the same time, a large transconductance to sustain the VCO oscillations. That increases the design complexity, power consumption and area occupation.

In [4], we proposed an enhancement to overcome the limitations of [3]. By placing a resistive element in parallel to the degenerated capacitance, a robust start-up even is ensured with a relatively large choice of capacitance values, resulting in 3 kHz frequency resolution.

In this paper, an RLC stage through dithering process is designed and implemented in a LC oscillator. Alike to [3] and [4], the topology exploits small degenerated capacitance with more enhanced shrink effect, able to achieve a fine frequency of some hundred hertz without any additional circuit.

The paper is organized as follow. Section II introduces the basic idea of capacitive degeneration and its enhancement with a resistive element. Section III describes the amended topology with a detailed analysis. To verify the theoretical affirmations, an overview of implementation in a Class-C oscillator is proposed and followed by the simulated results in Section IV. Conclusions are given in Section V.

II. CAPACITIVE DEGENERATION TECHNIQUE

A. Basic idea using only a capacitor

The basic idea of minimizing the effective capacitance is innovated by Fanori et al. [1] [6]. As shown in Fig. 1(a), the technique consists in moving a part of the varactor bank from the LC-tank to the sources of two transconductances that built the negative impedance of the oscillator. The result shows that the moved portion of capacitor is submitted to an effort of shrinking factor effect appearing in the capacitive degeneration of transistors M_1 and M_2. Since the circuit works in large signal regime, the frequency tuning characteristics can be evaluated, as well as the shrink factor through small signal time variant analysis [7]. In order to simplify the analysis, it is supposed that the transconductance of cross-coupled transistors, g_m, is averaged over a time interval equal to one period of the oscillation frequency. Under the assumptions, the equivalent scheme reported in Fig. 1(b) can model the oscillator reported in Fig. 1(a).

The effect of the moved capacitance C_{dgn} on the oscillator frequency tuning characteristics can be determined by evaluating the admittance Y as $Y = g_{m\,eq} + jC_{eq}$:

$$Y = -\frac{g_m}{2}\cdot\frac{4C_{dgn}^2\omega_{LO}^2}{g_m^2+4C_{dgn}^2\omega_{LO}^2} - j\omega_{LO}C_{dgn}\cdot\frac{g_m^2}{g_m^2+4C_{dgn}^2\omega_{LO}^2} \quad (1)$$

where ω_{LO} is the proper oscillation frequency of the oscillation and C_{dgn} is negative since it follows the sign of current that crosses M_1 and M_2 (due to the drain-gate connection).

For $C_{dgn} >> g_m/2\omega_{LO}$, Eq. (1) can be simplified as follows:

$$Y = -\frac{g_m}{2} - j\omega_{LO}C_{dgn}\left(\frac{g_m}{2C_{dgn}\omega_{LO}}\right)^2 = -\frac{g_m}{2} - j\omega_{LO}C_{dgn}Q_f^2 \quad (2)$$

where Q_f is the quality factor of the impedance which models the degenerated effect in the switch defined by:

$$Q_f = \Im(Z)/\Re(Z) = g_m/2\omega_{osc}C_{dgn} \quad (3)$$

g_{meq} becomes the classical negative transconductance, which restores tank losses [8], while C_{eq} is the capacitor C_{dgn} shrunken by a factor F_{shrk} equal to $F_{shrk} = Q_f^2 = -\left(g_m/2C_{dgn}\omega_{LO}\right)^2$.

Starting from Eq. (2), g_{meq} and C_{eq} have been plotted in Fig. 2 versus C_{dgn}. The equivalent capacitance C_{eq} shows a non-monotonic behavior, where it starts to decrease for $C_{dgn} > g_m/(2\omega_{LO})$, whereas the equivalent conductance g_{meq} shows a monotonic behavior that asymptotically tend to $-g_m/2$. As well, the plot in Fig. 2 indicates that in order to sustain oscillation, the absolute value of the real part of Y, should be larger enough than $1/R_{loss}$, but also sufficiently small to keep the required effect of reducing the effective capacitance. This trade-off does not allow a degree of freedom, since C_{dgn} and g_m are univocally defined from Eq. (3), i.e. if the Q-factor of the resonator becomes low, the transconductance g_m becomes large leading to excessively large value for capacitor C_{dgn}. Contrarily, if $C_{dgn} < g_m/(2\omega_{LO})$, the real part of Y tends dramatically to zero and losses cannot be more compensated.

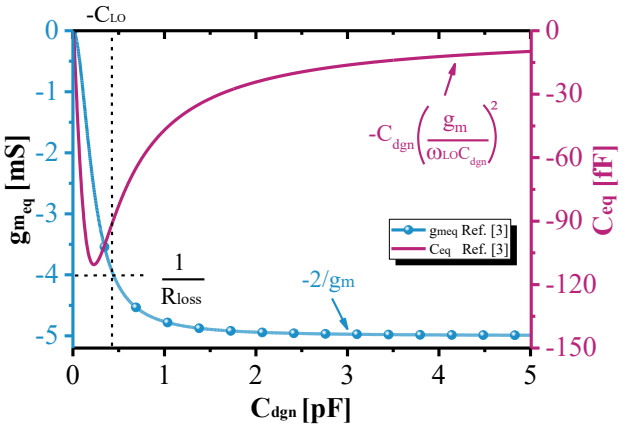

Fig. 2. Real and Imaginary parts of admittance Y (g_m=10 mS, R_{loss}=250 Ω, ω_{LO}=3.6 GHz) [3]

To resolve this drawback, an enhanced capacitive degeneration using resistive element is presented in the next sub-section.

B. Enhanced capacitive degeneration using a resistive element

As mentioned previously, placing in the region where $C_{dgn} >> g_m/2\omega_{LO}$, cannot provide a required shrink factor owing to weakness value of g_{meq}. Fig 3 shows a possible enhancement to compensate losses in the tank. A resistor R_{dgn} is added in parallel to the degenerated capacitor bank. Thus, the shrinking effect will be controlled accordingly to the following equation:

$$Y = -\frac{\frac{2}{g_m}+R_{dgn}+\left(\frac{2}{g_m}R_{dgn}C_{dgn}\omega_{LO}\right)^2}{\left(\frac{2}{g_m}+R_{dgn}\right)^2+\left(\frac{2}{g_m}R_{dgn}C_{dgn}\omega_{LO}\right)^2} - jC_{dgn}\omega_{LO}\frac{R_{dgn}^2}{\left(\frac{2}{g_m}+R_{dgn}\right)^2+\left(\frac{2}{g_m}R_{dgn}C_{dgn}\omega_{LO}\right)^2} \quad (4)$$

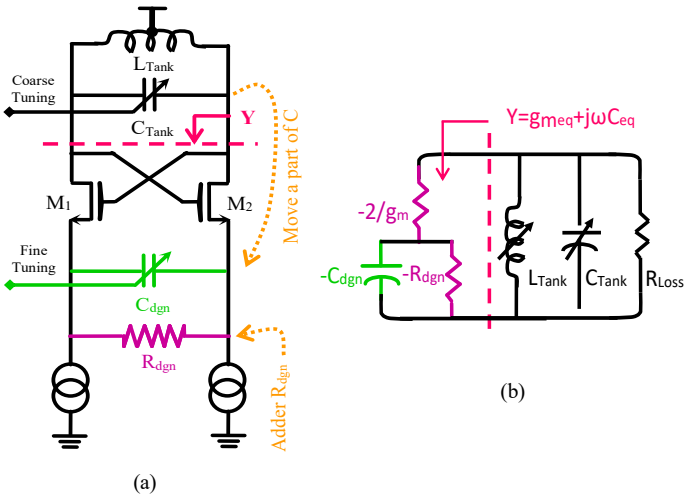

Fig. 3. (a) Simplified bloc diagram of the oscillator, (b) oscillator equivalent scheme [4]

Since $\left(\frac{2}{g_m}R_{dgn}C_{dgn}\omega_{LO}\right)^2 << \left(\frac{2}{g_m}+R_{dgn}\right)^2$ and $\frac{2}{g_m}\left(R_{dgn}C_{dgn}\omega_{LO}\right)^2 << 2/g_m$ and R_{dgn}, the expression of the admittance Y becomes:

$$Y \approx -\frac{1}{\frac{2}{g_m}+R_{dgn}} - jC_{dgn}\omega_{LO}\frac{R_{dgn}^2}{\left(\frac{2}{g_m}+R_{dgn}\right)^2} \quad (5)$$

Comparing this expression with Eq. (2), the main difference is that in this structure, gm_{eq} becomes the conventional negative impedance placed in series with the resistance R_{dgn}, while C_{eq} is equivalent to C_{dgn} shrunked by a factor F_{shrk} given by:

$$F_{shrk} = \frac{R_{dgn}^2}{\left(\frac{2}{g_m}+R_{dgn}\right)^2 + \left(\frac{2}{g_m}R_{dgn}C_{dgn}\omega_{LO}\right)^2} \approx \frac{R_{dgn}^2}{\left(\frac{2}{g_m}+R_{dgn}\right)^2} \quad (6)$$

This factor is equal to $(Q_f/C_{dgn}R_{dgn}\omega)^2$, where Q_f is the Q-factor of the admittance which models the degenerated effect in the feedback, and shown to be:

$$Q_f = \frac{\Im[Y]}{\Re[Y]} \approx \frac{C_{dgn}R_{dgn}^2\omega_{LO}}{\frac{2}{g_m}+R_{dgn}} \quad (7)$$

Similar to [3], to decrease the equivalent capacitance, Q_f could be further decreased to minimize the frequency resolution of the oscillator.

Based on Eq. (5), the transfer function of gm_{eq} and C_{eq} are plotted in Fig. 4, for same parameters as in [3]. It can be seen that a different variation of gm_{eq} over C_{dgn} is obtained. The curve starts from $1/g_m+R_{dgn}$ and has almost a linear behaviour asymptotically close to -4.5 mS. The advantage of using an additional resistance is that the real part of Y is considerably retained for low value of C_{dgn}, because R_{dgn} will play the same role of g_m, and is converted to transconductance. This results in sustaining the oscillation although small values of C_{dgn} are used. Another advantage is that C_{eq} is optimized and shows quite linear tendency which is beneficial to improve frequency resolution and tuning range.

The minimum resistance $R_{dgn(min)}$ must be chosen to satisfy the required shrink factor. It is determined by the following formula:

$$F_{shrk} \approx \frac{R_{dgn}}{\left(\frac{2}{g_m}+R_{dgn}\right)^2 + \left(\frac{2}{g_m}R_{dgn}C_{dgn}\omega_{LO}\right)^2} < 1 \quad (8)$$

III. Proposed Capacitive-Inductive Degeneration Coupling Technique

In the proposed circuit presented in Fig. 5, a couple of resistor and inductor is placed in parallel to the variable capacitor bank.

To study the proprieties effect of changing the capacitance C and the insertion of R-L components on the tuning of the oscillator frequency characteristic, the same methodology mentioned earlier has been applied. The admittance Y in the equivalent scheme of Fig. 6 is given by:

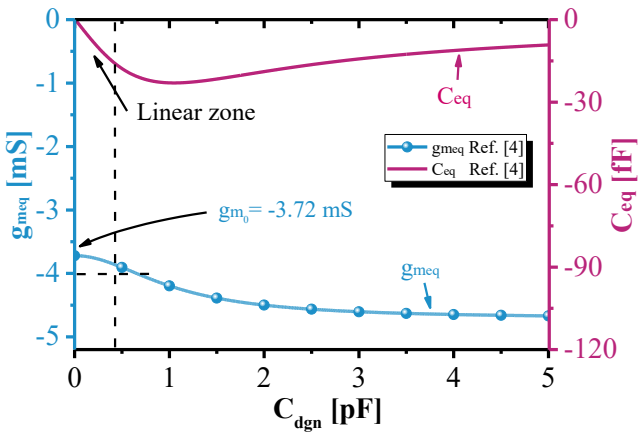

Fig. 4. Real and imaginary parts of admittance Y vs capacitance (g_m=10 mS, R_{dgn}=455 Ω, L_{dgn}=025 pH, f_0=3.6 GHz) [4]

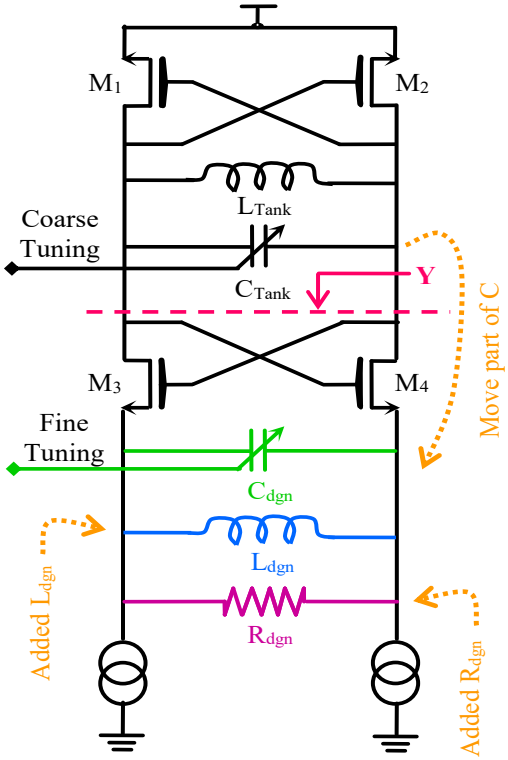

Fig. 5. Simplified bloc diagram of the proposed oscillator with CIDC

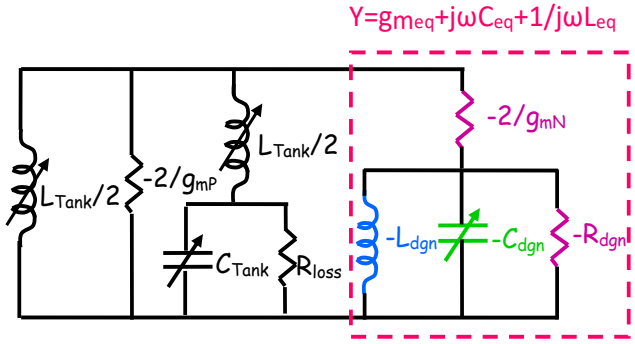

Fig. 6. Equivalent scheme of the proposed oscillator with CIDC

$$Y=-\frac{\frac{2}{g_{mN}}\left(\left(L_{dgn}\omega_{LO}-R_{dgn}\right)^2+\left(R_{dgn}L_{dgn}C_{dgn}\omega_{LO}^2\right)^2\right)+R(L_{dgn}\omega_{LO})^2-R_{dgn}^2L_{dgn}\omega_{LO}}{\left(\frac{2}{g_{mN}}(R_{dgn}-L_{dgn}\omega_{LO})-R_{dgn}L_{dgn}\omega_{LO}\right)^2+\left(\frac{2}{g_{mN}}R_{dgn}L_{dgn}C_{dgn}\omega_{dgn}^2\right)^2}-jC_{dgn}\frac{L_{dgn}^2R_{dgn}^2\omega_{dgn}^3}{\left(\frac{2}{g_{mN}}(R_{dgn}-L_{dgn}\omega_{LO})-R_{dgn}L_{dgn}\omega_{LO}\right)^2+\left(\frac{2}{g_m}R_{dgn}L_{dgn}C_{dgn}\omega_{dgn}^2\right)^2} \quad (9)$$

Since $\left(\frac{2}{g_{mN}}R_{dgn}L_{dgn}C_{dgn}\omega_{LO}^2\right)^2 << \left(\frac{2}{g_{mN}}(R_{dgn}-L_{dgn}\omega_{LO})-R_{dgn}L_{dgn}\omega_{LO}\right)^2$ and $\left(R_{dgn}^2L_{dgn}^2C_{dgn}^2\omega_{LO}^4\right) << \left(L_{dgn}\omega_{LO}-R_{dgn}\right)^2$,
Eq. (9) can be rewritten as follow:

$$Y=-\frac{\frac{2}{g_{mN}}\left(L_{dgn}\omega_{LO}-R_{dgn}\right)^2+R_{dgn}(L_{dgn}\omega_{LO})^2-R_{dgn}^2L_{dgn}\omega_{LO}}{\left(\frac{2}{g_{mN}}(R_{dgn}-L_{dgn}\omega_{LO})-R_{dgn}L_{dgn}\omega_{LO}\right)^2}-jC_{dgn}\frac{L_{dgn}^2R_{dgn}^2\omega_{dgn}^3}{\left(\frac{2}{g_{mN}}(R_{dgn}-L_{dgn}\omega_{LO})-R_{dgn}L_{dgn}\omega_{LO}\right)^2} \quad (10)$$

Referring to the equation mentioned in Fig. 6, the first term is the negative conductance given by:

$$g_{m\,eq}=\frac{\frac{2}{g_{mN}}\left(L_{dgn}\omega_{LO}-R_{dgn}\right)^2+R_{dgn}(L_{dgn}\omega_{LO})^2-R_{dgn}^2L_{dgn}\omega_{LO}}{\left(\frac{2}{g_{mN}}(R_{dgn}-L_{dgn}\omega_{LO})-R_{dgn}L_{dgn}\omega_{LO}\right)^2} \quad (11)$$

The second term reveals the equivalent capacitance C_{eq} emulated in the capacitance C_{dgn} shrunked by a factor of:

$$F_{shrk}=\frac{L_{dgn}^2R_{dgn}^2\omega_{LO}^2}{\left(\frac{2}{g_{mN}}(R_{dgn}-L_{dgn}\omega_{LO})-R_{dgn}L_{dgn}\omega_{LO}\right)^2+\left(\frac{2}{g_{mN}}R_{dgn}L_{dgn}C_{dgn}\omega_{LO}^2\right)^2}$$
$$\approx\frac{L_{dgn}^2R_{dgn}^2\omega_{LO}^2}{\left(\frac{2}{g_m}(R_{dgn}-L_{dgn}\omega_{LO})-R_{dgn}L_{dgn}\omega_{LO}\right)^2} \quad (12)$$

Further, the quality factor Q_f of Y where its models the degenerated effect in the feedback, can be expressed as:

$$Q_f=\frac{\Im[Y]}{\Re[Y]}\approx\frac{C_{dgn}L_{dgn}^2R_{dgn}^2\omega_{LO}^3}{\left(\frac{2}{g_{mN}}\left(R_{dgn}-L_{dgn}\omega_{LO}\right)-R_{dgn}L_{dgn}\omega_{LO}\right)^2} \quad (13)$$

To confirm the effect of adding R_{dgn} and L_{dgn}, gm_{eq} and C_{eq} are theoretically extracted in Fig 7, while maintaining the same configuration for fair comparison.

The result shows that gm_{eq} becomes more steady throughout capacitance C_{eq}. Practically, it has a horizontal straight behavior of around -5 mS. Considering the behavior of C_{eq}, it has a wide linear monotonic-curve without much variation on the value of shrunken capacitor. The shrink factor is proved in Fig. 8, with results from [3] and [4] for the same conditions. From the different plots of Fig. 8, it can be seen that a capacitor of 2 pF is reflected in the parallel to the LC-tank into an equivalent capacitance of 1.62 fF with a shrinking factor $1/F_{shrk}$ of about 1233. This factor is, respectively, 14 and10, times greater than factor in [3] and [4].

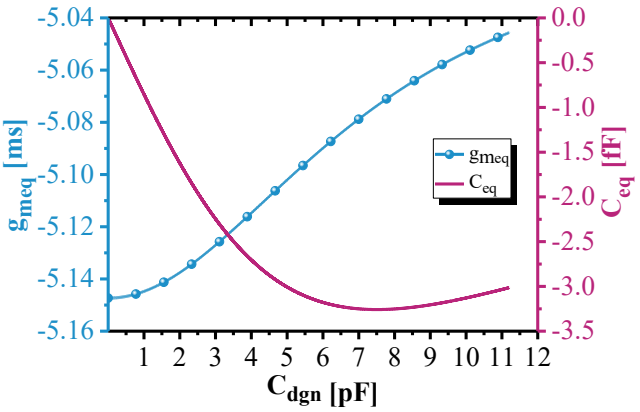

Fig. 7. Real and imaginary parts of admittance Y vs capacitance (g_{mN}=10 mS, R_{dgn}=455 Ω, L_{dgn}=0.25 pF, f_0=3.6 GHz) of the proposed structure

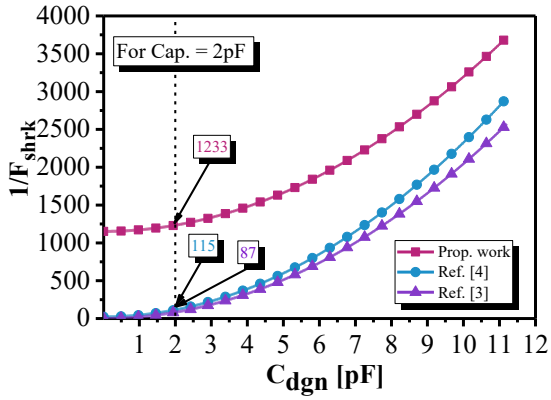

Fig. 8. Shrink factor versus capacitance

Expression of the resonance frequency ω_{LO} of the proposed circuit (cf. Fig. 6), as a function of the capacitance C_{dgn} placed between the sources of the negative resistance of NMOS transistors, can be found and deduced by the following expression:

$$f_{LO}(C_{dgn})\approx\frac{\omega_0}{2\pi}\sqrt{1+\left(Q_f\frac{C_{dgn}}{C_{TANK}}\right)} \quad (14)$$

where Q_f is given by Eq. (13) and $\omega_0=1/\sqrt{C_{TANK}L_{TANK}}$ represents the resonant frequency of the conventional LC oscillator.

Eventually, the shrink factor is influenced by L_{dgn}, R_{dgn} and ω_{LO}. Eq. (15) can be settled straightforwardly to an inequality < 1 in order to keep the effect at optimum:

$$F_{shrk} \approx \frac{L_{dgn}^2 R_{dgn}^2 \omega_{LO}^2}{\left(\frac{2}{g_{mN}}(R_{dgn} - L_{dgn}\omega_{LO}) - R_{dgn}L_{dgn}\omega_{LO}\right)^2} < 1 \quad (15)$$

IV. Application to a Class-C Oscillator

In order to validate the presented equations, the VCO depicted in Fig. 9 is designed in 130 nm CMOS technology with an NMOS varactor and a 32-bits fine array. The proposed architecture consists of a complementary Class-C oscillator as the core, a bias circuitry, and coupling stages with capacitive source degeneration. The proposed circuit was tailored to RF ISM frequency band applications, with a center frequency of XX GHz.

The tank consists of a spiral differential inductor of 3.75 nH with a simulated maximum quality factor of 34.6. For the coarse tuning bank, a NMOS varactor providing an average gain of around 1.025 GHz/V was implemented. The fine tuning bank was realized as reported in Fig 9. Since it is difficult to approve the effect of unit capacitance of a few atto-farad on the oscillation frequency, 32 capacitor pairs are tied in parallel. The row of varactor pairs is implemented with pair NMOS transistors in the inversion mode configuration. Although the C-V characteristic is non-linear and near monotonic, the transition from C_{mim} to C_{max} is very biased which is effectively useless tuning gain in analog domain, so a digital toggling command is adopted to simplify the control of the row. The untied unit varactor pair is controlled by the Tuning Control Word (TCW) where it measures a unit per one digital weight variation capacitance of 258 aF while changing the control voltage from 0 to 1 V. The unitary NMOS elements size is W=10 µm and L=0.13 µm with a maximal total capacitance of 8.3 pF.

To create the negative g_m, a cross-coupled pair is adopted, and the complementary topology (NMOS and PMOS) is used to reduce power consumption. To operate in Class-C, transistors of the cross-coupled pair are both biased in the saturation region. Hence, the bias voltage of NMOS (V_{gsn}) has to be lowered with respect to the supply voltage. Although this choice is not mandatory, it increases the transconductance of the differential pair and at the same time reduces the phase noise [9]. In addition, a large capacitance (C_{tail}) is connected at the drain of the tail current source, which filters the high-frequency noise injected by the bias and aids in shaping the injection current for a given shrinking factor [10].

The simulated fine-tuning frequency characteristic, shown in Fig. 10, demonstrates a very good agreement with the theoretical analysis. It has the same linear behavior as that of the theoretical curve. In this slope of operation, the shrink factor is around 1233 (0.82%) with a fine-tuning range of about 8.652 kHz, under 32 varactors. The attained effective fine-frequency step is approximately 270 Hz through capacitance-inductive degeneration.

In Fig. 11, the obtained Integral-Non-Linearity (INL) and Integral-Non-Linearity (DNL) curves are reported. A good linearity is achieved since the DNL is 0.37 LSB while the INL is 0.42 LSB.

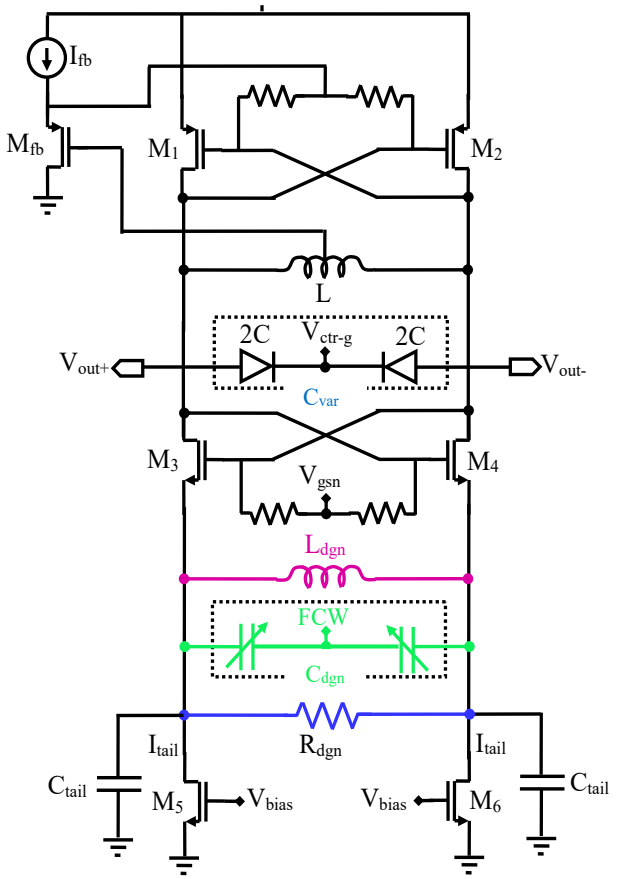

Fig. 9. Schematic of the proposed Class-C type degenerated VCO

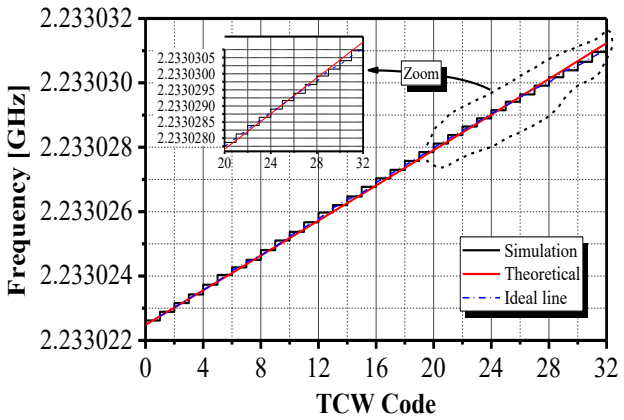

Fig. 10. Oscillator fine-tuning frequency response vs. the tuning control word

Fig. 12 depicts the simulated phase-noise characteristic from 100 Hz to 10 MHz of offset frequency. The oscillator achieves a phase noise of -107 and 120 dBc/Hz at 1 and 3 MHz offset, respectively, from the carrier frequency when oscillation frequency is 2.23 GHz.

The Figure of Merit (FoM) evaluated by Eq. (16) according to [11] is equal to 166 dBc/Hz.

$$FoM = L(\Delta f) - 20\log_{10}\left(\frac{f_0}{\Delta f}\right) + 10\log_{10}\left(\frac{P_{DC}[mW]}{1mW}\right) \quad (16)$$

where $L(\Delta f)$ is the measured phase noise in dBc/Hz at a frequency offset of Δf from the carrier frequency f_0 and P_{DC} is the measured power dissipation of the oscillator.

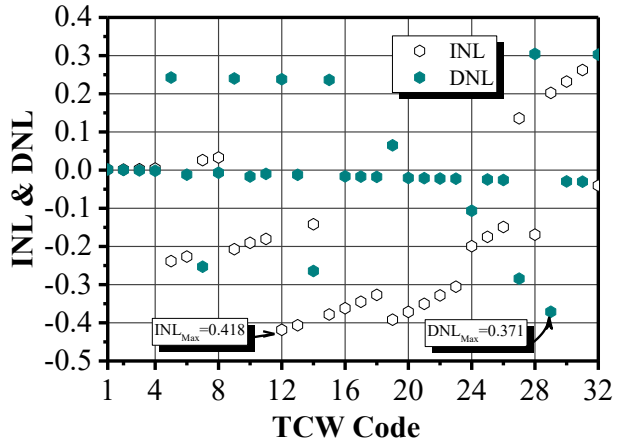

Fig. 11. Oscillator INL/DNL vs input code and 1 LSB for fine-tuning bank

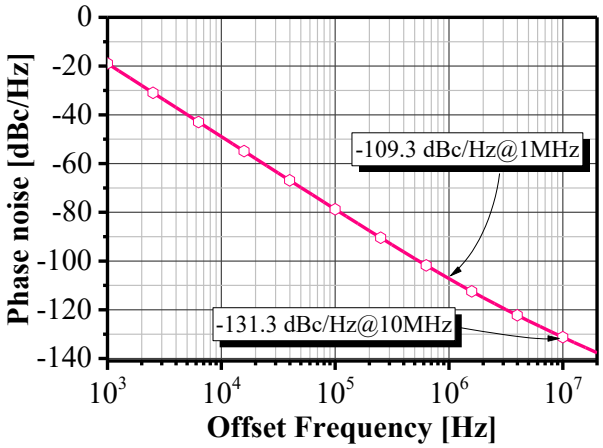

Fig. 12. Simulated phase noise of the proposed oscillator

In comparison with performances of other works, as shown in Table I, the proposed oscillator achieves the superior frequency resolution and the lowest power dissipation at 3.2 GHz with reasonable phase noise even in a 130 nm CMOS technology.

TABLE I. OSCILLATOR PERFORMANCE COMPARISON

Parameter	**This work**	[2]	[3]	[4]
CMOS Process [nm]	**130**	90	65	90
Supply voltage [V]	**1.2**	1.4	1.8	1.0
Tuning range [GHz]	**2.23-3.25**	3.2-4	2.9-3.6	1.22-3.52
Frequency tuning range (FTR) [%]	**45.7**	22.2	26	65
Phase noise@1MHz [dBc/Hz]	**-107**	-136	-127.5	-105.8
Structure [Cap.Tech.]	**Class-C**	Class-B	Class-C	Class-B
Resolution [kHz]	**0.27**	12[(b)]	0.15-1.5[(a)] [(c)]	3-16[(a)]
Power [mW]	**6.9**	18	16	4.8-5.2
FoM [dBc/Hz]	**-165.6**	N/A	-183	-174.8

[(a)] Capacitive degeneration, [(b)] Without dithering, [(c)] Tunable acting on current variation

V. CONCLUSION

A capacitive-inductive degeneration coupling technique (CIDC) has been proposed and applied to a CMOS Class-C oscillator. By using an RLC circuit mounted in parallel to the tank, capacitance is shrunken and frequency step can be further reduced. By exploiting a PMOS varactor in inversion region C-V characteristics, the equivalent capacitance diminishes to approximately 0.21 aF. This allows to perform a minimum frequency step with a resolution of about 270 Hz without any dithering process. The small signal analysis demonstrates the limits and the potentialities of the proposed idea, while the simulation results prove its robustness in 2.2-3.2 GHz frequency band. Even if the proposed structure is implemented in 130 nm CMOS technology, the oscillator has superior performances in terms of frequency tuning resolution with reasonable power consumption and phase noise compared to the state-of-the-art.

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