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Ultra-Low-Power Wideband NMOS LC-VCO Design for Autonomous Connected Objects

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Abstract—In this paper, a fully integrated subthreshold LC voltage controlled oscillator (VCO) is presented. A design methodology is also proposed to find the optimal parameters lowering the power consumption. This methodology has been applied to design oscillators for different frequency bands. Furthermore, an adaptive body biasing technique has been used to improve the startup constraints and allows a high immunity to PVT (process, voltage and temperature) variations. A VCO operating in 5 GHz ISM (Industrial, Scientific and Medical) band has been realized with the proposed methodology in 0.13 μ m CMOS. It consumes only 468 μ W from 0.39V supply voltage. This makes it possible to meet the required specifications of autonomous connected objects and IoT applications. The measured oscillation frequency can be tuned from 5.14 GHz to 5.44 GHz. The obtained phase noise is approximately equal to -112 dBc/Hz in post-layout simulation (PLS) and -104.5 dBc/Hz in measure.

Keywords—LC-VCO, RF, design methodology, subthreshold, PVT, adaptive body biasing, low power, IoT.

I. INTRODUCTION

The recent years have seen a drastic rise in Internet of Things (IoT) devices and connected products such as home automation systems, smart appliances, wireless sensors, and wearable etc. Objects are becoming intelligent and wirelessly interoperable to enhance transport, logistics, Health care digital, life and digital industry [1, 2]. It is envisioned that billions of objects will be equipped with sensors and will be connected to the Internet via heterogeneous access networks. This is due to the development of communication technologies such as radio frequency identification (RFID), semantic web services and wireless sensor networks etc. [3]. Studies estimate that 212 billion connected IoT objects will be reach in the end of 2020 [4].

Key requirement for these devices is the implementation of low power, low-cost and reconfigurable systems. In fact, an IoT sensor node should be portable and able to work under batteries or even able to harvest ambient energy for several years. The general architecture of an IoT sensor node is shown in Fig.1. It is composed of a wireless transceiver, a sensor, a power block and a processor unit, or a microcontroller (MCU) [5]. The wireless transceiver allows transmission and reception of the data using radio frequency (RF) connectivity. It is an important part of IoT systems which mostly affects the performance of the system. So, the transceiver RF must meet drastic power constraints.

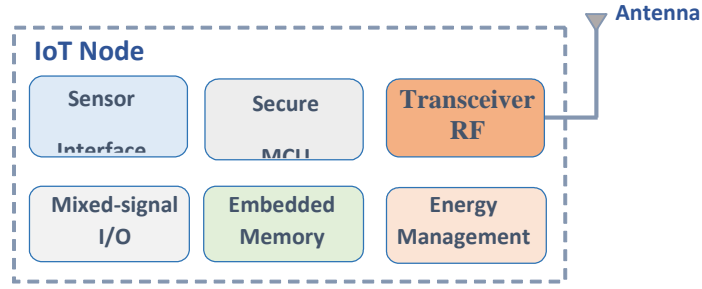


Fig 1. IoT sensor node topology

The voltage controlled oscillator (VCO) is an essential building block in all radio transceivers. It generates a local signal that is used in both sides (reception and transmission) to transport the RF to the required band. This block consumes the significant portion of the power budget. In this work, the main challenge consists in minimizing its power consumption. Many researches have been reported in literature in order to reduce the power consumption of VCOs which can be applied at different levels of abstraction (system, circuit or technology levels). For the circuit level, two main techniques have been presented: reducing the supply voltage and using the current-reuse techniques. This later suffers from asymmetrical outputs in terms of amplitude and phase [6-8]. The first technique requires the use of subthreshold MOS devices which present some drawbacks such as high sensitivity to PVT variations [9, 10]. These variations are caused by the exponential property of MOS transistors in the subthreshold region.

The purpose of this work is to design subthreshold VCOs with high immunity to PVT (process, voltage, and temperature) variations. Furthermore, a design methodology saving the power consumption and aiming optimal parameters has been used to satisfy the requirements of IoT applications: autonomy, stability and frequency agility. This paper is organized as follows. Section 2 investigates the subthreshold LC-VCO design. Section 3 describes the proposed design methodology of ultra-low power LC-VCOs. Section 4 presents the simulation results for different frequency bands. The obtained measurement results of an LC-VCO operating at 5.4 GHz are presented and discussed in section 5. Finally, section 6 draws conclusions.

II. SUBTHRESHOLD RF LC-VCO DESIGN

Several researches have been carried out in literature to implement ultra-low power analog circuits. A reduction of the supply voltage is considered as one of the most important techniques to reduce the power consumption, which pushed designers to use special approaches, such as using subthreshold MOS transistors.

In the subthreshold regime, also known as weak inversion, the drain current depends exponentially on the gate source voltage V_{gs} . This latter is slightly below the transistor's threshold voltage V_{th} and the concentration of carriers is very low but not negligible.

Subthreshold MOS transistors exhibit high transconductance g_m for a given bias current and comparable noise performance with the superthreshold ones. However, the subthreshold operation is less robust to transistor mismatches, power-supply noise and temperature compared to the other regimes. It presents a high sensitivity to PVT variations. In order to guarantee stable operation even while working in worst conditions, designers should consider the variations of the transconductance, so that biasing techniques should be used. The adaptive body-biasing technique is an adequate solution, since it improves the immunity to PVT variations and ensures the stabilization of V_{th} and g_m .

In this work, an NMOS cross-coupled topology using the adaptive body biasing technique has been selected. Figure 2 presents the detailed schematic of the VCO topology. It is composed by an LC resonator, also referred as LC-tank, an adaptive body biasing circuit (M_3 and M_4) and an NMOS cross-coupled pair (M_1 and M_2) biased in the subthreshold region. This pair is used to provide the negative conductance and to overcome the tank loss. The negative transconductance can be expressed as:

$$g_{active} = -\frac{g_{m_NMOS}}{2} \quad (1)$$

where g_{m_NMOS} is the transconductance of the NMOS transistor.

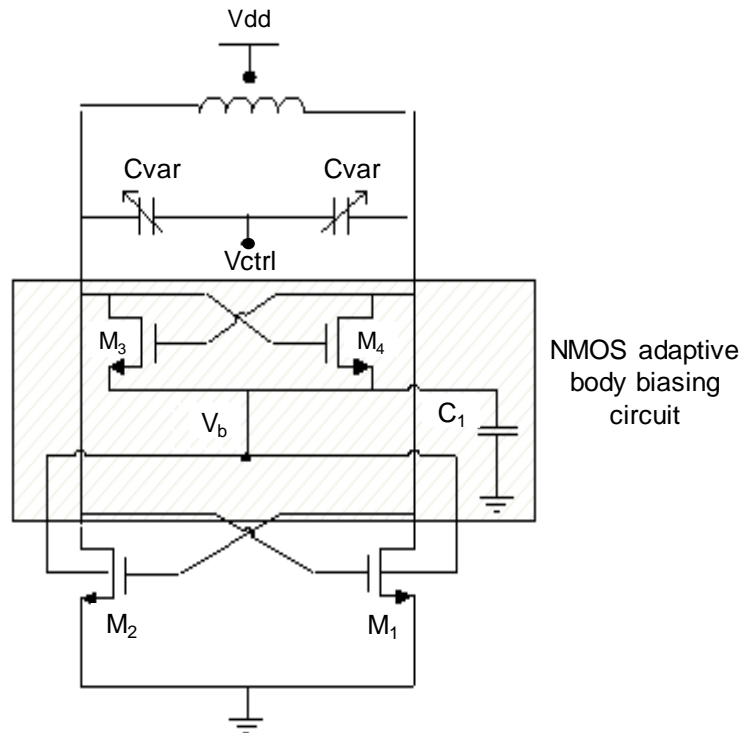


Fig. 2. Schematic of the implemented LC-VCO

The adaptive body biasing circuit adjusts automatically the threshold voltage of MOS transistors as well as the transconductance. Moreover, this circuit improves the startup constraint and reduces the MOS drain source current. Thus, when the threshold voltage varies, the power consumption can be decreased. The adaptive body biasing circuit allows to detect the VCO output amplitude (V_+ and V_-) and to feed it

back to the body bias in the negative transconductance cell. If the output amplitude of the VCO varies, the bulk voltages of g_{m_NMOS} are automatically adjusted in order to maintain a constant transconductance over PVT variations and to maintain the oscillation. As shown in Fig.2, the adaptive body biasing circuit is composed by a symmetric NMOS transistor pair and a grounded capacitor C_1 . This circuit detects the lowest magnitude and stores the voltage V_b into the capacitor. When the output amplitude decreases, V_b increases which lowers the threshold voltage of the negative transconductance cell [11]. This causes the increase of g_{m_NMOS} as well as the output amplitude. Initially, the negative transconductance is not sufficient to satisfy the oscillation condition. Then, the adaptive bloc can be used to speed up the oscillation startup of the VCO. In fact, the gate and drain voltages of M_3 and M_4 are initially set to $V_{dd}/2$. When these transistors are turned on, V_b increases and V_{th} of M_1 and M_2 decreases. This causes a higher value of the negative transconductance. In this case, the startup condition is met and the VCO starts oscillating.

III. LC-VCO DESIGN OPTIMIZATION APPROACH

In order to reach an ultra-low power operation suitable for IoT applications and to respect the various constraints, a design methodology using an optimization approach has been used in this work. It allows the design of high performance LC-VCO. This generic design methodology is based on the study and the optimization of VCO's components (inductor L , varactor C and active circuit). The designers should study the relation components/constraints and the impact of the physical and technological parameters of VCO's elements on its performances (power consumption, tuning range, phase noise and area occupation). For example, in order to enhance the power consumption and phase noise (PN) performances, it is necessary to optimize each element of the VCO and especially the LC resonator. Its quality factor (Q) and resistive losses (g_p) must be taken into account, since increasing Q and reducing g_p can improve both power consumption and PN. The design flow of high-performance LC-VCOs is illustrated in Fig. 3. It is based on three steps, as detailed below: i) the inductor optimization by maximizing the corresponding quality factor and minimizing the resistive losses, ii) followed by the varactor optimization, and iii) finally the active circuit optimization. In our study, the 130nm CMOS technology has been used to design VCOs.

- **Inductance optimization strategy**

The optimization process of the inductor requires a great attention when considering the design of high-performance VCO. The first step is to choose the inductor's type according to the targeted constraints. In order to satisfy the need of designers, different types of inductors are proposed in the technology design-kit ('*Ind_Sym_la*', '*Ind_Sym_mf*', '*Ind_dif_la*', etc.). Furthermore, the used technology provides differential inductance that is also more appropriate to design differential structure [12]. Indeed, the differential inductor results in chip area saving compared to two single-ended inductors. In this work, several S-parameter simulations have been realized using Spectre-RF simulator of Cadence.

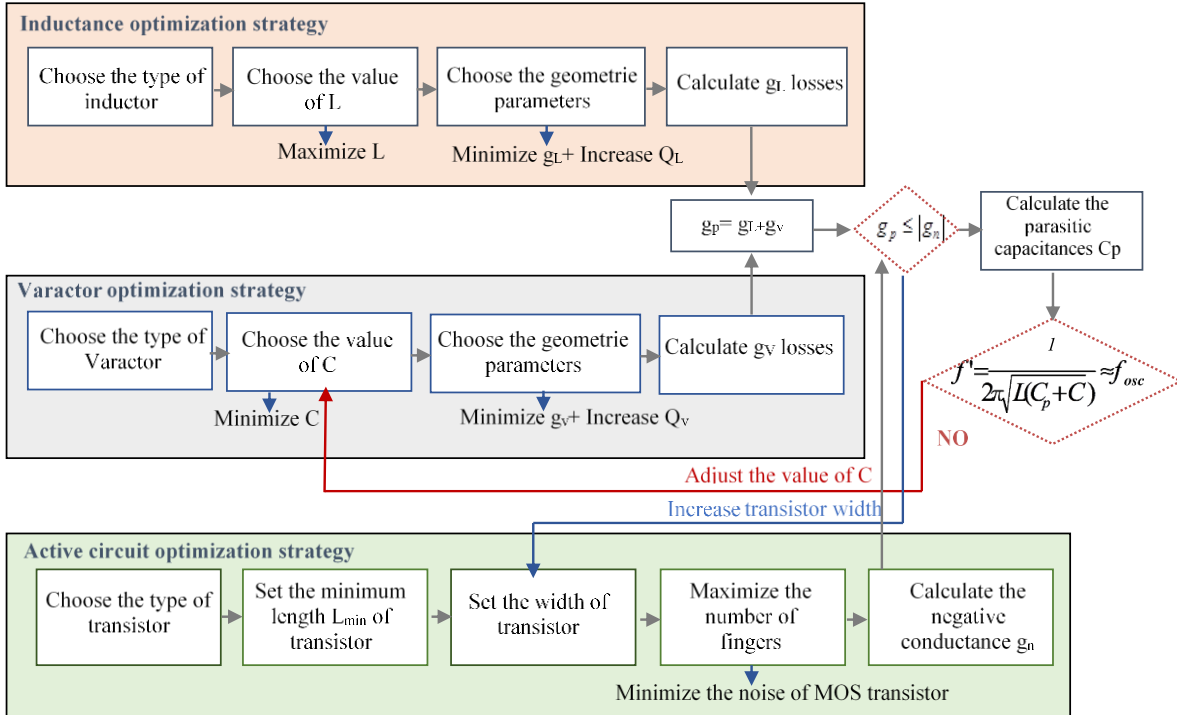


Fig. 3. Design methodology of sub-mW LC-VCO

The obtained results have demonstrated that the ‘*Ind_dif_la*’ inductor type presents a good compromise between quality factor (Q_L), resistive loss (g_L), occupation area and self-resonant frequency (SRF) compared to the other types. The second step is to size the inductance value. A high inductor value with minimal series resistance and maximal quality factor should be chosen since increasing L value reduces both power consumption and PN. Note that increasing L value is limited by its SRF, which should be higher than the oscillation frequency. Finally, designers should adjust both geometrical parameters: the inductor track width (W) and the number of turns (N). In this case, the influence of these two parameters has been studied. In order to decrease the resistive loss (g_L), the minimum number of turns (N_{min}) should be used. However, it is important to increase N in order to increase the inductance value that is also related to the technological constraints. Besides, the inductor's track width has a significant impact on SRF, Q_L and g_L . Generally, increasing track width allows to reduce the g_L and then to increase Q_L . However, it presents some drawbacks such as increasing the substrate coupling. This can cause a decrease of self-resonance frequency. Note that this SRF should be higher than the operating frequency to maintain the inductive behavior. So, in order to increase the SRF, designers should use occasionally the minimum track width (W_{min}).

- **Varactor optimization strategy**

The varactor is an essential component in LC resonator, since its quality factor affects the power dissipation and the phase noise performances. So, it is necessary to optimize the varactor to assess the performance of VCO. The optimization strategy begins with choosing the varactor type according to

constraints of the targeted application. For example, for a high constraint in terms of tuning range, the MOS varactors are recommended. However, for high constraints in terms of consumption and PN, it is preferable to use the diode varactor, since it presents a good compromise between linearity, quality factor (Q_v) and effective parallel equivalent conductance. For this design, diode varactor has been used. Then, the value of C should be minimized in order to reduce PN and power consumption. However, this will contribute to lower the frequency tuning range. Finally, the physical parameters of the varactor have to be adjusted. For example, for a diode varactor, both number and width of $P+$ bars can be adjusted in order to obtain a good compromise between capacity tuning range and quality factor. These characteristics affect the performance of the oscillator in terms of tuning range and PN.

- **Active circuit optimization strategy**

The active circuit is an essential block of VCO that is used to overcome the tank loss. However, it also brings back parasitic elements which can degrade the phase noise of the VCO and modify the oscillation frequency. In this circuit, using low-leakage transistors with minimum channel length can improve the switching speed and decrease the power consumption. Then, transistor width is determined in order to provide the minimum transconductance. Using the maximum number of fingers (NF) decreases the gate resistance and consequently, improve the performances of VCO in terms of noise and power consumption.

IV. SUB-mW RF LC-VCO IMPLEMENTATION AND RESULTS

1) Validation of the design methodology for different frequency bands

Rising the operating frequency presents important challenges in monolithic VCO design. Moreover, the oscillator must ensure high performances in terms of power consumption and PN. The contribution of our work is to design VCOs for different frequency bands and to verify the reliability of the proposed design methodology in high frequencies. Hence, several VCOs working at different frequency bands (from 1.5 to 9 GHz) have been implemented in 0.13 μ m CMOS technology. A low varactor value has been used ($C_v=0.4$ pF, $W_{p+}=1$ μ m, $NP+=4$), while, for each frequency band, we have varied both the transistors (W , NF) and the inductor (L , N , W).

Figure 4 illustrates the obtained results for the different oscillators. Note that each point represents a fixed designed circuit. Once comparing the obtained performances versus frequency, it can be seen that when the frequency increases, the phase noise and power consumption are kept low. That confirms the effectiveness of both subthreshold operation and design methodology.

These charts (cf. Fig.4) can be used to facilitate the optimal oscillator choice according to the constraints and requirements of the targeted application. Furthermore, it can be used to estimate the performances of any LC-VCO using the supply voltage reduction technique, in terms of power consumption and phase noise, for different frequency bands.

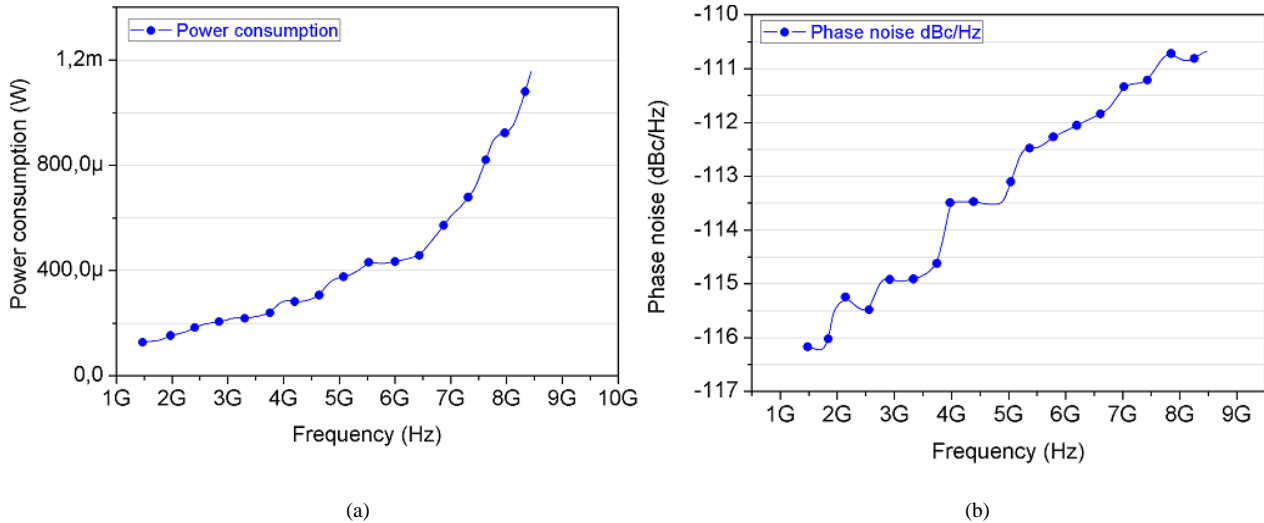


Fig.4. (a) Power consumption and (b) phase noise of LC-VCOs operating at different frequencies

2) LC-VCO implementation

An RF NMOS LC-VCO operating around 5.4GHz has been realized in 130nm CMOS technology from STMicroelectronics. The body biasing technique needs the use of a triple-well technology that offers the possibility of biasing the *P*-well independently from the *P* substrate [13]. The layout and microphotograph of VCO are shown in Fig.5. The LC-VCO layout occupies an area of (315 x 459) μm^2 without PADs and (560 x 426) μm^2 with PADs and decoupling capacitors (C_d). Note that the spiral inductor occupies more than 2/3 of the total surface.

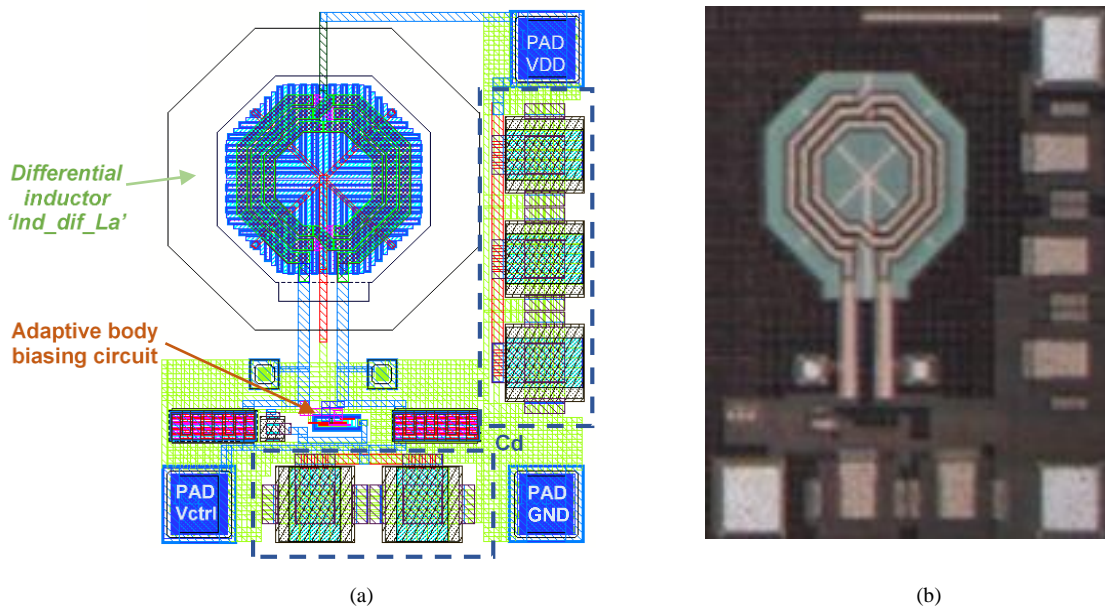


Fig. 5. (a) Layout and (b) microphotograph of the LC-VCO

In order to confirm the robustness of the adaptive body biasing technique, the oscillator has been checked taking into account the parasitic elements under various PVT. Different state corners are presented in this work. The first state combines the typical process and moderate temperature. The

second state combines worst PVT corners (high temperature, low Vdd and slow-slow process). The third state takes the best PVT corners (low temperature, high Vdd and fast-fast process). Table 1 presents the post-layout simulation results and the obtained percentages of variation in the different cases compared to the typical one. It can be noted that the oscillation is preserved even in the worst case. Also, an acceptable immunity to PVT variations is achieved confirming the efficiency of the adaptive body biasing technique. For example, in the best case, the observed variation in frequency, phase noise and power consumption is equal to only 1.2%, 1.7% and 29.3% respectively compared to the typical condition.

TABLE I. LC-VCO PERFORMANCES UNDER PVT VARIATIONS

	Typical case	Worst case		Best case	
Frequency of oscillation (GHz)	5.57	5.5	1.2%	5.53	0.7%
Power consumption (mW)	388	274	29.3 %	536	38%
Phase noise @1MHz (dBc/Hz)	-112	-110	1.7%	-111.1	1%
Peak-to-Peak output voltage (mV)	580	435	25%	700	20%

Additional analysis of the process and mismatch effect, through Monte Carlo simulations, has been performed with Spectre-RF of Cadence tool taking into account the layout extracted parasitic.

The obtained phase noise histogram of 100 iterations together with the fitted normal distribution curve are shown in Fig. 6. It depicts a mean phase noise value of -111.8 dBc/Hz and a standard deviation of only 0.19. These results confirm the robustness of the proposed sub-mW LC-VCO regarding the noise analysis.

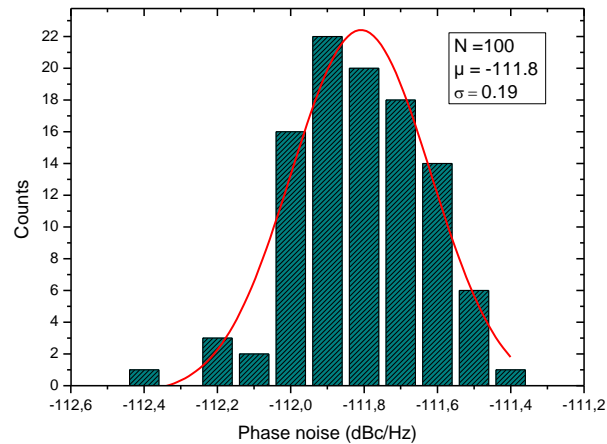


Fig. 6. The obtained phase noise histogram of 100 iterations

3) Measurement results

In order to assess the performances of the RF LC-VCO design, several measurements have been performed, under the following conditions: supply voltage of 0.39V, room temperature, noise and interferences all around the measuring station. This makes the measurement setup of our circuit very complex. The used on-chip measurement station is presented in Fig. 7. The DC and RF probing are

positioned into the PADs on the wafer. The measured power consumption is very low and remains constant while changing the control voltage. It is only 468 μW from 0.39 V supply voltage. That confirms the effectiveness of the subthreshold operation and of the design methodology.



Fig. 7. The used on-chip measurement station

An Agilent E4446A spectrum analyzer is used to measure the frequency and noise performances of the VCO. The output frequency spectrum measured for the two extreme values of V_{ctrl} are depicted in Fig.8. It can be seen that the oscillation frequency can be tuned from 5.144 GHz to 5.458 GHz with a tuning voltage varying from 0.001 to 0.39V.

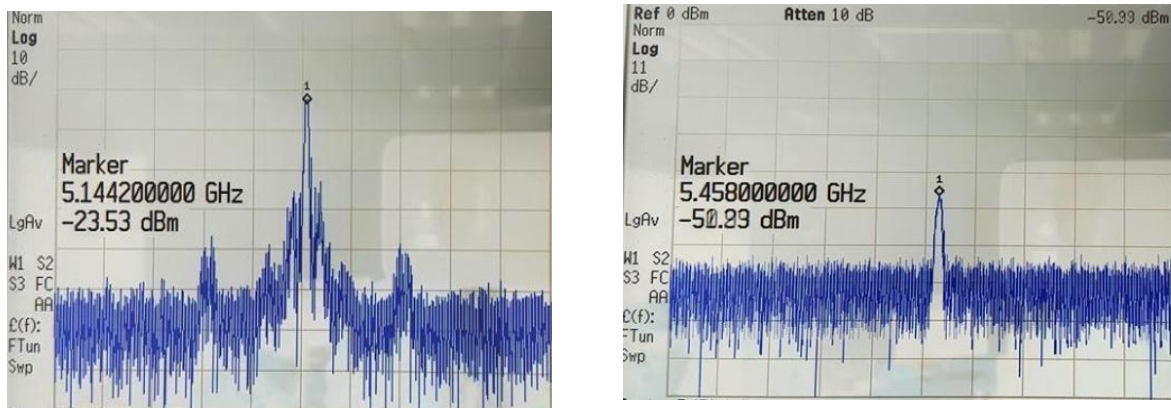


Fig. 8. The output frequency spectrum measured for (a) $V_{ctrl} = 0.001\text{V}$ and (b) $V_{ctrl} = 0.39\text{V}$

Figure 9 shows the measured phase noise variation. It is -104.41 dBc/Hz at 1MHz offset, in measure, while it is -112 dBc/Hz at 1MHz offset in post-layout simulations. A degradation of the phase noise is then observed due to the experimental conditions in a very noisy environment around the test station. In fact, the noise requirements are stringent when measuring RF circuits. So, it is necessary to use shielded chamber (which is not our case). Additional VCO noise measurement will be processed in low-noise and calibrated environment, as a future work, to address the correct phase noise.

The measured performances of our VCO are summarized in Table 2 and compared to other similar low-power VCOs operating around 5 GHz frequency band.

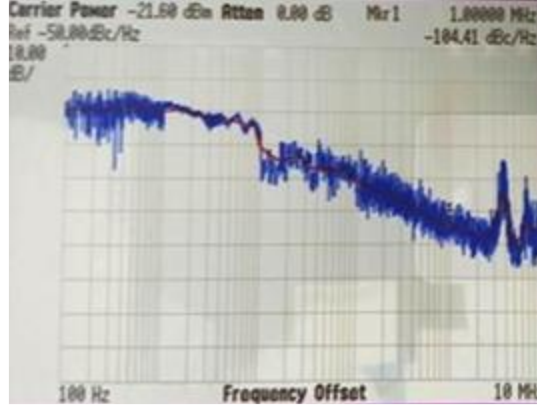


Fig. 9. The measured phase noise variation for $V_{ctrl} = 0.39$ V

A figure of merit (FOM) is usually used to judiciously compare the whole performances with other previously published works [14]. It is defined as

$$FOM = L\{\Delta f\} + 10\log(P_{DC}(mW)) - 20\log\left(\frac{f_{osc}}{f_{offset}}\right) \quad (2)$$

This FoM considers the most important performances of RF oscillators such as power consumption (P_{DC}), phase noise ($L\{\Delta f\}$) at the offset frequency (f_{offset}) and oscillation frequency f_{osc} .

It can be noted from Table 2 that our oscillator consumes the lowest power. Also, it achieves a comparable phase noise with the other works in post-layout simulations. A slight degradation of the phase noise in measure is observed due to the very noisy environment in which the measurements were carried out. Note that the phase noise needs to be measured in a low-noise environment soon. The implemented RF LC-VCO has good performances validating the design optimization methodology.

TABLE II. Performance comparison of the implemented LC-VCO with similar oscillators operating around 5 GHz

	[15]	[16]	[17]	[18]	[19]	This work
Process (nm)	180	180	180	180	180	130
Supply (V)	1.1	0.65	1.8	1.2	1.5	0.39
Frequency (GHz)	5.15	5.23	5.2	5.4	5.2	5.44
Power (mW)	0.8	2.37	2.59	0.9	3.71	0.468
Phase noise @1MHz (dBc/Hz)	-114.6	-115.1	-110	-112.7	-116	-104.4 / -112*
FOM (dBc/Hz)	-189.9	-185.7	-180	-188	-184	-182.4 / -191*

* PLS

V. CONCLUSION

This work describes the design and the implementation, in 0.13 μ m CMOS technology, of subthreshold sub-mW LC-VCOs operating at different frequency bands. These VCOs use the adaptive body biasing technique that allows a high immunity to PVT variations and can improve the startup constraint. Furthermore, a design methodology, aiming the power consumption optimization in LC VCOs while satisfying design constraints, has been presented in this paper. It has been applied to size the components

of subthreshold VCOs operating in different frequency bands. A 5.4GHz LC-VCO oscillator has been fabricated and measured. This VCO achieves in measure ultra-low power consumption of only 468 μ W drawn from 0.39V supply voltage. That makes the presented design and methodology suitable for IoT applications. Oscillation frequencies vary between 5.14 and 5.44 GHz with compact core area. The post-layout simulation results show a phase noise of -112dBc/Hz @1MHz offset frequency, while the measured phase noise is -104.41 dBc/Hz @1MHz. Note that the phase noise should be done in low-noise environment to address the correct phase noise in the future work.

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